Digital-to-Frequency Converters With a DTC: Theoretical Analysis of the Output SFDR

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***Abstract*— In this paper, we propose and analyze a pulse-output digital-to-frequency converter (DFC) generating square waves, which uses a digital-to-time converter (DTC) to correct the spurious tones (spurs) in the output spectrum. We focus on high-level architectural potential, discuss the design features of a DTC suitable for the proposed system, and explore possibilities and limits of this approach in terms of cleanness of the output spectrum. The behavioral model simulations confirm the theoretical analysis presented. Besides an analytical description of the output spurs, we derive a closed-form estimate of the worst-case spur, which leads to a simple design equation. This is useful to determine the DTC requirements [number of bits and integral non-linearity (INL)], given a certain spurious-free dynamic range (SFDR) target. We show that the maximum spur strength (in dBc) depends exclusively on the ratio between the output frequency and the clock frequency and the DTC features (number of bits, INL, and other impairments) and increases with the ratio by 6 dB/octave.**

***Index Terms*— Timing, radio frequency, digital-to-frequency converters, digital systems, digital circuits, phase modulation, phase control, frequency-domain analysis, time varying circuits, clocks, system-on-chip, mixed analog digital integrated circuits.**

I. Introduction

SQUARE waves or pulse-output clock signals are needed as timing references in many applications like digital clocks, samplers, and data converters [1], [2], Local Oscillators (LOs) for hard-switched mixers [3], [4] reference clocks in e.g. phased arrays [5] and clock recovery [6]. Furthermore, obtaining precise 50% duty-cycle is often important [7], e.g. for even-order harmonic suppression [8] or in cases where dividers are used to generate multi-phase clocks [9].

High-frequency pulse-output synthesizers with a digitally programmable frequency commonly employ Phase-Locked Loops (PLLs) [10]. However, Direct Digital Synthesizers (DDSs) [11] or a hybrid combination between DDS and PLL is also gaining interest [12], [13], especially in the context of Systems-on-Chip (SoCs), due to the DDS wide frequency range, extremely fine frequency resolution, immediate and phase-continuous frequency switch and compatibility with digital design flows. A key benefit for SoCs is that only one simple integer-N PLL is needed to be integrated on-chip to produce a high-frequency system clock, while multiple DDS blocks can generate from it all the other frequencies required in the system, in a flexible way. This solution is area-efficient and avoids coupling issues like in multi-PLL analog solutions, typically originating from coupling between resonating tank components used in the Voltage-Controlled Oscillators (VCOs) of PLLs running at different frequencies [3].

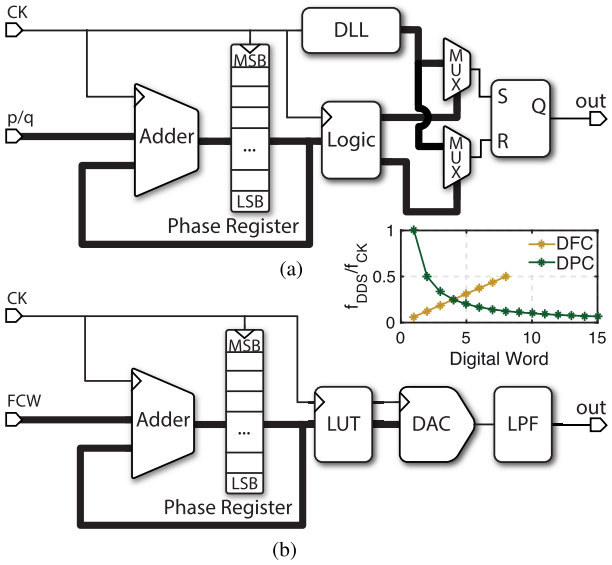

Fig. 1. Block scheme of a DPC [15] and traditional sine wave DFC [16]. The phase register synchronizes the current adder output to the clock. MSB and LSB stand for most/least significant bit of the adder output. The graph shows the output frequency grid for a 4–bit input word p/q (DPC) and FCW (DFC).

Direct digital frequency synthesis techniques are reviewed in [14], where two types are distinguished (Fig. 1): Digital-to-Period Converters (DPCs) and Digital-to-Frequency Converters (DFCs). DPCs generate a time-averaged *period* proportional to their digital input, while DFCs produce a time-averaged *frequency* proportional to their input code. For some applications it is convenient to control period, but for others digital frequency control is preferred, e.g. because of the linear instead of hyperbolic control function to the output frequency and ease of direct frequency modulation.

When starting from a fixed system clock, generating other period times or frequencies unavoidably comes with deterministic timing errors, often referred to as deterministic jitter, that appear in the output spectrum as spurious tones (spurs).These tones are potential causes of adjacent channel interference in multi-channel wireless communications systems [17] and degrade the dynamic range in data converters [18]. Thus,

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frequency synthesizers are often benchmarked in terms of maximum spur, e.g. fractional-N PLLs [19]–[21].

In the context of Digital Frequency Synthesis, Delay-Locked Loops (DLLs) have been proposed in the past for deterministic jitter correction [22]–[24], but recently DTCs with sub-pico-second resolution and linearity have become available [25], [26], so they can be used for this purpose.

DTCs for spur correction have been proposed inside DPC systems [15], [27]–[29], while in this paper we introduce a DTC in a DFC architecture, targeting 50 % duty-cycle pulse-output. We will analyze the DTC specifications (resolution, linearity) that impact the output-spectrum purity and derive simple equations to predict the maximum spurs, to facilitate the system design. Behavioral simulations will be used to prove the mathematical analysis.

Before doing so, we will give a brief overview of the literature in this field in Section II. Section III explains the DFC system architecture and identifies some Digital-to-Time Converter (DTC) features to improve the output spur level and speed. Section IV provides a detailed analysis of the output spurs, relating the DTC impairments to the output spectrum. In that section, the analysis is also validated by comparing it with behavioral simulations. Finally, conclusions are drawn in Section V.

II. Brief Overview on DPCs and DFCs

In a DPC (Fig. 1a), the control of the output period is accomplished by adding a continuously incremented delay to the edges of a fixed reference clock [29]–[33]. The most recent versions of DPCs, like the one shown in Fig. 1a, start with a single-phase reference clock, from a fixed-frequency PLL, and employ delay elements (usually DLL + multiplexer) to produce and select the output phase [24], [32].

DFCs were the first type of DDSs to be implemented [34], [35]. Sine wave DFCs (Fig. 1b) with a counter, a Look-Up-Table (LUT) with sine wave samples, a Digital-to-Analog Converter (DAC) and reconstruction filter are probably the best known DFCs [11], [16]. The counter acts as a digital phase accumulator controlled by a Frequency Control Word (FCW). The average frequency of the overflow bit is the target output frequency, and the multi-bit DAC interpolates to obtain a voltage sine wave. If a 1–bit output (often called pulse-output [11]) is wanted, this can also be done by a DTC. In [36], the potential of a digital delay element inside a DFC producing square waves was recognized and an algorithm was proposed to correct deterministic jitter, based on a DLL implementation.

By comparing a DFC with a DPC, one distinction is their application domain as mentioned above. However, it is also instructive to understand the different nature of their operation and, for their DTC-based implementations, the different role of the delay element. In a DPC the delay element is used to modify the period to adjust the output frequency ($= 1/T$). In contrast, in a counter-based DFC the average frequency already has the right (average) value [37], and the role of the delay element is the correction of the deterministic jitter, bringing the *instantaneous* frequency (not simply the time-averaged one) to the target. This ideally cancels the spurs in the output spectrum, thus acting as filtering (hence the name time-filtered square wave in [36]).

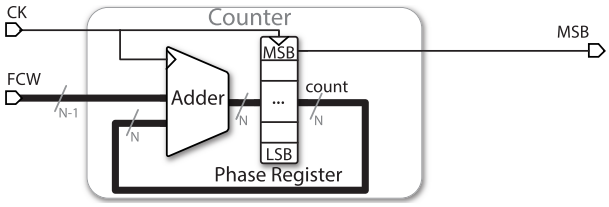

Fig. 2. Counter-based pulse-output DFC.

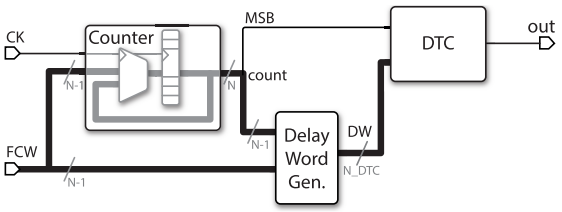

Fig. 3. Proposed pulse-output DFC retimed by a DTC.

Consider now the digitally-controlled delay element. In most of the aforementioned works, it has been implemented with a DLL plus multiplexer [22]–[24], [38]. However a DTC is substantially different from a DLL. A DLL requires two clock edges, between which the output edges are interpolated. It produces multiple outputs, i.e. a set of available edges for the multiplexer to choose from. Instead, a DTC is a *single-shot* device that only produces the edge that is needed, not wasting power in unused ones. Furthermore, a DTC acts in open loop, while a DLL has a feedback loop for delay control.

A DLL is typically limited to $5-6$ bits for a reference input clock of 1 GHz, as the delay of each buffer is typically limited to one gate delay ($\sim$10 ps in 65 nm technology). This resolution limits the output spectrum purity of digital synthesizers and additional spur suppression techniques are usually added. In [24], a 5−bit DLL produces maximum spurious tones of -24.5 dBc for an output frequency of 997 MHz, that can be pushed down to -48.2 dBc using dithering. The DDS in [39] achieves -65 dBc spurs for an output frequency of 496 MHz using a second order $\Sigma\Delta$. Vernier delay lines could be another alternative to DLLs [40], but they produce more edges than actually used, not being power efficient.

Recent research in DTCs for low-power fractional PLLs [41]–[43] has led to substantial improvements in DTC performance and has boosted the development of high-speed implementations at GHz frequencies that are suitable for use in DDS systems [25], [26], [29]. Most of these DTCs exploit a constant-slope delay generation [44] and achieve more than 10−bit resolution, a few LSB INL and a FoM down to a few fJ/conversion.

Choosing a DTC for deterministic jitter correction not only improves the output spectrum of the synthesizer, due to the $100\times$ increased resolution compared to the DLL, but also has a different impact on the output spectrum due to the different sources of DTC impairments, that this paper aims to analyze.

III. Proposed Architecture

A. Pulse-Output DFC

The core of the system proposed and analyzed in this work is the Pulse-Output DFC in Fig. 2, also known as

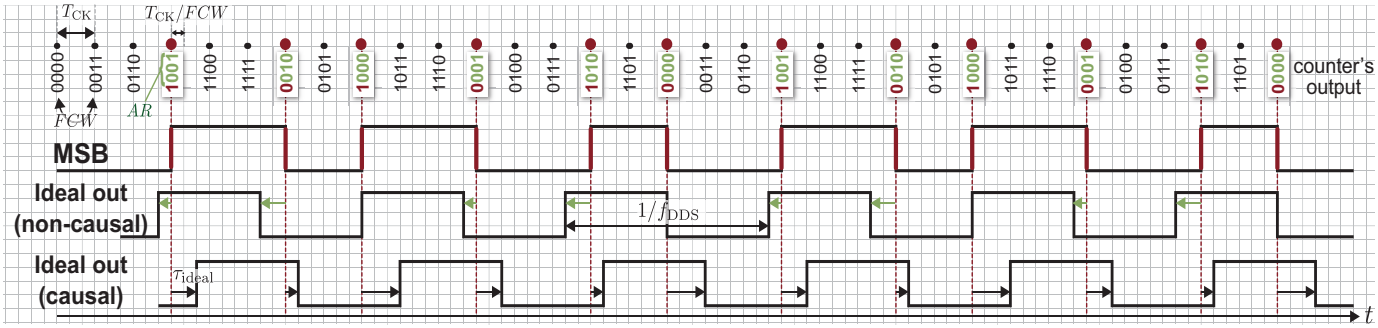

Fig. 4. Waveforms produced in the DTC-based DFC in Fig. 3 and quantization error between the ideal and real output. The example shown is for $N = 4$, $N_{DTC} = 3$, $FCW = 3$.

Pulse DDS [11]. This DDS concept has been known for decades [45], [46] and is based on the overflow rate of a binary counter with programmable step-size, named Frequency Control Word (FCW). The counter, acting as phase accumulator, consists of an $N-$bit adder and an $N-$bit register, thus the operation is modulo 2^N. The MSB of the counter is a square wave that has on average the target output frequency [37]:

$$f_{DDS} = \frac{f_{CK}}{2^N} \cdot FCW, \quad 0 \leq FCW \leq 2^{N-1} \tag{1}$$

where f_{DDS} is the average synthesized frequency of the Pulse-Output DFC, and f_{CK} is the (fixed input) clock frequency. The maximum achievable value of f_{DDS} is therefore $f_{CK}/2$. The frequency step $f_{CK}\,2^{-N}$ can be improved by increasing the size N of the counter. Based on (1), a DFC can also be seen as a programmable frequency divider [16].

B. DTC for Edge Retiming

The counter's MSB in the Pulse-Output DFC in Fig. 2 suffers from timing irregularities due to the coarse phase increment of the accumulator. To correct them, the MSB edges can be re-timed with a DTC, as shown in the proposed architecture in Fig. 3. The least-significant bits of the counter are used to compute the DTC delay word DW. In this architecture, the DTC acts on both rising and falling edges on its input waveform MSB, to obtain a 50 % duty-cycled square wave at the output. The correction mechanism is illustrated in the time domain in Fig. 4, for the case $N = 4$. The MSB of a counter with programmable step-size FCW is shown over time, together with the total counter output, which is updated every clock period T_{CK}. When FCW is not a power of 2, the coarse counter's increment causes the MSB edges to have a periodically incorrect timing, compared to the ideal output (second signal in Fig. 4). These periodic errors, together with the square waves not being 50 % duty-cycled on short term, give rise to spurs in the output spectrum [16].

The elegant correction algorithm proposed in [36] for a DFC with Digital Delay Line (DDL) can also be applied here to calculate, at every MSB edge, the DTC delay. The algorithm is based on the observation that the counter residue AR (i.e. the counter output excluding its MSB), read out at each edge of the waveform MSB, contains the excess error compared to the corresponding ideal non-causal edge. This can be seen in Fig. 4. The signal ideal out is the DTC output from Fig. 3. The grid pitch in Fig. 4 is T_{CK}/FCW which is the equivalent time for the counter to increase its output by one. The edge positions of signal ideal out (non-causal) are AR pitches before the corresponding edges of MSB. The output waveform is called non-causal as it would be produced by adding negative delays to the edges of MSB. In [36] it was proposed to make the output causal by adding a clock period to all the output edges. Thus, the net positive delay added to each MSB edge to produce the causal ideal output (black rightward arrows in Fig. 4) is

$$\tau_{ideal} = (FCW - AR)\,\frac{T_{CK}}{FCW} \tag{2}$$

where counter residue AR is bounded: $0 \leq AR \leq FCW - 1$. The maximum required delay to be added (i.e. the programmable delay range needed) is T_{CK}.

While digital correction schemes are more versatile and easier to build than their analog counterparts [37], [47], they can only provide quantized and hence approximated values of (2). If N_{DTC} is the number of bits of a DTC with full-scale delay T_{CK}, (2) can be rewritten as function of the DTC time resolution $T_{CK}/2^{N_{DTC}}$ as

$$\tau_{ideal} = \left[(FCW - AR)\,\frac{2^{N_{DTC}}}{FCW}\right]\frac{T_{CK}}{2^{N_{DTC}}} \tag{3}$$

where the term in square brackets is the current delay word.

C. Pushing Down Spur Levels With a DTC

This section considers design aspects of the Pulse-Output DFC + DTC in Fig. 3, with focus on the output spur levels and frequency. These considerations will lead to a set of parameters describing the high-level behavior of the DTC, that will be used in the behavioral modeling explained in Section IV.

As mentioned before, spur levels depend on the quality of the DTC. Besides the quantization errors, the DTC Integral Non-Linearity (INL) is also crucial for the output spurs. In fact, it is directly related to the harmonic distortion [2], since it implies a deviation of the DTC transfer curve from the straight line. The DTC DNL, instead, is less important here. Assuming it is divided into correlated and uncorrelated parts [1], its uncorrelated fraction can be considered as quantization error (section IV-A), while its correlated fraction summed up is the main source of the INL, so it is taken into account with it (section IV-D).

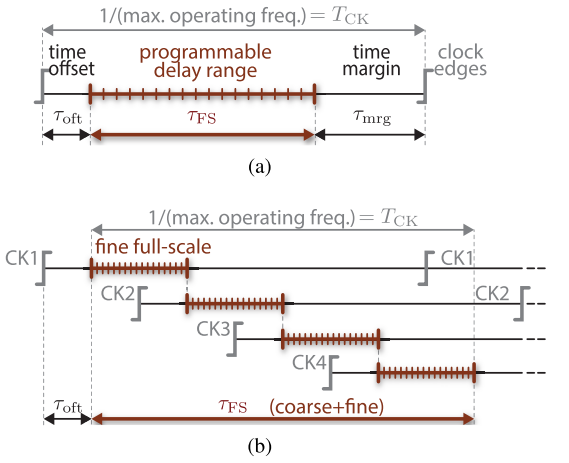

Fig. 5. Achieving a full programmable DTC delay range with dividers. Example based on the four-phase generator in [9]. (a) *Time slots for a single DTC.* (b) *Coarse + fine delay scheme.*

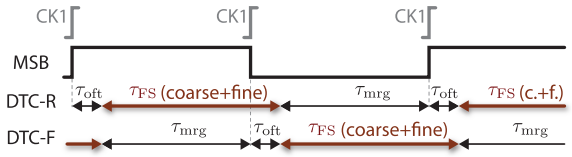

Fig. 6. Two time-interleaved DTCs for increased maximum output frequency.

The DTC maximum operating frequency is $1/T_{CK}$ (when the waveform MSB changes at every clock edge), and it should provide a programmable delay range of T_{CK}. However, a practical DTC has a non-zero time-offset, as shown in Fig. 5a, and needs a time margin after operation before it is ready for use again. Hence, its programmable delay-range (full-scale) is less than T_{CK}. To address this DTC limitation, we will consider in the model developed in this work a coarse/fine delay scheme, obtained with frequency dividers, as shown in Fig. 5b. Generating four clock phases using dividers by 2 as in [9] allows a DTC time-margin which should be sufficient for most DTC implementations, as shown in the time allocation in Fig. 5b. The coarse delay is provided by selecting one clock phase, while the fine delay is generated by the DTC, which is clocked by the selected phase. In this way, the fine full-scale required for the DTC is lowered to $T_{CK}/4$. A calibration will be needed to guarantee that the total programmable delay range T_{CK} will be covered continuously between the coarse and fine mechanisms.

Since the fastest DTC implementations work at a couple of GHz [25], [26], the system would produce square waves controlled on both edges at maximum 1 GHz. The output frequency can be pushed further with time-interleaving, where different DTCs work in succession. To cover this option in our model, the simplest form of time-interleaving - with only two DTCs - will be considered, as shown in Fig. 6. Note that the number of time-interleaved blocks chosen has no relation with the number of clock phases for the coarse delay. In fact, the time-interleaving technique separates two consecutive full-scale delay-ranges (see, for example, the red arrows for DTC-R (Rise) in Fig. 6), but this choice is independent from the way these delay-ranges are internally sub-divided (Fig. 5b).

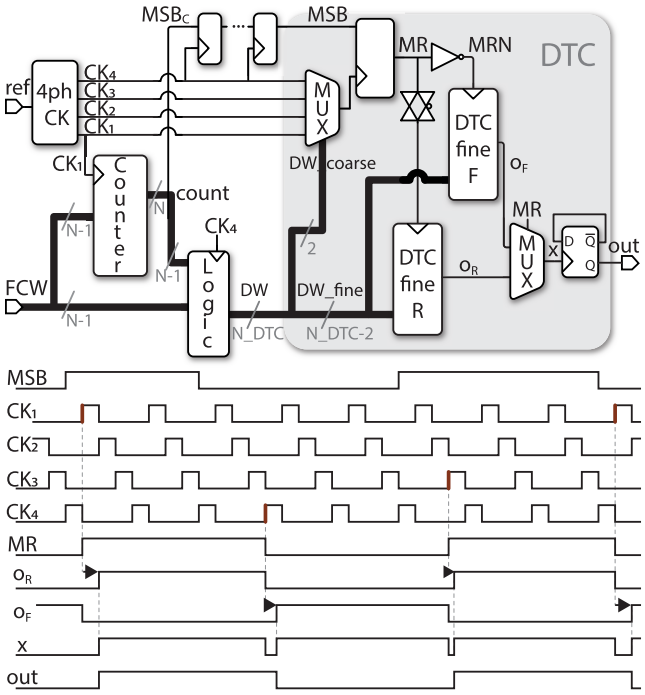

Fig. 7. Detailed model of the proposed DTC-based pulse-output DFC, with the DTC in gray.

With two DTCs alternating at every MSB edge, one DTC happens to be associated with MSB rising edges, the other one with falling edges. For this reason, the two DTCs will be named DTC-R (Rise) and DTC-F (Fall). As additional benefit, time-interleaving can result in extra time margin between the conversion and the next triggering edge, allowing for a better DTC settling to reduce memory effects that would otherwise degrade its INL [41], [44]. In terms of dynamic power consumption, two interleaved CMOS DTCs are almost equivalent to a single DTC operating at double frequency. However, a gain mismatch between interleaved DTCs would produce different delays, whose effect on the output spectrum will be discussed in Section IV.

D. DTC-Based Pulse-Output DFC

The block scheme of the Pulse-Output DFC in Fig. 3 can be detailed based on the features described in the previous paragraphs, resulting in Fig. 7. The DTC block in gray now has a coarse/fine structure and contains a R(ise)- and F(all)-DTC. The fine DTCs can be any high-speed implementation discussed in Section II.[1]

The four clock phases CK_1-CK_4 are derived from a reference signal with doubled frequency: $f_{CK} = f_{ref}/2$. The $N-$bit counter (phase accumulator) is clocked by CK_1. A logic block clocked by CK_4 computes the delay word DW from (3). The counter's most significant bit MSB_C is resampled multiple times with CK_4 to match the delay of the logic block. Thus,

[1]Whatever the delay mechanism of the DTC is, e.g. constant-slope charging of a capacitor starting from a variable start voltage [25], [26], variable current charging [37], [47], [48] or a variable capacitive load [29], all DTCs can be characterized by their number of bits, INL and full-scale delay, as used in Fig. 7. The particular DTC implementation does however impact the physical causes for INL but that goes beyond the scope of this paper.

the resulting signal MSB is synchronized with DW. Out of the $N_{\mathrm{DTC}} = N - 1$ bits of DW, the two most significant bits control the coarse delay: they select the correct clock phase CK_1-CK_4 to resample MSB, in order to produce the signal MR (resampled MSB). The remaining $N_{\mathrm{DTC}} - 2$ bits of DW determine the fine delay. They are sent to the two interleaved DTCs, activated by MR and its inverted form MRN. The outputs o_R and o_F of the two interleaved DTCs are then combined to produce the output signal out, as shown in Fig. 7. A delta-sigma modulator before the counter would change the profile of the output spurs, thus relaxing the resolution and linearity specifications of the DTC for spur correction. However, in this paper we will study the effect of a DTC as the only aid for spur canceling, in a deterministic, instantaneous way, to investigate how good is the DTC correction before resorting to orthogonal techniques.

IV. Output Spectrum in a DTC-Based DFC

The output spectrum of the proposed DFC in Fig. 7 will be analyzed, focusing on spurs produced by deterministic errors and on the effect of the DTC impairments on the Spurious-Free Dynamic Range (SFDR). The reference clock is assumed jitterless since it can be produced by a low noise integer-NPLL [49], [50] and its frequency is divided by the DFC logic, thus further reducing its impact on phase noise [51]. If the goal is to produce square waves with 50% duty-cycle, the output's odd harmonics should not be considered in the evaluation of the SFDR (they are part of the wanted signal). We will first investigate the effect of the DTC number of bits N_{DTC} (quantization error), while the DTC impairments will be analyzed in Section IV-D.

A. Effect of DTC Quantization Error on the Output Spectrum

Assume that the counter in Fig. 7 is reset to zero as initial state. Its finite length N implies its output is calculated modulo 2^N. The number of steps required to make the counter return to its starting value is the numerical period of the counter's output and is often called Grand Repetition Rate (GRR) [16]:

$$GRR \triangleq \frac{2^N}{\mathrm{GCD}\left(2^N, FCW\right)} \tag{4}$$

where GCD (.) denotes the greatest common divisor. If f_{CK} is the frequency of the counter's clock, then the repetition frequency of the phase register is f_{CK}/GRR.

The output spurs are residual errors coming the correction of signal MSB and therefore they are placed at integer multiples of the counter's repetition rate f_{CK}/GRR. The output frequency of the DFC can also be expressed as a function of this rate, from (1) and (4):

$$f_{\mathrm{DDS}} = \frac{f_{\mathrm{CK}}}{GRR} \cdot \frac{FCW}{\mathrm{GCD}\left(2^N, FCW\right)} \tag{5}$$

In this section we will show that the sub-harmonics, i.e. the spurs located at frequencies between DC and f_{DDS}, are related to the Discrete Fourier Transform (DFT) of the DTC quantization error. The analytical procedure follows similar steps as the analysis for DPCs [15], [27], targeted on finding a sequence that models the output quantization error. However, since the boundary conditions of DPCs and DFCs are different, as will be shown in Table I and in Fig. 11, the two quantization sequences do not share the same symmetries, except for special cases where sequences are identical.

TABLE I
Correspondent Variables Between [15] and This Work

	DPC [15]	This DFC
output frequency	$\frac{T_{\mathrm{DDS}}}{T_{\mathrm{CK}}} \triangleq \frac{p}{q} \rightarrow \frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} = \frac{q}{p}$	$\frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} = \frac{FCW}{2^N}$
num. of DTC quantiz. levels	n_p †	$2^{N_{\mathrm{DTC}}}$
periodicity of quantiz. error	$2K_Q = 2\frac{q}{\mathrm{GCD}\,(n_p, q)}$	$L = 2\,\frac{FCW}{\mathrm{GCD}\,(2^N, FCW)}$
output freq. range	$\frac{1}{2^I} \lesssim \frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} \leqslant 1$	$\frac{1}{2^N} \leqslant \frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} \leqslant \frac{1}{2}$
frequency resolution	$\Delta f_{\mathrm{DDS}} = \frac{f_{\mathrm{DDS}}^2}{2^M f_{\mathrm{CK}}}$	$\Delta f_{\mathrm{DDS}} = \frac{f_{\mathrm{CK}}}{2^N}$

† N in [15], but here N already indicates the number of bits of the counter.

Fig. 8 shows the DTC output as a function of time, for the case $N = 4$ and $FCW = 3$. The output is shown for both the ideal case of a DTC with infinite resolution and for a DTC with a finite number of bits $N_{\mathrm{DTC}} = 3$. Following similar steps as in [15] and [27], we can define the quantization error sequence $q_{\mathrm{e}}[l]$ as the difference between corresponding edges of the real quantized and ideal output, normalized to the DTC LSB $T_{\mathrm{CK}}/2^{N_{\mathrm{DTC}}}$. The index l acts as edge identifier, with $l \geq 1$. For our DFC, the following can be derived:

$$q_{\mathrm{e}}[l] \triangleq (-1)^l \left\{DW[l] - DW_{\mathrm{ideal}}[l]\right\} \tag{6}$$

with

$$DW[l] = Q\left\langle \frac{FCW - AR[l]}{FCW} \cdot 2^{N_{\mathrm{DTC}}} \right\rangle \tag{7}$$

$$DW_{\mathrm{ideal}}[l] = \frac{FCW - AR[l]}{FCW} \cdot 2^{N_{\mathrm{DTC}}} \tag{8}$$

and

$$AR[l] = Q\left\langle \frac{l}{2}\, GRR \frac{\mathrm{GCD}\left(2^N, FCW\right)}{FCW} + 1 - 2^{-(N_{\mathrm{DTC}}+1)} \right\rangle \cdot FCW - \frac{l}{2}\, 2^N \tag{9}$$

The operator $Q\langle\cdot\rangle$ denotes quantization, the easiest to implement being truncation, which will be considered in this work. We will show later that the exact choice of quantization has negligible impact on spur performance. As such, since the quantization errors are smaller than one DTC LSB, $|q_{\mathrm{e}}[l]| < 1\ \forall l$. Specifically, $0 \leqslant q_e[l] < 1$ for rising edges (odd l) and $-1 < q_e[l] \leqslant 0$ for falling edges (even l).

The periodicity of q_e in (6) in number of edges L is

$$L = 2\,\frac{FCW}{\mathrm{GCD}\left(2^N, FCW\right)} \tag{10}$$

Both the counter residue AR and the delay word DW (equations (7)-(9)) have period $L/2$. Moreover, the sequence $q_{\mathrm{e}}[l]$ has half-wave symmetry, that is $q_{\mathrm{e}}[l + L/2] = -q_{\mathrm{e}}[l]$.

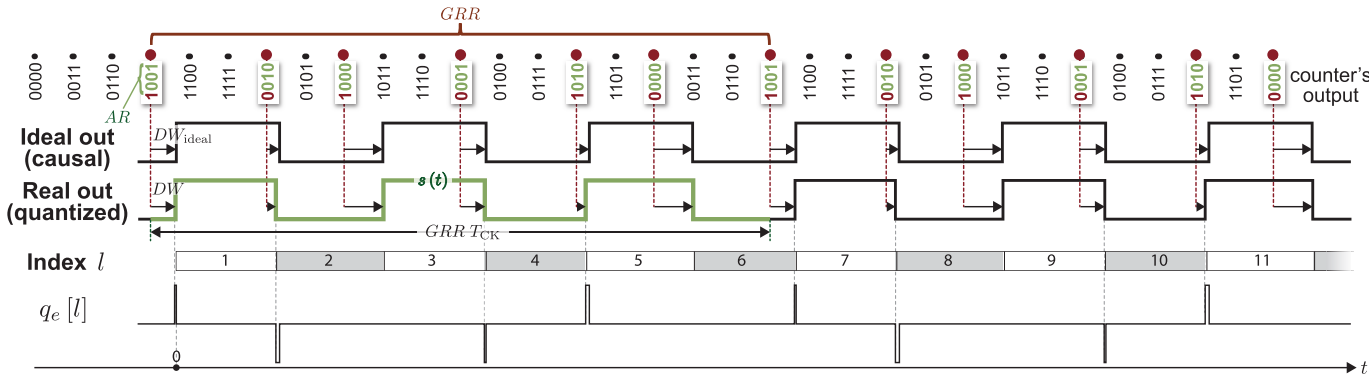

Fig. 8. Waveforms produced in the proposed DFC and quantization error between the ideal and real output. Example shown for $N = 4$, $N_{\mathrm{DTC}} = 3$, $FCW = 3$, thus $L = 6$.

We can identify the signal $s\,(t)$ in green in Fig. 8, defined in the time interval $GRR \cdot T_{\mathrm{CK}}$, and we can express the output, that we will name $x\,(t)$, as a periodic extension of $s\,(t)$:

$$x\,(t) = \sum_{\alpha=-\infty}^{+\infty} s\,(t - \alpha\ GRR\ T_{\mathrm{CK}}) \tag{11}$$

Thus, the output spectrum can be written as

$$X\,(f) = \sum_{h=-\infty}^{+\infty} X_h\ \delta\left(f - h\,\frac{f_{\mathrm{CK}}}{GRR}\right) \tag{12}$$

The output spectrum is thus a Dirac comb with impulses placed at multiples of f_{CK}/GRR and complex weights X_h. Indices h that are integer multiples of $L/2$ correspond to signal harmonics, as expressed in (5) for the case $h = L/2$. The other values of h correspond to fractional spurs, due to the DTC quantization error. Using the Fourier transform properties for periodic signals [52], the strength of the h^{th} fractional spur can be shown to be (see Appendix A):

$$X_h \approx -\frac{A}{GRR\ 2^{N_{\mathrm{DTC}}}} e^{j2\pi\frac{h}{L}}\ Q_{\mathrm{e}}\,[h] \tag{13}$$

where A is the output signal amplitude, with

$$Q_{\mathrm{e}}\,[h] = \sum_{l=1}^{L} q_{\mathrm{e}}\,[l]\, e^{-j2\pi\frac{h}{L}l} \tag{14}$$

As the sequence $q_{\mathrm{e}}\,[l]$ is real, its DFT $Q_{\mathrm{e}}\,[h]$ is conjugate symmetric [53] ($Q_{\mathrm{e}}\,[h] = Q_{\mathrm{e}}^{*}\,[L-h]$), meaning that the spurs repeat around each harmonic with equal absolute power. Therefore, only the sub-harmonics below the fundamental are relevant to study the output spectrum and to determine the SFDR. Due to the half-wave symmetry of the sequence $q_{\mathrm{e}}\,[l]$, $X_h = 0$ for even values of h.

Fig. 9 shows the simulated power spectrum of both the signal MSB and the output, as well as the calculated sub-harmonics using (13) and (14). They are plotted as a function of the normalized frequency f/f_{DDS}, for a typical example case $N = 12$, $N_{\mathrm{DTC}} = 11$, $FCW = 1792$. The calculations with (13) and (14) track the simulated spurs with an accuracy within 0.02 dB. Clearly, DTC retiming makes a big difference: it pushes the sub-harmonic spurs down by almost 70 dB to 73 dB SFDR. The spurs are repeated around every

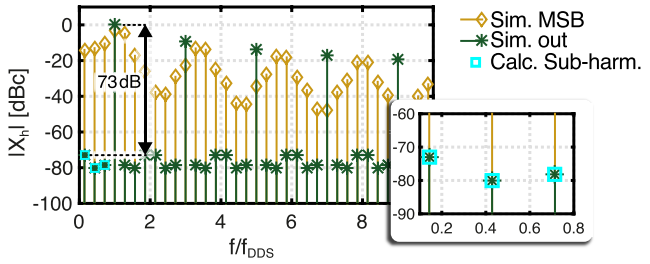

Fig. 9. Output spectrum from behavioral simulations of the proposed DFC, for $N = 12$, $N_{\mathrm{DTC}} = 11$, $FCW = 1792$.

odd harmonic. In this example, the sub-harmonics are only limited by the finite resolution of the 11-bit DTC and they are placed at odd multiples of the normalized counter rate $(f_{\mathrm{CK}}/GRR)\,/f_{\mathrm{DDS}} = 1/7$.

B. Worst-Case Spur: Closed-Form Estimate

While (13) gives an estimate for each sub-harmonic, a closed-form estimate for the worst-case spur amplitude, given the values of N, N_{DTC} and FCW, would be useful. It can provide a quick indication of SFDR for design purposes, e.g. to derive DTC requirements.

Note that the quantization error sequence $q_{\mathrm{e}}\,[l]$ as defined in (6) has a fixed offset $0.5\cdot(-1)^{l+1}$ compared to rounding, due to the fact that DW is a truncated version of DW_{ideal}. Any offset in $q_{\mathrm{e}}\,[l]$ can be seen as a rigid shift of the quantized output in Fig. 8, it affects only the power at the fundamental frequency, without changing the output fractional sub-harmonics. Therefore, we will consider for the calculations the zero-offset quantization sequence:

$$q_{\mathrm{e0}}\,[l] \triangleq q_{\mathrm{e}}\,[l] - \frac{1}{2}(-1)^{l+1} \tag{15}$$

Note: $|q_{\mathrm{e0}}\,[l]| < 1/2\,\forall l$ and $q_{\mathrm{e0}}\,[l + L/2] = -q_{\mathrm{e0}}\,[l]$ (half-wave symmetry). As the same $q_{\mathrm{e0}}\,[l]$ can be obtained if we assume $Q\,\langle\cdot\rangle$ to be rounding instead of truncation, the following SFDR equations are valid for any reasonable $Q\,\langle\cdot\rangle$ −function: floor $\lfloor\cdot\rfloor$, ceil $\lceil\cdot\rceil$ or nearest integer function $\lceil\cdot\rfloor$.

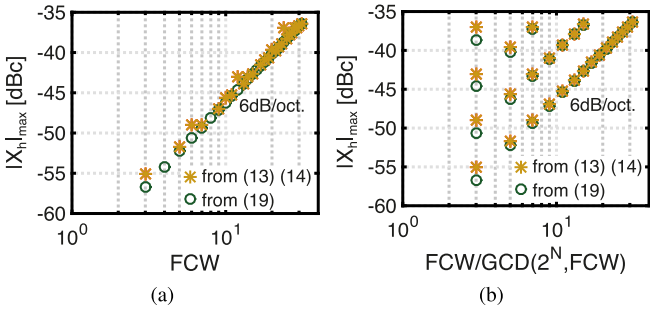

Fig. 10. Magnitude of the worst-case spur from (13), (14) and (19), vs (a) FCW and (b) $FCW/\mathrm{GCD}\left(2^N, FCW\right)$. Case $N = 6$ and $N_{\mathrm{DTC}} = 5$.

Using (13), (14) and the half-wave symmetry of $q_{\mathrm{e0}}[l]$, the worst-case spur relative to the fundamental output is

$$\max_h \frac{|X_h|}{A/\pi} \approx \frac{2\pi}{GRR\ 2^{N_{\mathrm{DTC}}}} \max_h \left| \sum_{l=1}^{L/2} q_{\mathrm{e0}}[l]\, e^{-j2\pi \frac{h}{L} l} \right| \quad (16)$$

With $h \in [1, \ldots, L/2-1]$. While the sign of $q_e[l]$ is determined by the parity of the index l, the sign of $q_{\mathrm{e0}}[l]$ for each l can be positive of negative. Thus, in analogy with data converters [1], $q_{\mathrm{e0}}[l]$ can be considered a uniform random variable $\tilde{q}_{\mathrm{e0}}$ from $-1/2$ to $1/2$ and approximated in (16) with the average value $E\{|\tilde{q}_{\mathrm{e0}}|\} = 1/4$. Therefore:

$$\begin{aligned} \max_h \left| \sum_{l=1}^{L/2} q_{\mathrm{e0}}[l]\, e^{-j2\pi \frac{h}{L} l} \right| &\approx E\{|\tilde{q}_{\mathrm{e0}}|\} \max_h \left| \sum_{l=1}^{L/2} e^{-j2\pi \frac{h}{L} l} \right| \\ &\approx \frac{1}{4}\frac{L}{\pi} \end{aligned} \quad (17)$$

where the last step in (17) comes from the following relation that is proven mathematically in Appendix B:

$$\max_h \left| \sum_{l=1}^{L/2} e^{-j2\pi \frac{h}{L} l} \right| \approx \frac{L}{\pi} \quad (18)$$

Therefore, the worst-case spur can be approximated as:

$$\max_h \frac{|X_h|}{A/\pi} \approx \frac{2\pi}{GRR\ 2^{N_{\mathrm{DTC}}}} \frac{L}{4\pi} = \frac{1}{2^N\ 2^{N_{\mathrm{DTC}}}} FCW \quad (19)$$

Fig. 10a shows the magnitude of the worst-case spur (in dBc) as a function of FCW, from (13) and (14), as well as its approximation (19). We chose the case $N = 6$ and $N_{\mathrm{DTC}} = 5$ for plot readability. The worst quantization spur does not depend on the clock frequency itself, but only on the ratio $f_{\mathrm{DDS}}/f_{\mathrm{CK}}$, as can be shown by re-writing (19) using (1):

$$\max_h \frac{|X_h|}{A/\pi} \approx \frac{1}{2^{N_{\mathrm{DTC}}}} \frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} \qquad (\mathrm{DFC}) \quad (20)$$

Moreover, from (19), the worst quantization spur increases by 6 dB every octave increase in FCW. This result can intuitively be understood by realizing that the average frequency is defined by the adder, while the DTC compensates for deterministic jitter, leaving a rather random residual quantization rms-error with power $\Delta^2/12$ related to the LSB-delay Δ of the DTC. As this quantization error is roughly constant in terms of rms-jitter, its phase noise contribution scales with $1/f_{\mathrm{DDS}}^2$, i.e. with 6 dB per octave of FCW.

The error with the fitting line (19) depends only on L, i.e. on the ratio $FCW/\mathrm{GCD}\left(2^N, FCW\right)$, as shown in Fig. 10b. The maximum error is 1.65 dB at $FCW = 3$ and its multiples with a power of 2 (corresponding to the same L). This error is mainly due to the approximation of $q_{\mathrm{e0}}[l]$ as random variable, that is less accurate for small L. Moreover, 0.4 dB of the total error is due to the approximation (18). Plots with different values of N and N_{DTC} showed that the absolute value of the spurs changes in accordance with (19) but the error with the fitting line stays the same and only depends on L.

C. Spectrum of DFCs Versus DPCs

A DFC can be compared to a DPC, such as the one shown in Fig. 1a, and analyzed in [15], in terms of their maximum quantization spurs, using the same DTC parameters.

The input word of the DPC is expressed in [15] as a binary ratio p/q. Table I lists the variables related to the DPC in [15] and their correspondent ones related to the DFC in this work. The ratio p/q is represented using I integer bits and M fractional bits. The denominator q is crucial to determine the periodicity of the quantization error $2K_Q$. It can be found by locating the right-most nonzero bit in the fractional part of the input word. By approximating the exponential in equation (46) of [15], it can be shown that for a DPC

$$\max_h \frac{|X_h|}{A/\pi} = \begin{cases} \frac{\pi}{2}\frac{1}{n_p}\frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} & K_Q = 1 \\ \frac{\pi}{2\sqrt{2}}\frac{1}{n_p}\frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} & K_Q = 2 \\ \frac{\pi}{3}\frac{1}{n_p}\frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} & K_Q = 3 \\ \frac{1}{n_p}\frac{f_{\mathrm{DDS}}}{f_{\mathrm{CK}}} & K_Q > 3 \end{cases} \qquad (\mathrm{DPC}) \quad (21)$$

Equation (21) becomes the same as (20) for $K_Q > 3$ and $n_p = 2^{N_{\mathrm{DTC}}}$. In fact, for a fair comparison, we assume equal number of quantization levels of the DTC for both the systems. The comparison DPC-DFC in terms of the maximum spurs is shown in Fig. 11 for three values of K_Q in the DPC. For clarity, we chose an example with only a few bits $N = 4$ and $N_{\mathrm{DTC}} = 3$. Obviously, this produces high maximum spurs, but we are interested in the spur comparison rather than the spur values. The assumptions for the comparison in Fig. 11 are listed in the inserted table. For the DPC, the plots in Fig. 11 are traced by fixing $q = 2^M$, with p going from 2^M to $2^{I+M} - 1$, while for the DFC, FCW goes from 1 to 2^{N-1}. The assumption $I = N$ ensures the maximum frequency overlap between the two systems, as can be seen from the expressions of the output frequency range in Table I. The points corresponding to integer ratios $f_{\mathrm{CK}}/f_{\mathrm{DDS}}$ are missing in Fig. 11, since they do not produce fractional spurs and (20)-(21) are not valid for those points.

Different observations can be made from Fig. 11. As for the DPC plots, by increasing K_Q from 1 to 4, the maximum spurs decrease by $20\log_{10}(\pi/2) = 3.9$ dB and reaches the same spur levels as the DFC for $K_Q > 3$. This means that the

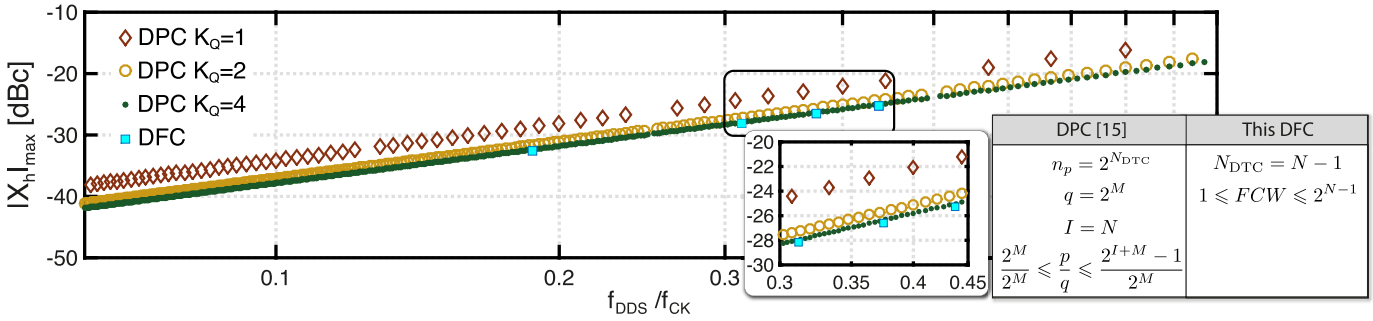

Fig. 11. Comparison of the maximum spurs in dBc, in a DFC (from (20)) and in a DPC (from (21)) for $K_Q = 1, 2, 4$ (corresponding to $M = 2, 4, 5$), $N = I = 4$, $N_{\rm DTC} = 3$. The table lists the assumptions for the comparison DPC-DFC.

maximum DTC quantization spur can be made the same for DFCs and DPCs with a proper choice of K_Q. Increasing K_Q means increasing M in Fig. 11. This explains why the points' density in the plots increases with K_Q, as higher M implies a smaller frequency resolution in the DPC (see Table I).

The main conclusion is that, at comparable output frequency range and at equal DTC, the DPC is not worse than the DFC in terms of the maximum spur achievable. However, the frequency resolution is different for the two systems. For a DPC it is not fixed, depending on the output frequency f_{DDS} itself, so it changes with the input word (see Table I and Fig. 1a), while for a DFC is constant since it depends on quantities that do not change during the system operation.

As for the output frequency range ($x-$domain of the plots), the upper limit $1/2$ in a DFC compared to 1 for the DPC is a false limitation. It can be brought to 1 at the expense of higher hardware complexity, by making the counter in the DFC sensitive to both the clock edges. In a DPC the logic is usually single-edge triggered, but indeed the upper limit 1 is due to the selection of both the clock edges from a DLL [15].

In a DPC, by changing the input word p, with q fixed, the periodicity $2K_Q$ of the quantization sequence is fixed, and therefore so are the number of subharmonics. In other words, for a fixed q, the set of subharmonics is always the same, while p changes only their position in the spectrum. In a DFC, the periodicity L of the quantization sequence is proportional to the input word FCW, so the set of subharmonics cannot be reduced to a few classes. This shows there is a fundamental difference in output spectrum between DFCs and DPCs.

D. Effect of DTC Impairments on the DFC Spectrum

Any DTC impairment results in timing errors in the correction of deterministic jitter, thus causing a spur increase in the output spectrum. The DTC also introduces random jitter, but this is less of a concern, since the DTC acts on the edges of a divided signal (the pulse-output DFC can be seen as a frequency divider). The random jitter produced in recent DTC implementations is in the order of $\sim$ 100 fs [25], [41], [54], so that the DTC contribution to the output random jitter for an output frequency of 1 GHz would be only 0.01%. Therefore, in this work we will focus only on deterministic jitter, which is manifested in the form of spurs.

A code-dependent error means that the DTC provides a deviation from the "ideal" delay that depends on its input word DW. However, from a modeling perspective, the effect on the resulting quantization error is the same as in the case of an ideal DTC with the error concentrated in DW itself. Therefore, the term $DW\,[l]$ in (6) can be expanded to incorporate the sources of errors coming from the DTC.

The DTC structure shown in Fig. 7 has four main causes of deterministic timing errors that affect the output spectrum: 1) INL, 2) time errors between the four clock phases, 3) full-scale time errors of the fine DTCs, 4) full-scale time mismatches between the two interleaved DTCs (R and F). Since these effects are mutually independent, they can be considered individually and then superimposed to derive a unified expression for the quantization error. All these sources of errors increase the output spurs and they can in principle be calibrated out.

1) INL: The DTC INL [1] is a dimensionless error only dependent on the input delay word: $\mathrm{INL}\,[DW\,[l]] \triangleq \mathrm{INL}\,[l]$. It can be directly added to DW in (6) so that:

$$q_{\rm eINL}\,[l] = (-1)^l\,\{DW\,[l] + \mathrm{INL}\,[l] - DW_{\rm ideal}\,[l]\} \quad (22)$$

The DFT in (14) should be calculated with the quantization sequence in (22).

2) Timing Errors Between the Four Clock Phases: Any timing error in the clock phases, e.g. resulting from duty-cycle errors in the reference signal, produce an error in the DTC coarse delay. As the total delay is the sum of coarse and fine delay, we can write:

$$q_{\rm eCKph}\,[l] = (-1)^l\left\{DW\,[l] + EW_{\rm CKph}\,[l] - DW_{\rm ideal}\,[l]\right\} \quad (23)$$

where the error word $EW_{CKph}\,[l]$ is the timing error of the current phase (function of the index l), normalized to the DTC resolution $T_{\rm CK}/2^{N_{\rm DTC}}$.

3) DTC Full-Scale Errors: The delay word DW can be separated into its coarse and fine components:

$$DW\,[l] = DW_{\rm coarse}\,[l] + DW_{\rm fine}\,[l] \quad (24)$$

For example, $1101_2 = 1100_2 + 0001_2$. The fine full-scale can differ from its nominal value $T_{\rm CK}/4$, because of variations of the period T_{CK}, or the DTC resolution due to PVT variations. The DTC delay (in seconds) can be written as:

$$\tau\,[l] = DW_{\rm coarse}\,[l]\,\frac{T_{\rm CK}}{2^{N_{\rm DTC}}} + DW_{\rm fine}\,[l]\,\frac{\tau_{\rm FS\,fine}}{2^{N_{\rm DTC}-2}} \quad (25)$$

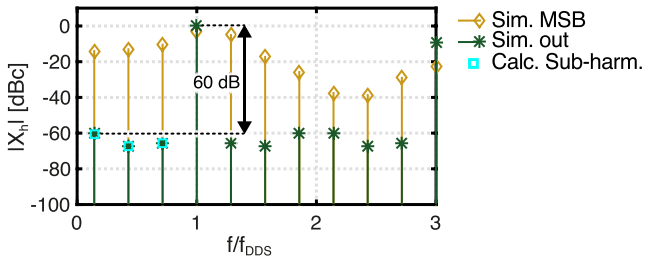

Fig. 12. Output spectrum with DTC impairments. Parabolic INL with $\mathrm{INL_{max}} = 3\,\mathrm{LSB}$, 2 DTC LSB error between clock phases CK_1 and CK_2, and 3 DTC LSB error in the DTC fine full-scale. Horizontal axis normalized to the target output frequency. DFC with $N = 12$, $N_{\mathrm{DTC}} = 11$, $FCW = 1792$.

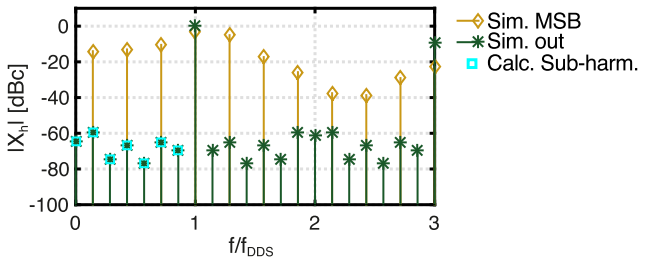

Fig. 13. Output spectrum with DTC impairments. Same parameters as Fig. 12, plus 3 DTC LSB mismatch between the full-scales of the two interleaved DTCs.

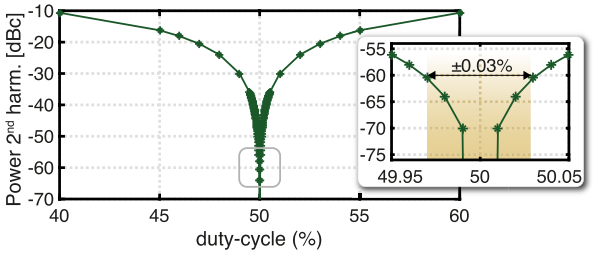

Fig. 14. Power of the second harmonic vs duty-cycle.

where $\tau_{\mathrm{FS\,fine}}$ is the fine delay full-scale. By applying the definition of the quantization error [15], [27] it is:

$$q_{\mathrm{eFS}}[l] = (-1)^l \left\{ DW_{\mathrm{coarse}}[l] + DW_{\mathrm{fine}}[l] \frac{\tau_{\mathrm{FS\,fine}}}{T_{\mathrm{CK}}/4} - DW_{\mathrm{ideal}}[l] \right\} \quad (26)$$

4) Full-Scale Mismatches DTCs (R and F): If there is a mismatch between the two interleaved DTCs R and F, the fine full-scale delay $\tau_{\mathrm{FS\,fine}}$ in (26) changes depending on the DTC involved, thus becoming a function of the index l. Therefore (26) still applies, with $\tau_{\mathrm{FS\,fine}}$ replaced with $\tau_{\mathrm{FS\,fine}}[l]$. This latter variable corresponds to the full scale of the DTC R or F, depending on the parity of the index l.

The complete equation for the quantization error when all the aforementioned sources of errors are considered is:

$$q_{\mathrm{e}}[l] = (-1)^l \left\{ DW_{\mathrm{coarse}}[l] + (DW_{\mathrm{fine}}[l] + \mathrm{INL}[l]) \frac{\tau_{\mathrm{FS\,fine}}[l]}{T_{\mathrm{CK}}/4} + EW_{CKph}[l] - DW_{\mathrm{ideal}}[l] \right\} \quad (27)$$

As an example, Fig. 12 shows the spectrum in dBc, resulting from behavioral simulations of the proposed system, when errors in the categories 1), 2), 3) have been inserted in the DTC model. In this example, we chose realistic error values of a few LSB, according to the state-of-the-art DTCs [25], [26], [55] The horizontal axis is normalized to the target output frequency. The simulated spectrum of signal MSB before the DTC correction is in yellow, the output spectrum is shown in dark green, and the calculated sub-harmonics with (13), (14) and (27) are shown as light-blue squares. Errors of a few LSBs in the categories 1), 2), 3) produce similar effects on the output spurs. They do not affect the half-wave symmetry of $q_{\mathrm{e}}[l]$. Therefore the fractional spurs are still placed at odd multiples of $(f_{\mathrm{CK}}/GRR)/f_{\mathrm{DDS}}$ only, but with higher strength compared to Fig. 9, where only the DTC quantization was considered. The spectrum in Fig. 12 has $-60\,\mathrm{dB}$ SFDR for a $11-$bit DTC, which is 13 dB worse than Fig. 9. The calculated sub-harmonics agree with simulation results within 0.02 dB. The sensitivity to errors of type 1) and 2) is the same, as the error weights in (22) and (23) are equal, while the error of type 3) is scaled by the nominal full-scale, as shown in (26).

The effect of errors of type 4) is different. Fig. 13 shows simulations with the same parameters of Fig. 12, plus an extra mismatch of a few DTC-LSBs between the full-scales of the two interleaved DTCs. The result is the presence of both a DC component, even signal harmonics, and extra fractional spurs at even multiples of $(f_{\mathrm{CK}}/GRR)/f_{\mathrm{DDS}}$. A mismatch changes the instantaneous output duty-cycle, thus breaking the half-wave symmetry of $q_{\mathrm{e}}[l]$ and giving rise to extra tones in the spectrum that are tracked by (14). The average duty-cycle determines the strength of the even harmonics. A $\pm 0.03\%$ deviation around 50% in the average duty-cycle keeps the second harmonic below $-60\,\mathrm{dBc}$, as shown in Fig. 14.

E. Worst Spur in Presence of INL

While errors of type 2), 3) and 4) listed above are closely related to the DTC implementation, an INL error will always be present, so it can be useful to describe the height of the maximum spur when the INL is the only DTC impairment, knowing the INL shape and maximum value INL_{max}.

The worst-case spur in (16) becomes:

$$\max_h \frac{|X_h|}{A/\pi} \approx \frac{2\pi}{GRR\,2^{N_{\mathrm{DTC}}}} \max_h \left| \sum_{l=1}^{L/2} \{ q_{\mathrm{e0}}[l] + (-1)^l \mathrm{INL}[l] \} \; e^{-j2\pi \frac{h}{L} l} \right| \quad (28)$$

Following the same reasoning of section IV-B, $\mathrm{INL}[l]$ can be considered a random variable $\tilde{\mathrm{INL}}$ and approximated with the expected value $E\left\{\left|\tilde{\mathrm{INL}}\right|\right\}$. Actually INL is a function of DW, and the sequence $DW[l]$ is dependent of the choice of the input word FCW. Therefore, for a generic FCW, we can consider DW a uniform random variable between 0 and $2^{N_{\mathrm{DTC}}-2}$ (the number of levels of the fine DTC, that has $(N_{\mathrm{DTC}} - 2)$ bits), and we can calculate the expected value as detailed in Appendix C.

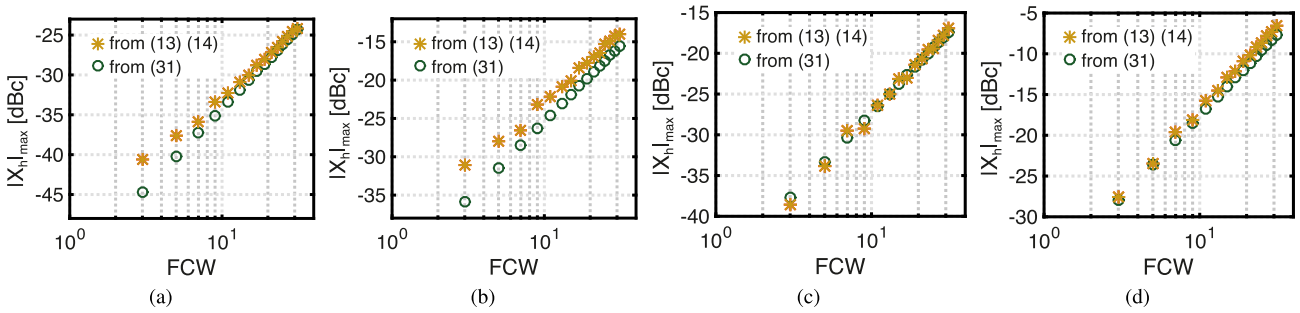

Fig. 15. Magnitude of the worst-case spur from (13) and (14), and approximation (31), for $N = 6$, $N_{\mathrm{DTC}} = 5$. Both plotted against odd values of FCW, in presence of (a) parabolic INL with $INL_{\max} = 3\,\mathrm{LSB}$, (b) parabolic INL with $INL_{\max} = 10\,\mathrm{LSB}$, (c) cubic INL with $INL_{\max} = 3\,\mathrm{LSB}$, and (d) cubic INL with $INL_{\max} = 10\,\mathrm{LSB}$.

Thus, the right-hand side of (28) can be approximated as

$$E\{|\tilde{q}_{e0}|\}\max_h\left|\sum_{l=1}^{L/2}e^{-j2\pi\frac{h}{L}l}\right| + E\left\{\left|\tilde{\mathrm{INL}}\right|\right\}\max_h\left|\sum_{l=1}^{L/2}(-1)^l e^{-j2\pi\frac{h}{L}l}\right| \quad (29)$$

where $E\left\{\left|\tilde{\mathrm{INL}}\right|\right\}$ depends on the shape of INL. Detailed steps for its calculation can be found in Appendix C, where the main results for parabolic and cubic INL shapes are:

$$E\{|\mathrm{INL}[l]|\} = \begin{cases} \dfrac{INL_{\max}}{4} & \text{parabolic} \\ \dfrac{INL_{\max}}{2\left(3-\sqrt{5}\right)} & \text{cubic} \end{cases} \quad (30)$$

Therefore, combining (28)-(30) with (18), it is

$$\max_h\frac{|X_h|}{A/\pi} \approx \frac{1}{2^N\,2^{N_{\mathrm{DTC}}}}FCW\,(1+\zeta\,INL_{\max}) \quad (31)$$

With $\zeta = 1$ for a parabolic INL shape and $\zeta = 2/\left(3-\sqrt{5}\right) \approx 2.6$ for a cubic INL shape.

Fig. 15 compares the maximum spur (in dBc) resulting from the analytical expressions (13) and (14) with the approximation (31), for both INL shapes, parabolic and cubic, with $INL_{\max} = 3\,\mathrm{LSB}$ and $INL_{\max} = 10\,\mathrm{LSB}$. The same number of bits as Fig. 10, $N = 6$ and $N_{\mathrm{DTC}} = 5$ has been chosen, for comparison purposes. The plots show the maximum spur as function of odd FCW, so that $\mathrm{GCD}\left(2^N, FCW\right) = 1$. In Fig. 15a, the maximum error is 4 dB at $FCW = 3$, which decreases to 0.2 dB at the maximum input word $FCW = 31$. Similar errors have been observed for different values of N and N_{DTC}. The approximation (31) is less accurate for a stronger non-linearity as shown in Fig. 15b. In this case, the maximum error between simulation and fitting is 4.72 dB at $FCW = 3$, and 1.62 dB at $FCW = 31$. In Fig. 15c, the maximum error is 1.1 dB at $FCW = 9$, while in Fig. 15d, the maximum error is 1.1 dB at $FCW = 31$.

Summarizing, (31) provides a simple equation for a crude estimate of the worst-case spur, while (13) and (14) can be used if a more accurate estimate is needed. The increase of 6 dB/octave of the worst-case spur with FCW is still valid in the presence of INL. The approximation of the maximum spur in (29) can be applied for every INL pattern, the shape factor being determined by $E\left\{\left|\tilde{\mathrm{INL}}\right|\right\}$, that can be calculated as shown in Appendix C.

V. Conclusion

In this paper we proposed an architecture of a Pulse-Output DFC generating square waves, with a deterministic DTC-based correction scheme to push down the spurs in the output spectrum. We discussed the design features of a DTC suitable for this application, and developed a behavioral model of the system to find the main bottlenecks that limit the output SFDR. The results depend exclusively on the ratio between the output frequency and the clock frequency and on the DTC features (number of bits, INL and other impairments). Simulations indicate that 60 dB clean spectrum is possible (Fig. 13), with a 12–bit counter, 11–bit DTC and realistic timing errors of a few LSBs added inside the DTC model, and without resorting to orthogonal techniques for further spur reduction. Compared to existing DFC systems, that rely on dithering or $\Delta\Sigma$ techniques, the advantage of the proposed Pulse-Output DFC in terms of maximum spur goes from 5 dB [29] to 12 dB [24]. The spur performance is comparable or better also in comparison to DPC architectures, while it features linear frequency control.

The quantization error of the DTC directly affects the spur amplitude. An approximation for the worst-case spur can be determined for the case of an ideal DTC limited only by quantization noise, given the number of bits of the DTC and the frequency input word. The DTC INL can also be taken into account, knowing the INL shape and the maximum INL value, leading to a simple design equation that allows to derive DTC INL requirements given a SFDR target. The maximum spur strength, in dBc, increases with the frequency control word by 6 dB per octave.

Appendix A
Derivation of (13) and (14)

Following similar steps as for the DPC in [15] and referring to Fig. 8, the ideal edge timing is:

$$t_{\mathrm{ideal}}[l] = \frac{l-1}{2}\,T_{\mathrm{DDS}} \quad (32)$$

With $l \geqslant 1$, rising edges for l odd, falling edges for l even. We can define the time-quantization error between corresponding edges of the real and ideal waveforms as:

$$\tau_{\mathrm{q}}[l] \triangleq t[l] - t_{\mathrm{ideal}}[l] \tag{33}$$

The signal $s(t)$ in Fig. 8 can be written as:

$$s(t) = A\left\{\sum_{\substack{l=1\\ l\ \mathrm{odd}}}^{L} u(t - t[l]) - \sum_{\substack{l=1\\ l\ \mathrm{even}}}^{L} u(t - t[l])\right\} \tag{34}$$

With $u(t)$ step function, A the signal amplitude and L defined in (10). Using (32) and (33), the Fourier transform of $s(t)$ is

$$S(f) = \frac{A}{j2\pi f}\left\{\sum_{\substack{l=1\\ l\ \mathrm{odd}}}^{L} e^{-j2\pi f\left(\tau_{\mathrm{q}}[l] + \frac{l-1}{2}T_{\mathrm{DDS}}\right)} - \sum_{\substack{l=1\\ l\ \mathrm{even}}}^{L} e^{-j2\pi f\left(\tau_{\mathrm{q}}[l] + \frac{l-1}{2}T_{\mathrm{DDS}}\right)}\right\} \tag{35}$$

The output is described by (11) and (12). The weights X_h can be calculated as [52]:

$$X_h = \frac{1}{GRR\ T_{\mathrm{CK}}} S\left(\frac{h}{GRR\ T_{\mathrm{CK}}}\right) \tag{36}$$

Combining (35) and (36) it is

$$X_h = \frac{A}{j2\pi h}\left\{\sum_{\substack{l=1\\ l\ \mathrm{odd}}}^{L} e^{-j2\pi\frac{h}{L}(l-1)} e^{-j2\pi\frac{h}{GRR\ T_{\mathrm{CK}}}\tau_{\mathrm{q}}[l]} - \sum_{\substack{l=1\\ l\ \mathrm{even}}}^{L} e^{-j2\pi\frac{h}{L}(l-1)} e^{-j2\pi\frac{h}{GRR\ T_{\mathrm{CK}}}\tau_{\mathrm{q}}[l]}\right\} \tag{37}$$

where the equality $GRR\ T_{\mathrm{CK}} = \frac{L}{2}T_{\mathrm{DDS}}$ has been used. By considering only the sub-harmonics ($h < L/2$) and being $\tau_{\mathrm{q}}/T_{\mathrm{CK}} << 1$ for all l, we can approximate the complex exponential:

$$e^{-j2\pi\frac{h}{GRR\ T_{\mathrm{CK}}}\tau_{\mathrm{q}}[l]} \approx 1 - j2\pi\frac{h}{GRR\ T_{\mathrm{CK}}}\tau_{\mathrm{q}}[l] \tag{38}$$

Therefore, (37) becomes

$$X_h \approx -\frac{A}{GRR\ T_{\mathrm{CK}}}\left\{\sum_{\substack{l=1\\ l\ \mathrm{odd}}}^{L} \tau_{\mathrm{q}}[l]\, e^{-j2\pi\frac{h}{L}(l-1)} - \sum_{\substack{l=1\\ l\ \mathrm{even}}}^{L} \tau_{\mathrm{q}}[l]\, e^{-j2\pi\frac{h}{L}(l-1)}\right\} \tag{39}$$

We can define the quantization error $q_e[l]$

$$q_e[l] \triangleq (-1)^{l+1}\frac{\tau_{\mathrm{q}}[l]}{\frac{T_{\mathrm{CK}}}{2^{N_{\mathrm{DTC}}}}} \tag{40}$$

Thus, (39) can be written as

$$X_h \approx -\frac{A}{GRR\ T_{\mathrm{CK}}}\frac{T_{\mathrm{CK}}}{2^{N_{\mathrm{DTC}}}}\left\{\sum_{l=1}^{L} q_e[l]\, e^{-j2\pi\frac{h}{L}(l-1)}\right\} \tag{41}$$

that is equivalent to (13) and (14).

APPENDIX B
PROOF OF THE APPROXIMATION IN (18)

We will prove (18):

$$\max_h \left|\sum_{l=1}^{L/2} e^{-j2\pi\frac{h}{L}l}\right| \approx \frac{L}{\pi} \tag{42}$$

We can rewrite the sum in (42) as

$$\sum_{l=0}^{L/2-1} e^{-j2\pi\frac{h}{L}(l+1)} = e^{-j2\pi\frac{h}{L}}\sum_{l=0}^{L/2-1} e^{-j2\pi\frac{h}{L}l} \tag{43}$$

From [56]

$$\sum_{l=0}^{L/2-1} e^{-j2\pi\frac{h}{L}l} = \frac{\sin\left(\frac{\pi h}{2}\right)}{\sin\left(\frac{\pi h}{L}\right)} e^{-j2\pi\frac{h}{L}\frac{L/2-1}{2}} \tag{44}$$

Therefore

$$\max_h \left|\sum_{l=1}^{L/2} e^{-j2\pi\frac{h}{L}l}\right| = \underbrace{\left|e^{-j2\pi\frac{h}{L}\frac{L/2-1}{2}}\right|}_{1} \max_h \left|\frac{\sin\left(\frac{\pi h}{2}\right)}{\sin\left(\frac{\pi h}{L}\right)}\right| \tag{45}$$

In the right-hand term of (45) the maximum value is obtained for the smallest odd value of h, i.e. $h = 1$:

$$\max_h \left|\frac{\sin\left(\frac{\pi h}{2}\right)}{\sin\left(\frac{\pi h}{L}\right)}\right| \overset{h=1}{=} \frac{1}{\left|\sin\left(\frac{\pi}{L}\right)\right|} \approx \frac{1}{\frac{\pi}{L}} = \frac{L}{\pi} \tag{46}$$

where the approximation of the sine with its argument is good for large L, i.e. all practical values of FCW. ■

We can also prove:

$$\max_h \left|\sum_{l=1}^{L/2} (-1)^l e^{-j2\pi\frac{h}{L}l}\right| \approx \frac{L}{\pi} \tag{47}$$

The sum in (47) can be written as:

$$\sum_{l=1}^{L/2} (-1)^l e^{-j2\pi\frac{h}{L}(l)} = (-1)\, e^{-j2\pi\frac{h}{L}}\sum_{l=0}^{L/2-1} (-1)^l e^{-j2\pi\frac{h}{L}l} \tag{48}$$

From [56]

$$\sum_{l=0}^{L/2-1} (-1)^l e^{-j2\pi\frac{h}{L}l} = \frac{1 + e^{-j\pi h}}{1 + e^{-j2\pi\frac{h}{L}}} \tag{49}$$

Therefore:

$$\max_h \left|\sum_{l=1}^{L/2} (-1)^l e^{-j2\pi\frac{h}{L}l}\right| = |-1|\underbrace{\left|e^{-j2\pi\frac{h}{L}}\right|}_{1} \max_h \left|\frac{1 + e^{-j\pi h}}{1 + e^{-j2\pi\frac{h}{L}}}\right| \tag{50}$$

The right-hand side of (50) is zero for h odd. The maximum value is obtained for the even value of h that is closest to $L/2$, i.e. $h = L/2 \mp 1$. Thus it is:

$$\begin{aligned}\max_h \left|\frac{1+e^{-j\pi h}}{1+e^{-j2\pi\frac{h}{L}}}\right| &\overset{h=\frac{L}{2}\mp 1}{=} \frac{2}{\left|1-e^{\pm j\frac{2\pi}{L}}\right|} \\ &= \frac{2}{\sqrt{2-2\cos\left(\pm\frac{2\pi}{L}\right)}} \\ &\approx \frac{2}{\sqrt{2-2\left(1-\frac{1}{2}\left(\frac{2\pi}{L}\right)^2\right)}} = \frac{2}{\frac{2\pi}{L}} = \frac{L}{\pi} \end{aligned} \tag{51}$$

where the Taylor expansion of the cosine $\cos(x) \approx 1 - \frac{x^2}{2}$ is good for all practical values of FCW. The proof of:

$$\max_h \left|\sum_{l=1}^{L/2} (-1)^{l+1} e^{-j2\pi\frac{h}{L}l}\right| \approx \frac{L}{\pi} \tag{52}$$

follows immediately, since

$$\left|\sum_{l=1}^{L/2} (-1)^{l+1} e^{-j2\pi\frac{h}{L}l}\right| = \left|\sum_{l=1}^{L/2} (-1)^{l} e^{-j2\pi\frac{h}{L}l}\right| \tag{53}$$

which leads back to (47). ■

Appendix C
Expected Value of INL

For a generic input frequency word FCW in a DFC with a block scheme like Fig. 7, we can consider DW a discrete uniform random variable $\tilde{DW}$ (assuming only integer values), with probability mass function (p.m.f.):

$$\xi_{DW}(DW) = \sum_{i=1}^{2^{N_{\mathrm{DTC}}-2}} \frac{1}{2^{N_{\mathrm{DTC}}-2}} \delta(DW - i) \tag{54}$$

where $N_{\mathrm{DTC}} - 2$ is the number of bits of each fine DTC. The INL is a function of $\tilde{DW}$, so its expected value $E\{|\mathrm{INL}(DW)|\}$ should be calculated using (54). To simplify calculations, for high enough N_{DTC}, $\tilde{DW}$ can be approximated as a continuous-type random variable, with uniform probability density function (p.d.f.):

$$\xi_{DW}(DW) \approx \begin{cases} \dfrac{1}{2^{N_{\mathrm{DTC}}-2}} & 0 \leqslant DW \leqslant 2^{N_{\mathrm{DTC}}-2} \\ 0 & \text{otherwise} \end{cases} \tag{55}$$

With $N_{\mathrm{DTC}} > 6$, by using (55) instead of (54), the error in the calculation of $E\{|\mathrm{INL}(DW)|\}$ is $< 1\%\,\mathrm{INL}_{\max}$.

The INL function should have mean value 0, since we are interested in the real error compared to the average delay: the result should be independent of delay offsets. A 0–mean parabolic INL with symmetry axis at $DW = 2^{N_{\mathrm{DTC}}-3}$ (Fig. 16) can be written as

$$\mathrm{INL}(DW) = DW\left(DW - 2^{N_{\mathrm{DTC}}-2}\right)\frac{\mathrm{INL}_{\max}}{\left(2^{N_{\mathrm{DTC}}-3}\right)^2} + \frac{2}{3}\mathrm{INL}_{\max} \tag{56}$$

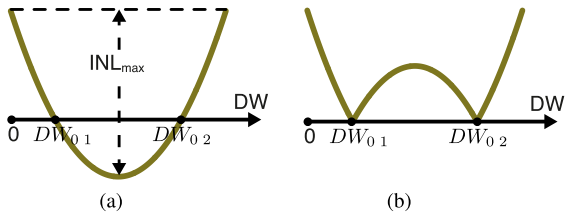

Fig. 16. Parabolic INL and its absolute value. (a) $\mathrm{INL}(DW)$. (b) $|\mathrm{INL}(DW)|$.

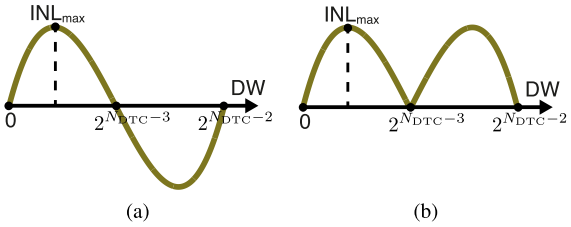

Fig. 17. Cubic INL and its absolute value. (a) $\mathrm{INL}(DW)$. (b) $|\mathrm{INL}(DW)|$.

Its roots are

$$DW_0 = \frac{3 \pm \sqrt{3}}{3}\, 2^{N_{\mathrm{DTC}}-3} \tag{57}$$

Therefore, from (56) and (5-55) in [57],

$$\begin{aligned} &E\{|\mathrm{INL}(DW)|\} \\ &= \frac{1}{2^{N_{\mathrm{DTC}}-2}} \int_0^{2^{N_{\mathrm{DTC}}-2}} |\mathrm{INL}(DW)|\, dDW \\ &= \mathrm{INL}_{\max}\left\{\frac{1}{3}\left[2\left(\frac{3-\sqrt{3}}{3}\right)^3 - 1\right] - \left[2\left(\frac{3-\sqrt{3}}{3}\right)^2 - 1\right]\right. \\ &\quad \left. + \frac{2}{3}\left[2\frac{3-\sqrt{3}}{3} - 1\right]\right\} \approx \frac{\mathrm{INL}_{\max}}{4} \end{aligned} \tag{58}$$

The same steps can be followed for a generic function $\mathrm{INL}(DW)$. The cubic function in Fig. 17 has the expression:

$$\mathrm{INL}(DW) = DW\left(DW - 2^{N_{\mathrm{DTC}}-3}\right)\left(DW - 2^{N_{\mathrm{DTC}}-2}\right) \times \frac{\mathrm{INL}_{\max}}{\frac{3-\sqrt{5}}{2}\left(2^{N_{\mathrm{DTC}}-3}\right)^3} \tag{59}$$

Thus

$$\begin{aligned} &E\{|\mathrm{INL}(DW)|\} \\ &= \frac{1}{2^{N_{\mathrm{DTC}}-2}} \int_0^{2^{N_{\mathrm{DTC}}-2}} |\mathrm{INL}(DW)|\, dDW \\ &= \frac{1}{2^{N_{\mathrm{DTC}}-2}} \frac{\mathrm{INL}_{\max}}{\frac{3-\sqrt{5}}{2}\left(2^{N_{\mathrm{DTC}}-3}\right)^3} 2\left[\int_0^{2^{N_{\mathrm{DTC}}-3}} \mathrm{INL}(DW)\, dDW\right] \\ &= \frac{\mathrm{INL}_{\max}}{2\left(3-\sqrt{5}\right)} \end{aligned} \tag{60}$$

REFERENCES

[1] F. Maloberti, *Data Converters*, 1st ed. Springer, 2007.

[2] M. J. M. Pelgrom, *Analog-to-Digital Conversion*, 3rd ed. Cham, Switzerland: Springer, 2017. [Online]. Available: https://www.springer.com/gp/book/9783319449708

[3] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[4] H. Darabi, *Integration of Passive RF Front End Components in SoCs*, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 2013.

[5] H. J. Visser, *Array and Phased Array Antenna Basics*. Hoboken, NJ, USA: Wiley, 2005.

[6] M. Kihara, S. Ono, and P. Eskelinen, *Digital Clocks for Synchronization and Communications*. Norwood, MA, USA: Artech House, 2002.

[7] T.-H. Lin, C.-C. Chi, W.-H. Chiu, and Y.-H. Huang, "A synchronous 50% duty-cycle clock generator in 0.35-μm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 585–591, Apr. 2011.

[8] C. Shi and E. Sánchez-Sinencio, "On-chip two-tone synthesizer based on a mixing-FIR architecture," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2105–2116, Aug. 2017.

[9] M. C. M. Soer, E. A. M. Klumperink, D.-J. Van D. Broek, B. Nauta, and F. E. Van Vliet, "Beamformer with constant-Gm vector modulators and its spatial intermodulation distortion," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 735–746, Mar. 2017.

[10] F. M. Gardner, *Phaselock Techniques*, 3rd ed. Hoboken, NJ, USA: Wiley, 2005.

[11] J. Vankka and K. A. I. Halonen, *Direct Digital Synthesizers: Theory, Design and Applications*, 1st ed. New York, NY, USA: Springer, 2001.

[12] R. Vishnu and S. S. Anulal, "An avoidance technique for mitigating the integer boundary spur problem in a DDS-PLL hybrid frequency synthesizer," in *Proc. Int. Conf. Commun. Signal Process. (ICCSP)*, Apr. 2015, pp. 443–446.

[13] S. Biswas and V. Revathi, "A fast-switching low-spurious 6–18 GHz hybrid frequency synthesizer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dec. 2015, pp. 312–315.

[14] P. P. Sotiriadis and K. Galanopoulos, "Direct all-digital frequency synthesis techniques, spurs suppression, and deterministic jitter correction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 958–968, May 2012.

[15] S. A. Talwalkar, "Quantization error spectra structure of a DTC synthesizer via the DFT axis scaling property," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 6, pp. 1242–1250, Jun. 2012.

[16] Analog Device. *A Technical Tutorial on Digital Signal Synthesis*. Accessed: May 16, 2019. [Online]. Available: https://www.analog.com/media/cn/training-seminars/tutorials/450968421DDS_Tutorial_rev12-2-99.pdf

[17] A. F. Molisch, *Wireless Communication*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.

[18] A. M. Fahim, *Clock Generators for SoC Processors: Circuits and Architectures*. New York, NY, USA: Springer, 2005.

[19] F.-W. Kuo *et al.*, "An all-digital PLL for cellular mobile phones in 28-nm CMOS with -55 dBc fractional and -91 dBc reference spurs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 3756–3768, Nov. 2018.

[20] C.-W. Yao *et al.*, "A 14 nm fractional-N digital PLL with 0.14ps$_{rms}$ jitter and -78 dBc fractional spur for cellular RFICs," in *ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 422–423.

[21] C.-R. Ho and M. S.-W. Chen, "A fractional-N digital PLL with background-dither-noise-cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spurs in 65 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 394–396.

[22] B. W. Garlepp *et al.*, "A portable digital DLL for high-speed CMOS interface circuits," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 632–644, May 1999.

[23] D. de Caro *et al.*, "A 3.3 GHz spread-spectrum clock generator supporting discontinuous frequency modulations in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2074–2089, Sep. 2015.

[24] S. Talwalkar, T. Gradishar, B. Stengel, G. Cafaro, and G. Nagaraj, "Controlled dither in 90 nm digital to time conversion based direct digital synthesizer for spur mitigation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2010, pp. 549–552.

[25] S. Sievert *et al.*, "2.9 A 2 GHz 244 fs-resolution 1.2 ps-Peak-INL edge-interpolator-based digital-to-time converter in 28 nm CMOS," in *ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 52–54.

[26] H. Jiang *et al.*, "A 12-bit 2.5 GHz 0.37ps-Peak-INL digital-to-time converter with parasitic-insensitive charge-based phase interpolator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[27] P. P. Sotiriadis, "Exact spectrum and time-domain output of flying-adder frequency synthesizers," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 57, no. 9, pp. 1926–1935, Sep. 2010.

[28] S. A. Talwalkar, "Digital-to-time synthesizers: separating delay line error spurs and quantization error spurs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 10, pp. 2597–2605, Oct. 2013.

[29] A. Elkholy, S. Saxena, G. Shu, A. Elshazly, and P. K. Hanumolu, "Low-jitter multi-output all-digital clock generator using DTC-based open loop fractional dividers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1806–1817, Jun. 2018.

[30] L. Dartois, A. Roullet, and R. Riboni, "High frequency digital synthesizer with aperiodic correction optimizing the spectral purity," U.S. Patent 4 792 914 A Dec. 20, 1998.

[31] H. Mair and L. Xiu, "An architecture of high-performance frequency and phase synthesis," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 835–846, Jun. 2000.

[32] D. E. Bockelman, "Direct digital synthesizer based on delay line with sorted taps," U.S. Patent 6 510 191 B2, Jan. 21, 2003.

[33] T. Rapinoja *et al.*, "A digital frequency synthesizer for cognitive radio spectrum sensing applications," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1339–1348, May 2010.

[34] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Trans. Audio Electroacoust.*, vol. 19, no. 1, pp. 48–57, Mar. 1971.

[35] C. E. Wheatley, III, and D. E. Phillips, "Spurious suppression in direct digital synthesizers," in *Proc. 35th Annu. Freq. Control Symp.*, May 1981, pp. 428–435.

[36] E. McCune, "Time-filtered squarewave output from direct digital synthesis," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 996–999.

[37] H. Nosaka, Y. Yamaguchi, A. Yamagishi, H. Fukuyama, and M. Muraguchi, "A low-power direct digital synthesizer using a self-adjusting phase-interpolation technique," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1281–1285, Aug. 2001.

[38] E. W. McCune, Jr., "Digital frequency synthesizer and method with Vernier interpolation," U.S. Patent 5 247 469 A, Sep. 21, 1993.

[39] T. Finateu *et al.*, "A 500-MHz $\Sigma\Delta$ phase-interpolation direct digital synthesizer," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 452–455.

[40] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.

[41] N. Markulic, K. Raczkowski, P. Wambacq, and J. Craninckx, "A 10-bit, 550-fs step digital-to-time converter in 28 nm CMOS," in *Proc. ESSCIRC*, Sep. 2014, pp. 79–82.

[42] N. Markulic *et al.*, "A DTC-based subsampling PLL capable of self-calibrated fractional synthesis and two-point modulation," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3078–3092, Dec. 2016.

[43] M.-S. Yuan, C.-C. Li, C.-C. Liao, Y.-T. Lin, C.-H. Chang, and R. B. Staszewski, "A 0.45 V sub-mW all-digital PLL in 16 nm FinFET for bluetooth low-energy (BLE) modulation and instantaneous channel hopping using 32.768 kHz reference," in *ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 448–450.

[44] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, Jun. 2015.

[45] G. D. Skingle, "Frequency synthesiser," U.S. Patent 3 772 681, Nov. 13, 1973. [Online]. Available: https://patents.google.com/patent/US3772681

[46] C. E. Wheatley, III, "Digital frequency synthesizer with random jittering for reducing discrete spectral spurs," U.S. Patent 4 410 954 A, Oct. 18, 1983.

[47] H. Nosaka, T. Nakagawa, and A. Yamagishi, "A phase interpolation direct digital synthesizer with a digitally controlled delay generator," in *Proc. Symp. VLSI Circuits*, Jun. 1997, pp. 75–76.

[48] A. Yamagishi, H. Nosaka, M. Muraguchi, and T. Tsukahara, "A phase-interpolation direct digital synthesizer with an adaptive integrator," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 6, pp. 905–909, Jun. 2000.

[49] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N^2," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec. 2009.

[50] X. Gao *et al.*, "A 2.7-to-4.3 GHz, 0.16ps_{rms}-jitter, -246.8dB-FOM, digital fractional-N sampling PLL in 28nm CMOS," in *ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 174–175.

[51] X. Gao, E. A. M. Klumperink, and B. Nauta, "Advantages of shift registers over DLLs for flexible low jitter multiphase clock generation," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 55, no. 3, pp. 244–248, Mar. 2008.
[52] S. S. Soliman and M. D. Srinath, *Continuous and Discrete Signals and Systems*, 2nd ed. London, U.K.: Pearson.
[53] W. L. Briggs and V. E. Henson, *The DFT: An Owners' Manual for the Discrete Fourier Transform*. Philadelphia, PA, USA: SIAM, 1987.
[54] A. Elmallah, M. G. Ahmed, A. Elkholy, W.-S. Choi, and P. K. Hanumolu, "A 1.6ps peak-INL 5.3ns range two-step digital-to-time converter in 65nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[55] S. Sievert *et al.*, "A 2 GHz 244 fs-resolution 1.2 ps-peak-INL edge interpolator-based digital-to-time converter in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2992–3004, Dec. 2016.
[56] E. W. Weisstein. *Exponential Sum Formulas*. Accessed: May 16, 2019. [Online]. Available: http://mathworld.wolfram.com/ExponentialSumFormulas.html
[57] A. Papoulis and S. U. Pillai, *Probability, Random Variables, and Stochastic Processes*, 4th ed. New York, NY, USA: McGraw-Hill.

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