A Baseband-Matching-Resistor Noise-Canceling Receiver Architecture to Increase In-Band Linearity Achieving 175MHz TIA Bandwidth with a 3-Stage Inverter-Only OpAmp

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***Abstract*— In this paper we propose a baseband noise-canceling receiver architecture to increase in-band linearity. Key feature of the architecture is that all active circuits are in baseband, including the LNTA. The receiver targets high IF bandwidths, enabled by a TIA composed of an OpAmp using only inverters. The receiver is fabricated in 22nm FDSOI CMOS. Measured results show an in-band IIP3 of > 9dBm for an IF bandwidth of 175MHz with sub-5dB NF across 1-6GHz LO.**

***Keywords*— Base-station, in-band linearity, noise-canceling, wide-band IF, Inverters-only OpAmp, TIA, LNTA, IIP3**

I. Introduction

High in-band linearity has become important in many sub-10GHz CMOS receiver applications: 1) High in-band linearity is necessary in applications where the band of interest may contain many signals, such as in cognitive radio, base station applications [1] and intra-band carrier aggregation scenarios [2]. 2) Most self-interference cancellation techniques used for in-band full-duplex receivers involve significant cancellation in the digital domain [3]. Therefore RF and analog receiver front-ends need to be sufficiently linear for the success of such techniques. 3) MIMO applications involving beam-forming either in digital or combination of analog and digital domains need high in-band linearity [4].

Also, most of the above applications are increasingly targeting higher IF-bandwidths in order to fulfill higher data-rate requirements. For example, recent works on base-station receiver designs [5], [6] have targeted high IF-bandwidth to support all 3GPP bands.

Fig. 1 shows various mixer-first receiver architectures in the context of in-band linearity. The receiver in Fig. 1(a) [7] does not achieve high in-band linearity due to significant signal swing at the input of the TIA, and similar is the case for [8]. Even though [1] shown in Fig. 1(b) can achieve high in-band linearity, it is more noisy due to the dedicated 50Ω matching resistor. In the noise-canceling topology of Fig. 1(c) [9] , linearity is limited by the LNTA, which operates at RF frequencies. Fig. 1(d) [10] shows another way to increase in-band linearity, but due to its lack of input matching it is not practical in many applications.

We propose a noise-canceling receiver architecture where all active circuits work at baseband frequencies. It features high bandwidth, high in-band linearity, OoB filtering and good input matching. The coming sections discuss the architecture, the circuits and measurements on a prototype chip.

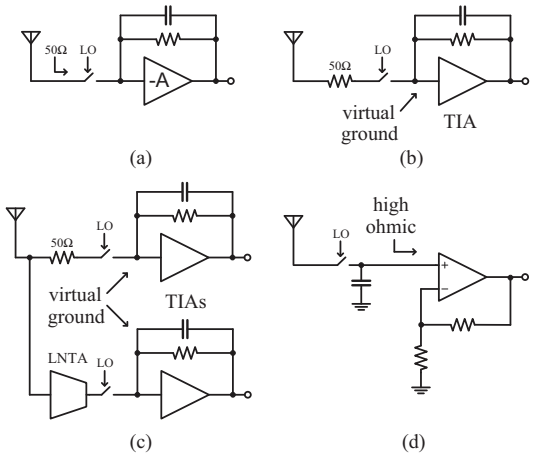


Fig. 1. Representative mixer-first receiver architectures (a) [7], (b) [1], (c) [9] , and (d) [10] for comparing their in-band linearity along with noise, matching, and OoB linearity performances

II. Architecture

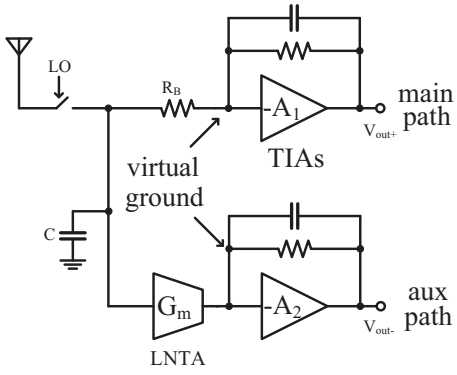


Fig. 2. Proposed baseband-matching-resistor noise-canceling receiver architecture

The proposed receiver is shown in Fig. 2. It is a noise-canceling architecture with the feature that all active circuits work at baseband frequencies. Input matching is

provided by R_B, whose impedance is frequency translated to the input by the passive mixer. An auxiliary path containing an LNTA with transconductance G_m cancels the noise of this resistor. Note that the N-path filter formed by the source impedance and the capacitor C rejects OoB interferers.

The proposed receiver architecture achieves higher in-band linearity mainly because of the virtual ground at the input of the TIAs and the LNTA operating in baseband. The virtual ground at the input of the TIAs not only reduces the swing at the input of the TIAs, but also allows the loop-gain to be > 1 unlike in the case of the architecture shown in Fig. 1 (a). Higher loop-gain further reduces the distortion produced in the TIAs.

Additionally, operating the LNTA in baseband enables the use of feedback to achieve the desired linearity. Feedback not only helps to improve the linearity of the LNTA, but also makes the linearity robust to PVT changes. Most RF LNTAs do not have this luxury, such that they dominate the overall non-linearity, with linearization techniques suffering from variation across PVT as explained in [11].

Since this noise-canceling architecture has the matching resistor and all noise-canceling circuits in baseband, we refer to this architecture as BaseBand Noise-Canceling (BBNC) in this paper.

III. Circuit design

The receiver targets multi-band and multi-channel applications with a bandwidth of more than 100MHz, requiring high in-band linearity and low noise over a wide range of LO frequencies.

A. Mixer and LNTA

The circuit in Fig. 2 is realized 4 times sharing one differential antenna input, providing quasi differential I and Q paths, with the passive mixer switches operating at 25% duty cycle. The passive mixer switch sizes are chosen such that they have small on-resistance to minimize noise which cannot be canceled. The N-path filter capacitors C are 2pF each. Fig. 3(a) shows the LNTA. The value of R_{LNTA} must be chosen low enough to limit their noise contribution, while $(g_{Mp}+g_{Mn})\cdot R_{LNTA}$ must be sufficiently high to achieve the required in-band IIP3. This requires large transistor sizes. In [9], where the LNTA operates at RF, larger input transistors would degrade input matching. However, in the proposed architecture, large transistor sizes only (slightly) affect the bandwidth of the N-path filter formed by the source resistance, mixer switches and effective capacitor C shown in Fig. 2. The bias voltages are set by the replica bias circuit in Fig. 3(b), which keeps the dc output voltage of the LNTA near mid-supply. This is also the input dc voltage of the TIA to which the LNTA output is connected.

B. TIA

Designing for a wide IF-bandwidth in mixer-first receivers boils down to the design of a wide-band TIA. The TIA OpAmp is realized with only inverters as gain stages. This avoids unnecessary internal nodes such that the bandwidth can be high. It also offers other advantages like current re-use and rail-to-rail output swing [12],[13].

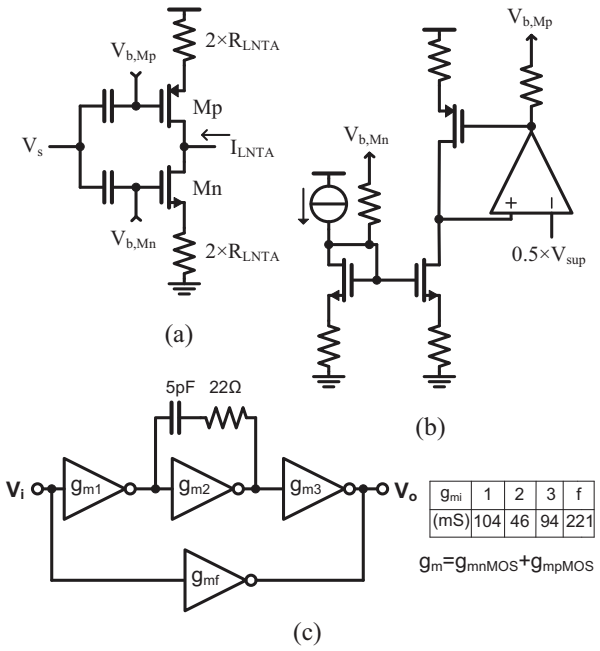


Fig. 3. (a) LNTA schematic, (b) its biasing circuit, and (c) 3-stage inverter-only OpAmp architecture

Fig. 3(c) shows the 3-stage inverter-only OpAmp designed for a UGB of 6GHz. It consists of three cascaded inverters in the main path and a feed-forward inverter path. The main path gives sufficient gain till 175MHz to achieve the required linearity. A combination of Miller compensation with right half plane zero removal and a high frequency feed-forward inverter path stabilizes the OpAmp. Note that the circuit parameters mentioned in Fig. 3(c) are for the OpAmp -A_2 of Fig. 2. For OpAmp -A_1, the corresponding values are scaled to obtain the required loop-gain.

The high loop gain of the OpAmps leads to a good virtual ground at the input, which reduces the input voltage swing, improving linearity. Also distortion caused by output voltage swing V_{out} is reduced by the high loop gain.

Note that common mode control is not necessary, since the OpAmps work independently and there is no coupling between any of the I/Q/+/-/main/aux paths.

IV. Experimental results

The receiver was realized on chip in a 22nm FDSOI CMOS process. The active chip area is $0.48mm^2$ and it works at a supply voltage of 0.83V. Placement of the various receiver blocks in the chip is shown in Fig. 4. Mixer switches are placed near to the bond-pad so that RF routing is minimal. The four capacitors are placed near the mixer switches to provide short return paths for the high frequency currents. The clk block consists of a $\div 2$ circuit and a 4-phase 25% duty-cycle generation circuit.

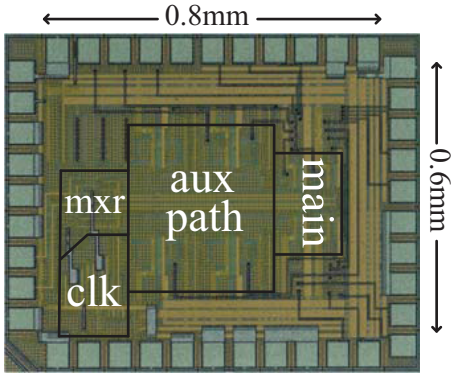


Fig. 4. Chip photo showing various receiver blocks

A. Test Setup

Fig. 5 shows the test setup used to measure the receiver. The measurements were performed with a single-ended source, followed by a passive balun driving the receiver. The differential output voltage is measured by an active differential probe. On-chip common-source amplifiers and all-pass voltage attenuator circuits are used at the output to measure NF and IIP3 respectively such that noise and distortion of the active differential probe do not dominate the respective measurements. The corresponding gain and attenuation were de-embedded. Although Fig. 5 shows circuits to measure NF of the I-path and IIP3 of the Q-path, the receiver has provisions to measure both NF and IIP3 of both the I and Q paths.

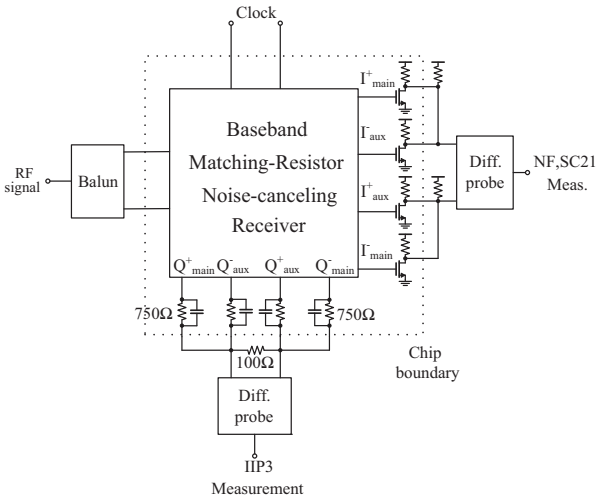
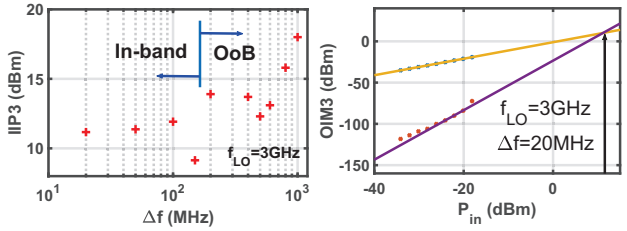


Fig. 5. Test setup to measure the receiver

B. Measurement Results

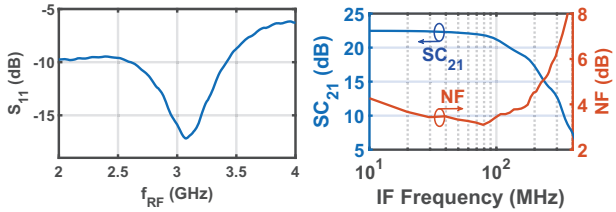
The bandwidth of the receiver is measured to be 175MHz. Fig. 6(a) shows the IIP3 measured using two-tone tests for both in-band and OoB. In case of in-band IIP3 measurement, two tones f_1 and f_2 are at $\Delta f - 2MHz$ and $\Delta f + 2MHz$ respectively. For the OoB IIP3 measurement, two tones f_1 and f_2 are at Δf and $2\Delta f - 50MHz$ such that the IM3 products are always at 50MHz. In-band IIP3 is >9dBm for all Δf within the TIA bandwidth.



(a) (b)

Fig. 6. Measured (a) IIP3 across interferer offset frequencies and (b) OIM3 at 20MHz offset

Fig. 6 (b) shows the measured IM3 curve for Δf=20MHz. This measurement shows that the IIP3 is valid till an input power of -20dBm. Fig. 7 (a) shows the measured S_{11} at 3GHz LO frequency. The N-path filtering action can be observed in the measured S_{11}. Fig. 7 (b) shows the measured noise figure and conversion gain (SC_{21}) across IF frequencies at 3GHz LO frequency. The $<$ 3dB NF at 80MHz confirms the noise-canceling properties of the circuit. This matches with the simulation which shows 2.75dB, compared to 7.4dB without the auxiliary (noise-canceling) path at same offset (80MHz) and LO (3GHz) frequencies.



(a) (b)

Fig. 7. Measured (a) S_{11} showing N-path filtering and (b) NF and SC_{21} at 3GHz LO

Fig. 8 shows the flexible nature of the receiver for multi-band and multi-channel operation. It shows the measured NF, SC_{21} and IIP3 at 50MHz offset and S_{11} across LO frequencies from 1-6GHz. Note that the large input capacitance of the LNTA does not degrade the S_{11} of the receiver, as explained in section III. NF and IIP3 stay around 3dB and 10dBm respectively for the measured LO sweep of 1-6GHz. Though the receiver is functional till 8GHz in extracted simulations, we measured it till 6GHz due to the frequency-limitation of the 2×LO source (12.75GHz) feeding the clk block.

C. Comparison

Table I lists in-band IIP3 and TIA bandwidth (along with other performance parameters) of state of the art receivers and compares it to our receiver performance. The proposed receiver has the highest IIP3 except for [6], which achieves a band-edge IIP3 of 12dBm, but this is after de-embedding the off-chip LNA, which is reflected in the higher noise figure

Table 1. Result summary and comparison with prior art

	This Work	JSSC16[2]	JSSC12[9]	JSSC18[8]	ISSCC16[5]	ISSCC18[6]
Architecture	BBNC	Mixer-first	FTNC	Mixer-first	ZIF RX	ZIF RX
Technology	22FDX	28nm	40nm	45nm SOI	45nm	65nm
In-band IIP3 (dBm)	9	7 *	-3 ‡	-10 ‡	-4 ‡	12 †‡
IF bandwidth (MHz)	175	50	2	10	50	100
f_{RF} (GHz)	1-6	0.4-3.5	0.08-2.7	0.2-8	0.4-4	0.4-6
NF (dB)	2.5-5	2.4-2.6	1.9	2.3-5.4	2	12
Power (mW)	172	38-75	35.1-78	$50+30\times f_{LO}$ ◇	200	6600 **
Area (mm^2)	0.48	0.23	1.2	0.8	49 **	68.7 **

* Measured for 20MHz bandwidth, baseband supply = 1.5V
† De-embedding off-chip LNA
◇ mW/GHz
‡ taken from band-edge IIP3
** Full SOC

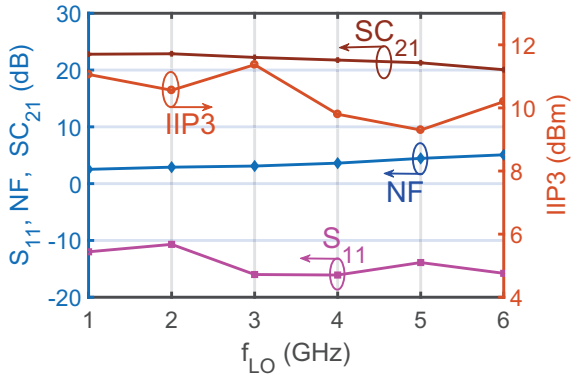


Fig. 8. Measured S_{11}, NF, SC_{21}, and IIP3 across LO frequencies

of 12dB. [2] reports an in-band IIP3 of 7dBm, however this is measured for a TIA bandwidth of 20MHz and uses a dual analog supply with a higher 1.5V supply for the baseband circuits. Our bandwidth also compares favourably to other work. We mainly target base-station applications and our power numbers are lower compared to [5] and [6] which target the same application.

V. Conclusion

The proposed receiver can achieve high in-band linearity over a wide RF frequency range of 1-6GHz. This is mainly because all active circuits operate in baseband and can be designed using feedback, both the LNTA and the TIA. Due to the noise-canceling properties, input matching is good with low NF. An inverter-only multi-stage OpAmp enables the wide IF bandwidth of 175MHz.

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