Channel Profile Engineering of 0.1μm-Si MOSFETs by Through-the-Gate Implantation

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Abstract

A novel approach to the SSR channel profile formation for MOSFETs is suggested, with dopant implantation in the late stages of the processing, with the gate, source/drain already in place ("TGi"). Only a single damage/activation anneal and the back-end thermal budget are experienced by the implanted dopants, which results in steep profiles even when light boron ions are used. High-performance NMOS devices with excellent SCE control designed for low-voltage digital, analog and RF operation were realized using this technique. For PMOS the use of TGi is restricted by significant diffusion of source/drain extensions due to the TGi damage induced TED.

Introduction

For MOS devices scaled to deep submicron dimensions, the use of super-steep retrograde doping profiles (SSR) can significantly improve short channel effects (SCE) and deliver increased current drivability [1,2]. The effectiveness of such profiling depends on its steepness (the ideal being a "step"-like shape). Implantations of heavy arsenic ions have been widely used to form SSR for PMOS transistors (e.g. [3]) while for NMOSTs there seems to be no comparable candidate. The traditionally used boron ions are prone to strong TED and OED, with any consecutive implantation or oxidation step resulting in washing out of the original SSR profile. Indium ions are heavy, but they have a low level of electrical activation and have been shown to exhibit TED comparable to boron [4]. Additionally, lateral re-distribution and de-activation (of B and In, respectively) during processing results in strong reverse SCE and anomalous SCE [5]. Here, we demonstrate a novel approach to the SSR formation, with the implantation performed as the last step in the formation of the active part of the device, with the gate, source/drain already in place (Through-the-Gate implantation, "TGi"). The only thermal budget experienced by the SSR in this case is a single damage/activation anneal and the back-end processing. We have studied application of this technique for both NMOS and PMOS devices. We show here, for the first time, that TGi can be successfully implemented to form a *boron* SSR profile. High-performance NMOS devices with excellent SCE control designed for low-voltage digital, analog and RF operation were realized using this technique. For PMOS TGi results in significant diffusion of source/drain extensions due to TED induced by the TGi damage.

Experimental

The dual-flavor CMOS process features: L_g down to 0.07μm (e-beam), t_{ox} in the range 3.2-5.5nm (C-V), low-energy boron/arsenic implants and tilted pocket implants combined with short RTP anneals to form shallow source/drain junctions. For NMOS, boron was implanted through the nominally 150nm-thick gate to form the SSR (see figure **1**). For PMOS arsenic or phosphor were studied. RTA of 20s at 1030°C was applied to anneal the TGi implantation damage and activate dopants in the channel. The devices were targeted for operation at 1.2V, so the V_T values have been chosen to be 100mV (digital "low-V_T") and 300mV ("analog/RF -V_T") lower than in the 1.5V reference technology ("High-V_T" = 0.4V).

Results and Discussion

Figure **2(a)** shows the comparison between the channel profiles (SIMS measurements) of the completed reference

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NMOS devices (with boron channel implants before the gate oxidation) and devices with TGi profiles. The latter provide an excellent SSR shape even if compared against indium profiles. Ion mixing of Si and O during the TGi does not result in gate oxide quality degradation for low doses of B [7] which is confirmed in figures **3(a)** and **(b)** in which the results of E_{bd} and Q_{bd} measurements are shown for two gate oxide thicknesses. The SCE are significantly improved by the SSR profiling especially for low-V_T and analog-V_T devices (figures **4**, **5**); the use of TGi also removes the reverse SCE completely, since there are no implantation or oxidation steps afterwards. Figure **6** shows variations in the V_T across the wafers. It is clear that the spread of V_T is similar for all variants. A numerical sensitivity analysis shows that a 10% deviation in the dose (energy) of the TGi result in less than 5% (15%) V_T variations for a device with L_g =0.1μm. Representative transfer and output characteristics of the 0.11μm transistors with TGi boron profiles are compared to the reference device in figures **7** and **8**. It is remarkable that while TGi low-V_T devices have as good SCE immunity as reference devices (V_{DD} =1.5V) they also deliver almost the same current drive for supply voltage scaled to 1.2V (figure 8). The measured increase in the current drive and G_m^{sat} of the devices with SSR profiles originates from lower V_T and the increased mobility in the channel (see figure **9**).

Being self-aligned in nature (see figure **1**), the through-gate implanted SSR also gives rise to smaller drain junction capacitance (figure **10**), especially if compared to blanket fully activated In SSR. In the case of TGi, the peak concentration of the SSR profile is essentially shifted away from the surface by the poly-gate thickness, while it stays at the same depth as in the channel region should blanket SSR be used. The low values of parasitic capacitances are confirmed by excellent ring oscillator delay of 26ps/stage at 1.8V (figure **11**) for 0.18μm technology devices with TGi-NMOSTs that compares favorably to [6]. NMOS parameters for TGi and conventional devices are summarized in Table 1. Notably, while 0.11μm analog NMOST with reference channel profile operates in deep punch-through mode, the TGi analog device operates normally, showing that this devices are well-suited for low-voltage analog and RF applications.

For PMOS devices the TGi profiles are less steep (figure 12) than conventionally formed SSRs. It would still be advantageous to have a possibility to use TGi in view of parasitic capacitances reduction described above. Unfortunately, TGi induces significant boron source/drain TED when the TGi implantation damage is annealed (figure 13). To study the latter effect we have measured the dependence of boron source/drain diffusion under the gate on the dose of Si TGi damage and the RTA temperature in the range of interest. The results (figures 14) confirm that TED of S/D is large and also provide a good estimation of the TED effects on boron source/drain junctions in actual PMOS devices.

Conclusions

We have shown that Boron SSR channel profile can be achieved for NMOSTs by Through-the-Gate implantation resulting in improved SCE immunity, increased G_m^{sat} and current drive. No degradation of gate oxide quality, nor increase in transistor parameter variations were observed. In PMOS, the TGi, performed after the boron source and drain have been placed, results in significant source/drain diffusion due to TED induced by the implantation damage. Self-alignment of the implant with the gate results in low drain junction capacitance. We have shown that this simple technique has a significant manufacturing potential, especially for low-voltage and analog/RF CMOS applications.

Acknowledgements

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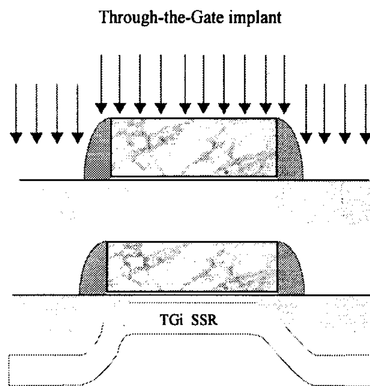

Figure 1 Processing sequence to form the Through-the-Gate implanted (TGi) Boron SSR profile. The profile endures only a single RTP step to anneal damage and activate dopants, and a back-end thermal budget.

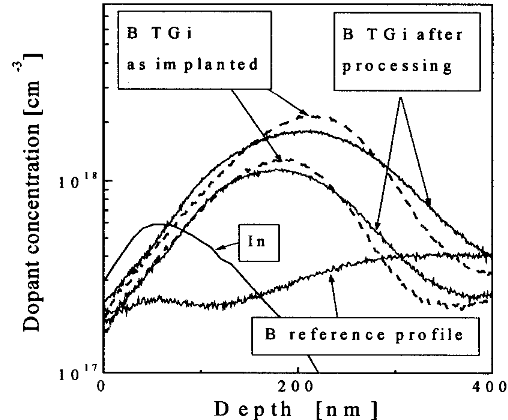

Figure 2 Boron SIMS profiles in the channel region for default and TGi SSR NMOST channel profiles (2.3e13cm^{-2} @100keV and 4e13cm^{-2}@110keV) as implanted and after the processing was completed. T_{gate}=150nm, t_{ox}=4.5nm. The indium (1.5e13@190keV) SIMS profile after complete processing is added for comparison (courtesy of S. Kubicek of IMEC).

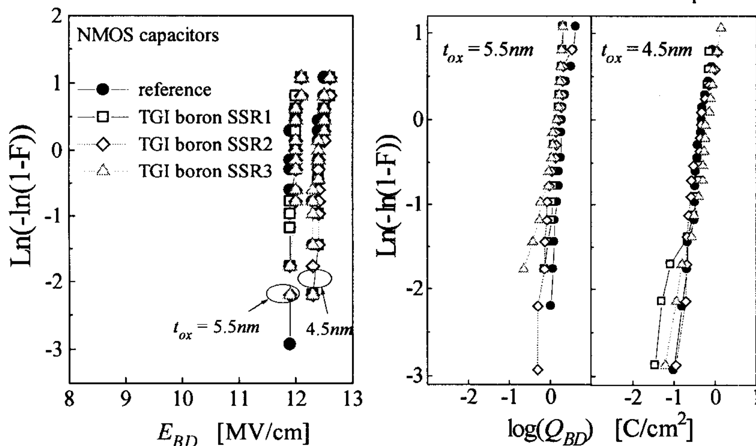

Figure 3 Weibull distributions of electric field at breakdown (**a**) and accumulated Q_{BD} (**b**), measured on 40 8×10^{-4}cm^2 NMOS capacitors with 5.5nm and 4.5nm gate oxides for various channel profiles. For all TGi boron implantations used there is no gate oxide degradation observed. TGi doses range: (1.2-4)e13cm^{-2}; energies range: (80-110)keV.

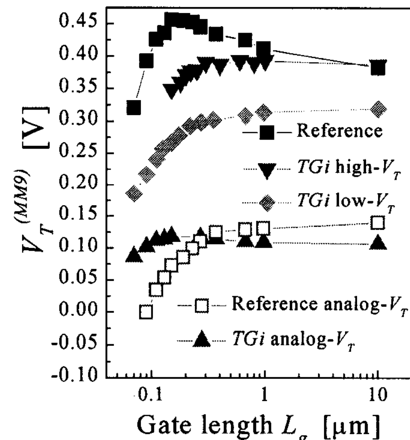

Figure 4 V_T for NMOSTs (determined using MOS MODEL9 extraction routines [8]) with reference and TGi channel profiles. Both type of devices also had tilted pocket implants for extra SCE control.

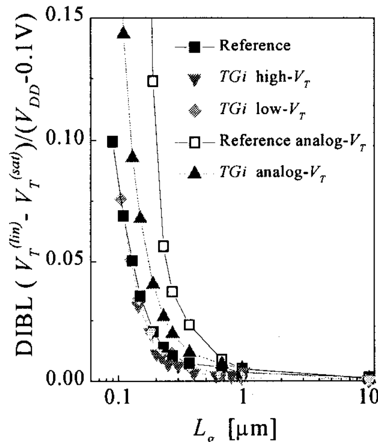

Figure 5 DIBL for NMOSTs with reference and TGi channel profiles. VDD was 1.5V "Reference" and "high-V_T" TGi variants and 1.2V for the rest.

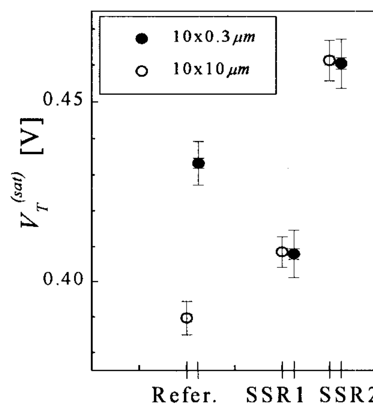

Figure 6 Saturation V_T variation for NMOSTs with reference and TGi channel profiles. T_{gate} is measured to vary between 140 - 155nm, t_{ox} was 4.5nm. TGi SSR profiles as in figure 1. The error bars indicate V_T spread over the wafer.

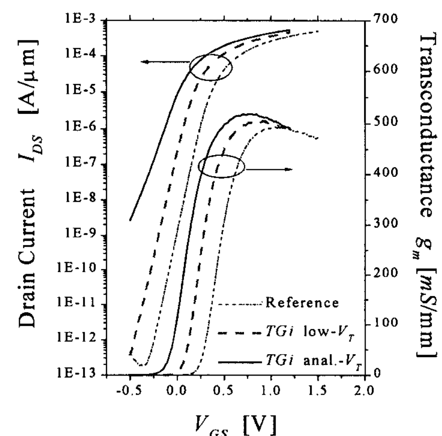

Figure 7 Typical sub-V_T characteristics and transconductance for reference and TGi NMOSTs with drawn L_g = 0.11μm, t_{ox}=3.2nm. V_{DS} was 1.2V for TGi and 1.5V for reference devices respectively.

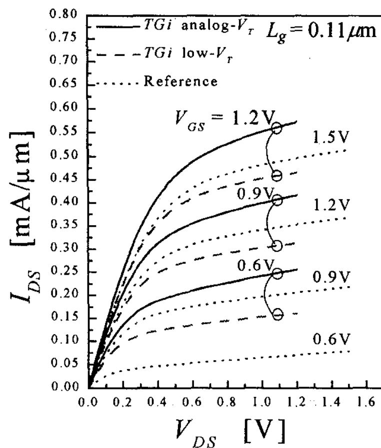

Figure 8 Output characteristics for Reference and TGi NMOSTs. V_{DD} was 1.5V "Reference" and 1.2V for the TGi variants.

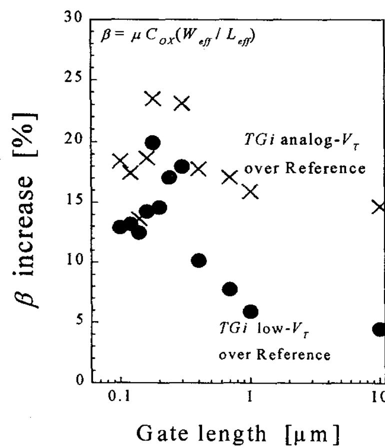

Figure 9 Electron mobility increase when TGi SSR profiling is used in place of Reference "flat". Gate oxide is 3.2 *nm*.

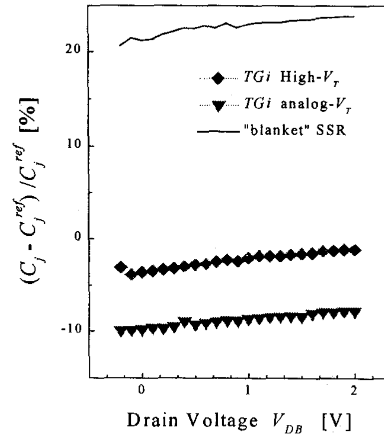

Figure 10 Measured junction capacitance. There is no C_J increase when TGi SSR is used, while for "blanket" SSR C_J is increased dramatically. C_J is significantly reduced for analog-V_T TGi devices.

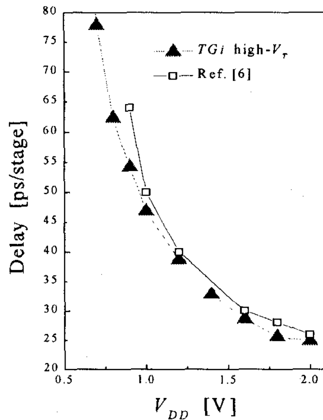

Figure 11 Unloaded 0.18μm CMOS ring oscillator gate delay with NMOS devices with TGi SSR compared to the values for reference technology from [6].

	Ref. High-V_T	**TGi High-V_T**	Ref. High-V_T	**TGi Low-V_T**	Ref. Analog-V_T	**TGi Analog-V_T**
L_g [μm]	0.18	**0.18**	0.11	**0.11**	0.11	**0.11**
V_{DD} [V]	1.5	**1.5**	1.2	**1.2**	1.2	**1.2**
V_T^{MM9} [V]	0.48	**0.36**	0.42	**0.24**	0.05	**0.11**
DIBL	0.020	**0.020**	0.090	**0.075**	>0.5*	**0.140**
I_{on} [mA/μm]	0.370	**0.440**	0.360	**0.460**	0.640*	**0.550**
I_{off} [A/μm]	1e-11	**5e-10**	1e-9	**1e-7**	1e-4*	**8e-6**
S^{sat} [mV/dec]	74	**76**	81	**83**	>150*	**107**
G_m^{sat} [mS/mm]	408	**430**	495	**512**	540*	**520**
C_j [nF/cm^2]	120	**119**	120	**117**	106	**110**

* - device operates in deep punch-through mode

Table 1 Summary of TGi and Reference technology performance values for devices with t_{ox} = 3.2 *nm*. Note a significant improvement in performance values for low-voltage and analog devices with TGi.

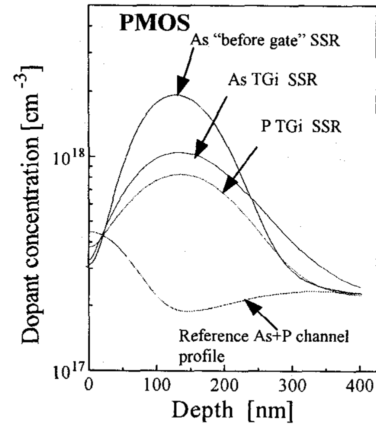

Figure 12 PMOST SSR profiles comparison as simulated to have the same V_T for all variants. The steepest profile is achieved using As implant before the gate deposition.

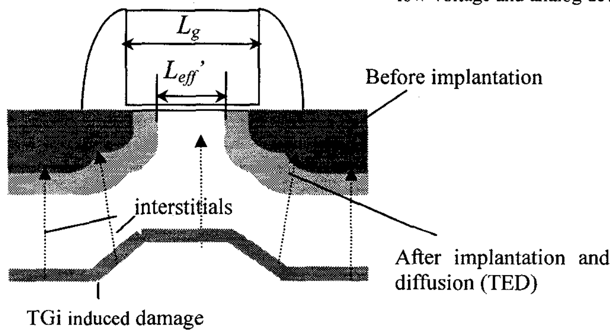

Figure 13 Effect of TGi on PMOST source/drain junctions: during an implantation anneal the damaged region in the bulk supplies interstitials which can significantly increase diffusion of the boron source/drain regions (TED), extending them under the gate. The amount of under-diffusion can be determined electrically using, e.g., MOS MODEL9 L_{eff} extraction procedure [8]. To measure the effect of varying dose and RTA temperature one has to ensure that the channel profile is unchanged – TGi of Si atoms can be used.

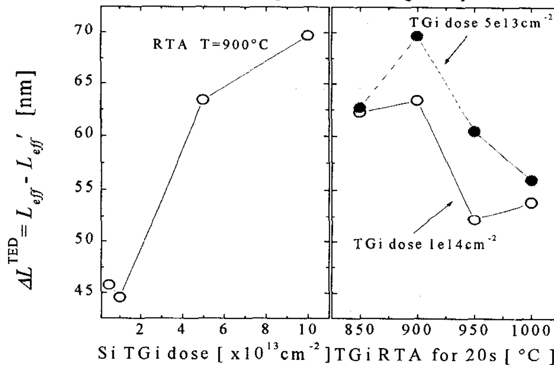

Figure 14 Measured increase in lateral junction under-diffusion caused by TED for different Si TGi implantation and anneal conditions. TED are separated from thermal diffusion by subtraction it from the reference L_{eff} for samples annealed at the same temperature but without TGi.