Non-linear Behavior of Al-contacted Pure Amorphous Boron (PureB) Devices at Low Temperatures

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Abstract - Deposition of pure amorphous boron (PureB) layers on n-type Si results in p^+n-like devices even in cases where B in-diffusion during the deposition is not expected. It is suspected that such behavior is due to the formation of an interfacial hole layer (IHL) between the PureB and Si. To further investigate physical mechanisms governing conduction of holes across the PureB/Si interface and through the IHL, electrical measurements were performed from room temperature down to cryogenic temperatures as low as 100 K. In this paper, current-voltage (*I-V*) measurements are made on structures where the PureB connects to p-type Si regions. One set of devices comprises ring-shaped structures designed for measuring the conductance through the IHL. In these structures, the PureB layer is deposited in rings that are contacted at the inner and outer perimeter with Al. Another set of samples includes devices where the PureB layer was deposited on p-type bulk Si. At room temperature, a close to linear change of current with voltage was seen irrespective of the PureB layer thickness and post-deposition processing. Lowering the operating temperature led to an increasingly non-linear *I-V* characteristics. Plausible explanations for the non-linear behavior are considered and discussed in the paper.

I. INTRODUCTION

Aluminum deposition is a common way of contacting semiconductor devices such as those made in Si technology [1], [2]. Depending on the physics and chemistry of the metal-semiconductor contact [3], Al can form a Schottky barrier to the semiconductor the rectifying behavior of which is used in Schottky devices [2]. In other devices, the Schottky barrier may impede the desired operation because an ohmic contact of the Al to the semiconductor is required. Consequently, fabrication methods have been developed to enable tuning of the Schottky barrier height [3]–[5]. Alternatively, tunneling of majority carriers through the Schottky barrier can be promoted to achieve ohmic contacting [2]. This is, for example, the case when Al is deposited on highly doped p-type Si [2], [6].

Al-contacting is commonly used in pure amorphous boron (PureB) deposition technology for fabrication of PureB photodiodes [7]–[9]. The attraction of PureB technology lies in the formation of nm-thin PureB layers obtained by Si exposure to diborane (B_2H_6) at different processing conditions and temperatures from 400°C to 700°C [10], [11]. Although the combined thickness of the PureB layer and B-diffused Si obtained from 700°C depositions can be lower than 10 nm, the saturation current density of PureB photodiodes is in the range of conventional deep-diffused pn-junction devices and can be lower than 10^{-19} A/μm^2 [10], [12]. An effective electron blocking mechanism was determined by emitter Gummel number measurements of devices where PureB was incorporated in the emitter region [12]. The physical mechanisms governing such behavior need to be further investigated. It has been proposed that a monolayer of acceptor states formed at the PureB/Si interface is responsible for creating a layer of fixed negative charge that can maintain an interfacial hole layer (IHL) which effectively behaves as a highly doped p-region [10], [13]. The presence of this p-type region is substantiated by experimental evidence showing high conductance along the PureB-Si interface even for deposition at 400ºC where no doping of the bulk Si is expected [14]. In other earlier work on deposition of amorphous boron layers on Si, they were found to cause band bending at the interface with the Si [15]–[17], supporting the existence of an IHL. In PureB photodiodes, the bonding leading to the formation of the IHL has been assumed to be responsible for the exceptionally good performance with respect to low dark currents, high stability, and robustness in harsh environments [18]. Moreover, it has been shown that the PureB serves as a diffusion barrier for pure aluminum deposition [19].

The nature of the Al-on-PureB contact and the relationship to the PureB/Si IHL is still a subject of investigation [20]. The experimental evidence gathered on PureB p^+n-like diodes that were metallized, shows that the electron blocking properties are unimpeded when PureB layer thickness is larger than 2 nm. However, increasing the thickness of the PureB layer negatively impacts the series resistance [12]. For longer B_2H_6 exposure time, the PureB thickness can be increased to some nm and for such thick layers the contact resistivity was shown to increase linearly with the thickness. A boron resistivity from 500 Ωcm to 10 kΩcm was determined where the spread was related to the process history of the deposition chamber [21].

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However, for layers thinner than about 3 nm, the contact resistivity is attractively low and it is suspected that the PureB layer then behaves as a high-ohmic tunneling layer [12]. A simulation study of an Al-Si configuration where a thin Si layer, on top of bulk Si, mimics the PureB properties in terms of doping concentration and thickness showed that an IHL could well be responsible for the observed blocking of the electron injection [20]. In the model, it was proposed that Al forms a Schottky barrier to the boron top layer through which holes tunnel from the IHL to the Al. The plausibility of this model was supported by measurements from [12].

In this paper, low temperature measurements of two sets of PureB devices are presented. They were performed with the aim of investigating the nature and the physical properties of Al-contacts to PureB layers and the connection to the IHL formed at the PureB/Si interface. Current-voltage (*I-V*) measurements are performed at temperatures from 100 K to 300 K for ring-shaped devices fabricated with different PureB deposition and post-deposition steps. Non-linearities in *I-V* characteristics of ring-shaped structures were observed at cryogenic temperatures for thick PureB layers. Similarly, non-linear behavior of the *I-V* characteristics was seen for measurements performed at lower operating temperatures for thick PureB layers on p-type bulk Si even though the contact to substrate was ohmic.

II. Device Fabrication

Two types of devices were examined. One type, ring-shaped structures, were fabricated with the basic design described in [22] that allows the extraction of the sheet resistance along PureB/Si interface. The schematic cross section and layout are shown in Fig. 1 where the width, L_{PB}, and radius, r_g, of the ring are indicated. The PureB layer was deposited in the whole ring and the inner and outer perimeter was contacted by Al.

The substrates used for fabrication of the PureB ring-shaped diodes were 1-10 Ωcm n-type (100) Si wafers. Guard rings at the ring perimeter were created by B^+ implantation to a dose of 10^{13} cm^{-2} at an energy of 180 keV through a 300-nm thick thermal oxide. The backside of the wafer was implanted with P^+ to a dose of 10^{15} cm^{-2} at an energy of 150 keV. The activation of the impurities was performed with a 20-min anneal at 1000°C. Wet etching of the oxide was performed to expose the Si surface for the PureB layer deposition at a temperature of 700°C. The duration of the PureB layer deposition was either 6 min or 20 min which gave a PureB layer thickness of approximately 3 nm or 8 nm, respectively [23]. Some of the devices were subjected to subsequent annealing steps at either 800°C or 850°C for 20 min and 30 min, respectively.

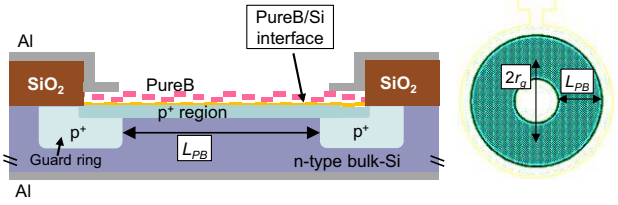


Figure 1. Schematic cross section (left) and top view (right) of ring-shaped devices that have PureB rings of varying width L_{PB} and radius r_g.

TABLE I. PureB depostion and post-deposition fabrication steps for ring-shaped structures.

Device name	PureB deposition	Post-deposition treatment	Junction depth (nm)
B[6,700]	6 min @ 700°C	-	6
B[20,700]	20 min @ 700°C	-	10
B[20,800]	20 min @ 700°C	10 min @ 800°C	35
B[20,850]	20 min @ 700°C	30 min @ 850°C	125
B[20,900]	20 min @ 700°C	20 min @ 900°C, PureB removal	190

The subsequent annealing had the effect of increasing the junction depth since the PureB layer can be used as an abundant source of B [10]. One of the samples where the PureB is deposited at 700°C for 20 min is subjected to a 900°C anneal lasting 20 min after which the PureB layer is removed by plasma etching. All the variations in the PureB deposition procedure and the post-deposition steps are listed in the Table I. Junction depths to a bulk doping concentration of 10^{15} cm^{-3} were obtained from the process simulations performed as described in [24]. Contacting of the devices was performed by the 875 nm Al deposition at 350°C which was patterned, and plasma etched down to about 150 nm followed by a HF wet etching to remove Al in the light-entrance windows. Al was deposited on the backside of the wafer at room temperature to a thickness of 675 nm to contact the cathode.

The second type of test structure, a simple contact to p-type bulk Si, was fabricated by depositing PureB in oxide windows to a p-type 2-5 Ωcm (100) Si substrate on which a 0.2-µm-thick surface doping of 10^{17} cm^{-3} was grown by epitaxy. The PureB layer was deposited in another reactor than for the ring-structures. It was a 10 min deposition at 700°C that gave a layer thickness of ~ 7 nm. With this reactor it was known that the resistivity of the PureB was in the 10 kΩcm range while for the ring-structures a much lower resistivity of about 500 Ωcm was expected [21]. The PureB was metalized as for the ring-structures on the front and back of the wafer.

III. Current-Voltage (*I-V*) Measurements

Low temperature measurements of the ring-shaped PureB devices were performed in a cryostat. Liquid nitrogen was used as a cryogen so temperatures as low as 77 K could be achieved. A Keithley parameter analyser 4200 SCS was used to measure the *I-V* characteristics of the devices. The measurements of the PureB contacts to p-type bulk Si were performed through the wafer using a wafer prober with a temperature-controlled chuck that enabled temperatures down to 3.5°C.

A. Ring-shaped PureB devices

Ring-shaped structures with $L_{PB} = 70$ µm were measured at temperatures from 100 K to 300 K. The PureB deposition conditions and post-deposition treatments are listed in Table I. The *I-V* characteristics were measured from the outer to inner contacts of the ring-structure by applying a voltage V_D to the inner contact. The results for the devices B[6,700] and B[20,700] that have no post-deposition anneals are shown in Fig. 2a and 2b, respectively. The B[6,700] device displays linear *I-V*

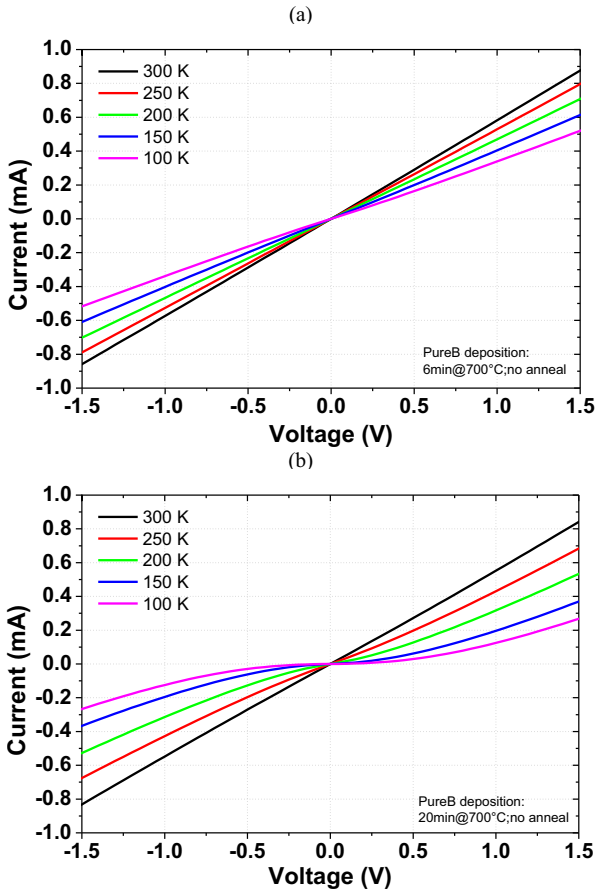


Figure 2. *I-V* characteristics of the PureB layer ring-shaped structures for temperatures between 100 K and 300 K where the PureB layer is deposited for (a) 6 min at 700°C, (b) 20 min at 700°C.

characteristics irrespective of the device temperature. At 300 K, the B[20,700] device also displays linear behavior but as the temperature decreases, the *I-V* characteristics start to show non-linear behavior.

Measurements on the structures where the PureB layer is deposited at 700°C for 20 min followed by post-deposition anneals show similar behavior in terms of non-linearities at low operating temperatures. The comparison of the *I-V* characteristics for the devices with various PureB deposition processes is shown in Fig. 3 for temperatures of 100 K and 300 K. Post-deposition anneals increase the junction depth of the p-type region under the PureB layer

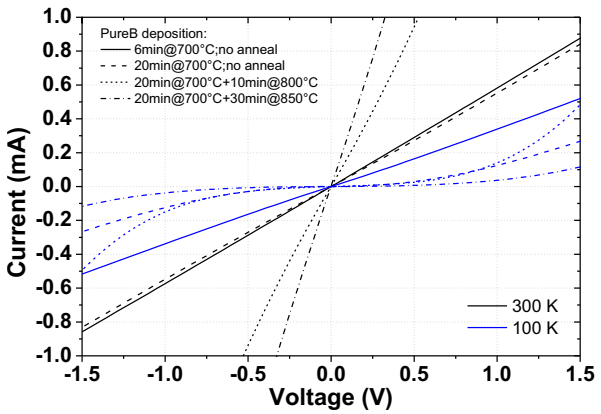


Figure 3. Comparison of the *I-V* characteristics for various PureB deposition and post-deposition steps for the temperatures of 100 K and 300 K.

due to B in-diffusion. These deeper junctions with higher peak doping have lower sheet resistance which could be seen from the *I-V* characteristics. As the temperature decreases, non-linear effects start to dominate the characteristics irrespective of the junction depth. Therefore, it is plausible that the thickness of the PureB layer is responsible for the observed non-linearities.

The current through the PureB ring was measured at 0.1 V for temperatures between 100 K and 300 K and plotted as an Arrhenius plot in Fig. 4. Measurements of the B[20,900] device where the PureB layer was removed prior to metallization is also shown for comparison. This device has the largest current level which is almost constant for the whole temperature range. The Al contact to the highly-doped p-type region obtained from the B in-diffusion forms a tunneling Schottky contact. Almost constant current with temperature was also measured for the device where the PureB layer deposition is performed for 6 min at 700°C. It is suspected that the PureB layer in such a device is sufficiently thin to allow for tunneling to the Al contact through the PureB layer. On the other hand, the devices with a thicker PureB layer deposited at 700°C for 20 min with different post-deposition annealing steps, show an exponential decrease of the current with decreasing operating temperature. The assumption that the holes tunnel to the Al contact through PureB layer, as proposed in the rudimentary model [20], would explain this behavior. A discussion on the tunneling mechanism and the connection to non-linearities in the *I-V* characteristics is provided in Section III.

B. Devices with PureB deposited on p-type bulk Si

To further study the impact of Al contact on conductance of holes in PureB devices, measurements were performed on PureB-on-p-type bulk devices with an area of 40×40 μm^2. The measured *I-V* characteristics for temperatures of 3.5°C, 10°C, 20°C, 30°C and 40°C are shown in Fig. 5. Non-linear behavior is observed even for temperatures as high as 40°C. The *I-V* characteristics are symmetrical around a bias voltage of 0 V. As the temperature decreases, non-linear effects start to become more prominent. As in the case of non-linearities in the ring-shaped structures, it is assumed that the thickness of the PureB layer is responsible for observed behavior. Moreover, for this sample a much higher PureB resistivity

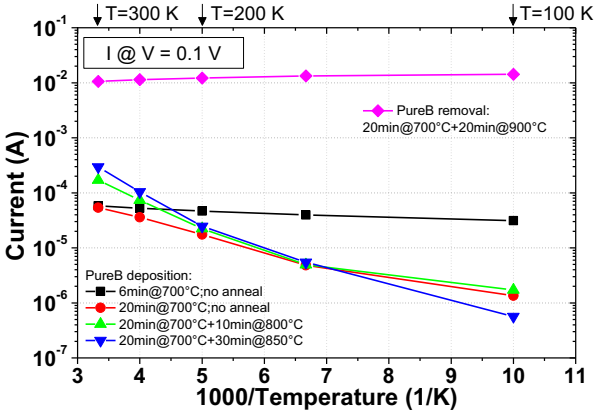


Figure 4. Arrhenius plot of the current measured at 0.1 V for the ring-shaped devices with various PureB deposition and post-deposition steps. For comparison, the measurements of the sheet resistance structure where the PureB layer is removed prior to the Al deposition is also shown.

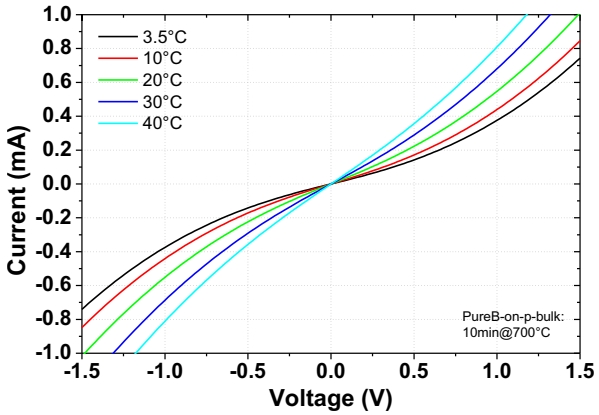


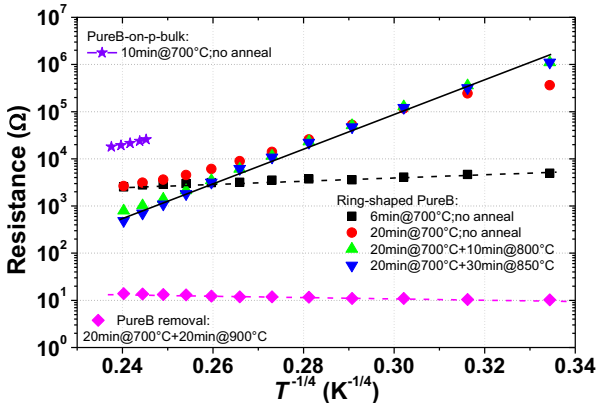
Figure 5. *I-V* characteristics of the device where PureB layer is deposited for 10 min at 700°C on p-type bulk for temperatures between 3.5°C and 40°C

is expected which may explain that the non-linearities could be observed even at room temperature.

C. *Comparison of temperarure dependent resistance extracted for various PureB devices*

From the *I-V* characteristics of the samples with $L_{PB} = 100$ µm, the resistance at 0.1 V bias voltage was calculated and the results are plotted with respect to $T^{-1/4}$ and shown in Fig. 6a for ring-shaped PureB devices with different deposition and post-deposition fabrication steps. For comparison, the resistance of the device where the PureB layer is removed and the device where the PureB layer is deposited on a p-type substrate is also plotted. The resistance of the B[6,700] device shows constant values irrespective of the temperature. However, the devices where the PureB layer is deposited for 20 min at 700°C show exponential increase of the resistance with decreasing $T^{-1/4}$ which characterizes variable range hopping conduction characteristic to amorphous materials [25]. The resistance with respect to $T^{-1/4}$ calculated at bias voltages of 0.1 V, 0.3 V and 0.5 V is shown in Fig. 6b. The measurements were performed for the devices B[6,700] and B[20,850]. For the device with 6-min PureB deposition it is suspected that the holes tunnel to the Al contact showing no change in the resistance for different bias voltages. Since VRH exhibits field dependence [26], the change in characteristics of thick PureB samples with bias could be due to VRH in the PureB layers. However, Schottky contacts can have similar temperature and bias dependence. Simulations of back-to-back Schottky contacts with a barrier of 4.25 eV to n-type bulk with doping of 10^{18} cm^{-3}, assuming the area of the device of 5000 µm^2 and a tunneling contact were performed in Sentaurus Device [27]. The work-functions define the slope of the resistance with respect to the temperature change. Simulation results are shown in Fig. 6b. For comparison, the analytical model for VRH is used to model temperature dependent resistance. Given that both Schottky contacts and the VRH mechanism show similar behavior with temperature, it could not be concluded with certainty that only the VRH or the Schottky resistance dominates the series resistance of the devices.

(a)



(b)

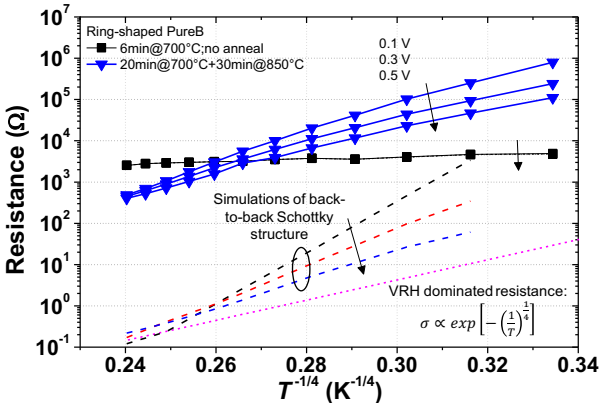


Figure 6. (a) Resistance at 0.1 V with respect to $T^{-1/4}$ for the PureB devices where the PureB layer is fabricated with various deposition and post-deposition fabrication steps. (b) Resistance with respect to $T^{-1/4}$ of the B[6,700] and B[20,850] devices. The resistance is calculated at voltages of 0.1 V, 0.3 V and 0.5 V. For comparison, simulations of a back-to-back Schottky structure and a VRH dominated resistance are shown.

IV. Discussion on the Origin of Non-Linear Behavior of Al-Contacted PureB Layers

For thick PureB layers the results show that the *I-V* characteristics change from almost ohmic behavior at room temperature to non-linear behavior at low temperatures. An explanation for this is offered by the rudimentary model of PureB-on-Si where Al forms a Schottky barrier to the PureB layer [20]. The band diagram in support of this model is made based on assumptions taken from [20] and is shown in Fig. 7. The thickness of the top layer was 5 nm, the IHL was modeled by a high fixed interface charge concentration, $N_I = 5\times10^{13}$ cm^{-2} at the interface between the Si top-layer and the bulk. The Al metal with work-function of 4.1 eV was assumed to form a Schottky contact to the top-layer with a barrier for holes. It is suspected that the holes from the IHL tunnel to the Al when the PureB/Si interface is brought close to the Al contact by a reduced thickness of the PureB layer. Thin PureB layers would thus form an ohmic contact. On the other hand, for thick PureB layers, tunneling of holes from the IHL to the Al contact would be suppressed at lower temperature. Both mechanisms, a change of the Schottky barrier tunneling with temperature or VRH, would result in non-linearities in the *I-V* characteristics as seen at low temperatures, and with

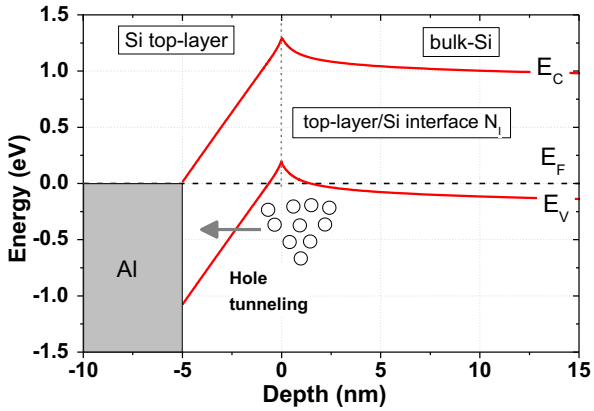


Figure 7. Band diagram of the Al-contacted Si top-layer on Si bulk with a thickness of the top-layer of 5 nm. The interface hole layer is simulated by assuming a fixed interface charge concentration of 5×10^{13} cm^{-2}.

the present measurements it is not possible to discern between the two.

Any further analysis is complicated since the PureB in ring-shaped structures was contacted by Al on either end of the IHL. It is assumed that contacts represent two back-to-back Schottky diodes with a resistor between, defined by the sheet resistance of the IHL, as shown in Fig. 8. To properly analyze such a structure, impedance spectroscopy could be used with an appropriate equivalent network [28], [29]. If a Schottky contact is formed, capacitive behavior of the Al-contacted PureB layers should become visible.

V. Conclusions

At room temperature, irrespective of the PureB thickness, the *I-V* characteristics are close to linear. It can be assumed that the Al contact to PureB is ohmic. Linear behavior is preserved even at cryogenic temperatures as low as 100 K for the samples with thin PureB layers or in cases where the PureB layer is completely removed. In contrast, ring-shaped structures with thicker PureB layers show non-linearities in *I-V* characteristics which are more pronounced when measurements are made at low temperatures. While VRH conduction in the PureB layer could well dominate the series resistance of the devices with the thicker PureB layers, similar temperature dependence would also be expected if the resistivity of the Schottky contact plays a role. In addition, tunneling of holes from the IHL to an Al Schottky contact would also explain the lower series resistance of devices with thin PureB layers that does not change with temperature. Likewise, both VRH and Schottky contacting could be responsible for the non-linear behavior observed for temperature dependent measurements of devices with the PureB layer deposited on p-type bulk Si. For this sample a much higher PureB resistivity is expected which may explain that non-linearities could be observed even at room temperature. The change of the tunneling with temperature is explained by the fact that the holes are tunneling from IHL to Al contact passing through PureB layer. Since the PureB layer should have an abundance of trap states, both VRH and direct tunneling of holes to the Al contact could support this behavior. This explanation is in accordance with the rudimentary model of the Al-contacted PureB-on-Si configuration proposed in [20]. Impedance spectroscopy should be performed to possibly confirm the assumption that a Schottky barrier is formed by Al deposition on PureB.

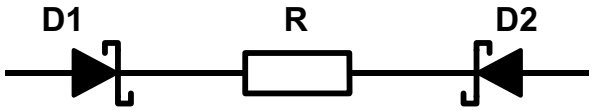


Figure 8. Back-to-back Schottky diode configuration representing the PureB contacted ring-shaped structure.

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