An Automotive MP-SoC Featuring an Advanced Embedded Instrument Infrastructure for High Dependability

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Abstract—In safety-critical systems, many-processor Systems-on-Chip are being increasingly employed. An example is an imminent collision detection System-on-Chip for cars. Such a system requires zero downtime and a very high reliability despite aging issues under harsh environmental conditions. By monitoring the health status of processor cores and other IPs, and taking appropriate counteractions if required, we accomplished this goal via IJTAG compatible embedded instruments. This paper shows the design of the required IJTAG network, and a number of new IJTAG-compatible embedded instruments like slack-delay, power-supply current I_{DDT} and Intermittent Resistive Fault monitors. In addition, we discuss their numbers and optimal locations in a processor core and provide a PDL description for one of our embedded instruments. In the case of for instance a four-processor implementation, requiring only two for actual data processing, the lifetime can increase by a factor of roughly three.

Keywords — IJTAG embedded instruments; IEEE 1687; power-supply voltage & temperature monitors; power-supply current I_{DDT}; slack-delay & IRF monitors

I. INTRODUCTION

With the decreasing dimensions in the low nanometers range, the option of many processor-cores in System-on-Chips (SoC) is becoming viable nowadays [1]. Many-Processor Systems-on-Chip (MP-SoC) find increasingly applications in safety-critical systems, like in automotive, where one can use processors as Electronic Control Units (ECUs). Unfortunately, the dependability of these MP-SoC systems is decreasing [2] and hence especially in safety-critical applications under harsh environmental conditions, on-chip counter actions are required to maintain a high dependability value. An example of such an application is the Imminent Collision Detection (ICD) system in cars [3, 4]. Already in 2003, Mercedes-Benz introduced this so-called PRE-SAFE system in their top-level line. It is a pure safety system confirming that a collision is unavoidable within fractions of seconds and guarantees the system only takes any drastic measures in the case of a real collision [3]. It is obvious that this type of system should require a very high dependability with zero downtime. The dependability of a cyber-physical system, like the ICD, depends on all parts of the system over time. Experience has shown that the *analogue* front ends (sensors, actuators, OpAmps, filters and data converters) of these systems often suffer in particular of offset drift and some timing problems [5, 6]. The increased introduction of digitally assisted mixed-signal IPs and embedded instruments [6] as well as advanced digital signal processing in the sensor parts [5] have shown to be able to improve their dependability.

The degradation of the clock frequency has shown to be a major issue in the *digital* processor cores of a cyber-physical system during lifetime because of aging; the degradation is strongly dependent on local temperature and voltage stress. The degradation can be observed using slack-delay embedded instruments in critical paths (after aging) and knowing the actual supply voltage and temperature. One can also monitor clock degradation via measuring the highly correlated I_{DDT} values [7]. Next, one can carry out these measurements on-chip in a pseudo on-line testing manner during lifetime. It requires however, a predefined workload for these tests [7].

Most dependability research nowadays relates to conventional fault models only, usually excluding intermittent faults. This paper includes the early monitoring of a special category, the intermittent resistive faults (IRF). This paper also presents the integration of temperature, voltage, slack-delay, power-supply current and IRF embedded instruments into a simple IJTAG network, following the IEEE 1687 standard. It guarantees a consistent configuration and data management to the internal processors and external world. Based on our previous measurement results of embedded instruments, one can actually predict on-chip the remaining lifetime of a processor core (prognostics) [8]. Next, one can apply isolation and substitution procedures with spare cores, realizing zero mean downtimes and an increased lifetime by a factor of three in the case of a 4-processor core SoC requiring only two processors for data processing.

The organisation of the paper is as follows. First, we give a short presentation and explanation of the set-up of the imminent collision detection SoC. In the next section, we discuss the number and locations of several chosen embedded instruments in the used OpenCore Plasma

processor core [9]. The major portion of the paper will then discuss a number of (new) IJTAG compatible embedded instruments, in particular the power-supply I_{DDT}, delay-slack and intermittent resistive fault (IRF) monitors. The latter improves the dependability by taking intermittent faults in the defect universe into account. Of the latter monitor, the paper will also provide the PDL description. Finally, we present the chosen IJTAG infrastructure of our SoC and conclusions are given.

II. DESIGN OF THE DEPENDABLE ICD MP-SoC

The currently available ICD systems require, unfortunately, a quite expensive sensory environment. A low-cost version for lower-medium cars makes use of anisotropic magnetic resistors (AMR) in combination with cheap acoustic sensors/actuator as used in parking systems, and a number of digital processors [4]. The short time period, a fraction of a second, before impact gives room for preparing counteractions like upright positioning of the chair, forward move of headrest to avoid whiplash, pre-fastening of the seatbelt and pre-inflating of the airbag. The imminent collision detector is actually a cyber-physical System-on-Chip. We have chosen for Open-Core Plasma processor cores (two and 4-core version) as digital signal processing resource [9]. Figure 1 shows that cores are interconnected via a network interface (NI) to a fault-tolerant network-on-chip (NoC), including routers (R). There is a FlexRay IP connection with the rest of the car electronics (e.g. other ICD SoCs) [10]. The focus of this paper is on the IJTAG embedded instruments in and around the Plasma processors. Segment insertion bits (SIB) connect the IJTAG client interfaces of the instruments to the JTAG

TAP controller [11]. The implementation of the design of the SoC uses the 40nm LP TSMC process. The sensory data comes from four AMR sensors (KMZ49), and two acoustic sensors/actuator (HC-SR04) and connected to the SoC via a bridge/NI to the NoC. As stated previously, much work on making specifically the AMR and front-end dependable has already been carried out in the past, and hence the remainder of this paper will focus on making the processor cores highly dependable.

In the processor cores, many non-trivial calculations take place [4], especially for the AMR sensors, to accomplish in the end a robust and reliable collision prediction via sensor fusion of both families of sensors. It is obvious that the cores play a vital role in the system, where zero mean down time and high dependability are a prerequisite. The two (/four) version cores have an overcapacity in calculation power, and hence one can consider one of them as redundant, to be used for automatic repair via run-time mapping software [12].

III. THE USED EMBEDDED INSTRUMENTS

The number, location, and choice of embedded instruments is a far from trivial process, requiring much work in advance. As aging of the processor cores, often reflected in reduced clock speed is the main issue, temperature (T) and voltage monitors (V) were selected, as they are major aging stressors; in addition they influence clock delay directly (Figure 2). One can measure delay degradation directly via slack-delay monitors (D), and indirectly via correlation [7] with an I_{DDT} monitor (I_{DDT}).

For detecting intermittent resistive faults, an IRF embedded instrument has been included (IRF), further enhancing the dependability.
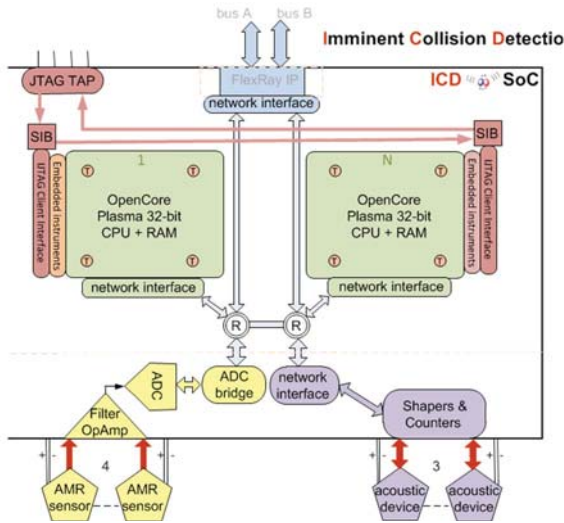

Figure 1. Schematic set-up of the Imminent Collision Detection (ICD) SoC, using two (or 4) cores, and four AMR sensors and three ultrasonic sensors/actuator externally.
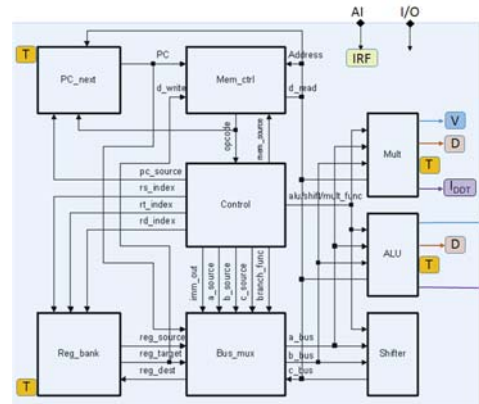

Figure 2. Plasma core [9] locations and number of embedded instruments. Temperature (T), Voltage (V), current I_{DDT}, Delay slack (D), and IRF embedded instruments.

We used several CAD tools to determine the locations of the embedded instruments. For temperature embedded instruments, we inserted them *within* the core very near functional blocks (e.g. ALU), in contrast to the conventional locations *outside* the core. The above has obvious consequences for the layout of the Plasma core. Our developed framework for temperature calculations in processors (VHDL-based) under realistic workloads [13] was used to determine the ranking of the most likely hotspots *in* the processor, being the multiplier and ALU units, besides program counter and register bank. Based on this, we also inserted the voltage and current embedded instruments (*outside* the core). The delay-slack embedded instrument locations on critical paths were guided via timing analysis under NBTI aging in 40 nm CMOS [14]. In total nine embedded instruments per core have been used, as shown in Figure 2.

A. Temperature and Voltage Embedded Instruments

Temperature (T) and voltage (V) embedded instruments are major health monitors for processor cores since local high temperatures and voltage stress accelerate aging and hence reduce dependability due to phenomena such as e.g. negative bias temperature instability (NBTI) [14].

Researchers proposed several monitoring mechanisms for temperature in the past such as the bipolar junction transistor (BJT) based ones [15], CMOS delay based, resistor temperature dependency approaches, and threshold. One can find BJTs in the form of parasitic lateral or vertical transistors in CMOS processes, and they are the most suitable due to their robust sensing nature and corrections by one-point calibration. We employ BJTs [15] as the basis for our temperature embedded instruments.

In the case of voltage monitoring embedded instruments, researchers also suggested several approaches, such as the ones based on ringoscilators (RO) [16] and the more sophisticated techniques employing feedback [6]. In the ICD-SoC, the RO approach is used. Temperature & voltage embedded instruments can also be imported in a design via IP vendors [17]. We especially designed the remaining embedded instruments in the ICD-SoC, which we discuss subsequently.

B. The Slack-Delay Embedded Instrument

The dominant aging mechanisms in processors (i.e. NBTI) are strongly dependent on the operating conditions as well as the workload. Within a die, temperature and voltage variations affect the timing of critical paths differently. In order to monitor delay slack in critical paths, we present a slack-monitor in the 40nm TSMC processing. Figure 3 shows the proposed
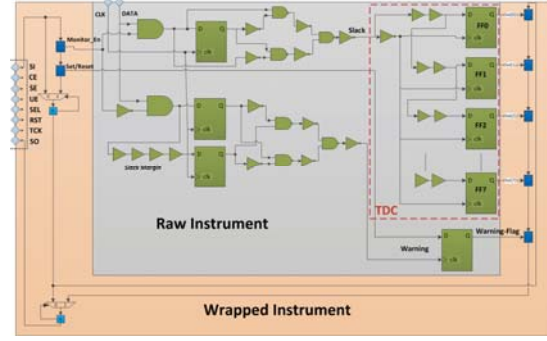

Figure 3. The raw delay-slack monitor and the IJTAG wrapped embedded instrument extension.

embedded instrument. It operates in two modes, depending on the logic status of the signal 'Monitor_En'.

If 'Monitor_En=0', the "Slack_Monitor" block will look for any timing violation in the critical path. One can control this violation time via the 'slack margin', which is essentially a chain of buffers. If there is any violation it sets the "Warning_Flag=1" (Figure 4). We also envision that fault propagation from an embedded instrument to the IJTAG controller will have a separate mechanism as proposed in [18]. At the moment the IJTAG controller receives the 'Warning-Flag', it will configure the instrument to determine the exact timing information by setting the 'Monitor_En' control to '1'. If the signal 'Monitor_En=1', the embedded instrument will measure the timing difference between the data-transition and the upcoming positive clock edge. One of the major aspects of the proposed design is its independence from the data transitions. It works for both a transition on the data signal i.e. from "1 -> 0" and from "0 -> 1" (Figure 4). This slack pulse is then applied to a Time-To-Digital Conversion (TDC) circuit that converts it to a (thermometric) digital code. The TDC block has
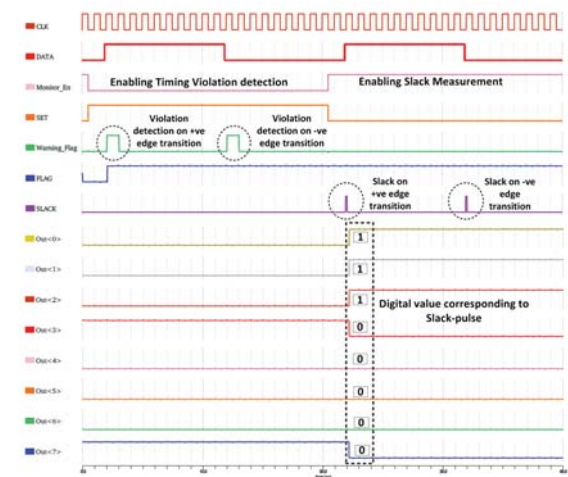

Figure 4. Simulation results of the raw delay-slack monitor using 40nm TSMC processing.

one input signal 'slack' and an 8-bit output. The slack pulse passes through the delay line; when the negative edge of 'slack' occurs the value in the delay line, flip-flops captured it. One can increase the resolution of the TDC by reducing the delay elements in the delay line. In the current implementation, each buffer consists of two inverters. The user can select the delay line depending on the monitoring requirements.

C. The I_{DDT} Current Embedded Instrument

An alternative approach for monitoring processor clock-frequency degradation from aging is based on its strong correlation with the transient current of the core [7]. In Figure 5, we present the raw I_{DDT} embedded instrument globally, as well as the IJTAG wrapping around the raw EI. Researchers developed off-chip as well as on-chip I_{DDT} monitors since the nineties, where in the design, speed and resolution are main issues [19]. One option for the EI consists (Figure 5) of a current to voltage conversion, taking care to remain as close to V_{DD} for the core under test as possible. After amplification of this voltage, one can use a voltage-controlled RO in combination with a counter to provide (14-bits) digital data. Furthermore, several supporting circuits are required, like a controller and a samples memory. Registers for the BIST of the EI, a BIST enable and BIST pass/fail are available (Figure 5). Another register is for calibration purposes. To start the I_{DDT} measurement, and get samples and finally indicate the completion of samples, requires three registers; the above combinations are referred to as Control and Status TDRs. Of particular interest are the configuration TDR registers, providing settings on e.g. the chosen window. We present an I_{DDT} embedded instrument, which is compatible with the emerging standard IEEE 1687. By using this standard, one can configure the monitor in the proper modes (e.g. set the window) and subsequently measuring the currents; it can be flawlessly fused with other IJTAG embedded instruments and a proper network structure [3].
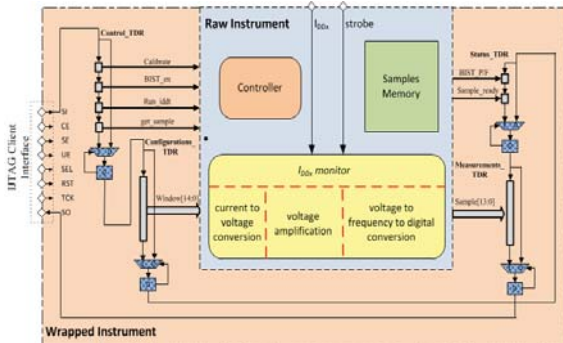
One can carry out the measurements via the TAP controller during final testing, or internally during lifetime via an embedded IJTAG controller [11]. It opens the road for zero mean downtime, and significantly increased reliability in the case of homogeneous multi-processor SoCs. We presented some initial results of a first version embedded instrument as a poster in [20].

D. The Intermittent Resistive Fault (IRF) Embedded Instrument

Figure 6 shows the raw IRF monitor wrapped with IJTAG into an embedded instrument. The IRF monitor checks the timing and the guard-band of a selected (wire) path of the circuit, which is result of an intermittent resistive fault in that wire. If a specified guard-band (safety margin) is violated, it provides a warning signal which is a sign of an impending timing failure. In this case, an IJTAG register captures the amount of violation. After the warning flag is high, the IJTAG controller reads the stored data and sets the ACK signal. This signal acts as a reset for the IRF embedded instrument.

Figure 7 shows the simulation results of the IRF EI inserted in a critical path of an AES-128 encoder circuit. The clock of the system is depicted on top of this figure. The signal "guard-band" (Figure 6) is the slack of the selected path that one should not violate. The signals "Data" and "Data*" are the outputs of the path in fault-free and faulty cases. The signal "Warning" shows the moment a timing violation is detected and the combination of output signals (Out[0], Out[1], Out[2], Out[3]) determines the amount of violation.
In Figure 7, the simulation result is provided for an 8 ns time duration. As can be seen, the monitor detected two IRFs, one at 3.1 ns and the other at 4.5ns.

Figure 5. The raw I_{DDT} monitor block scheme and the wrapped embedded instrument version.
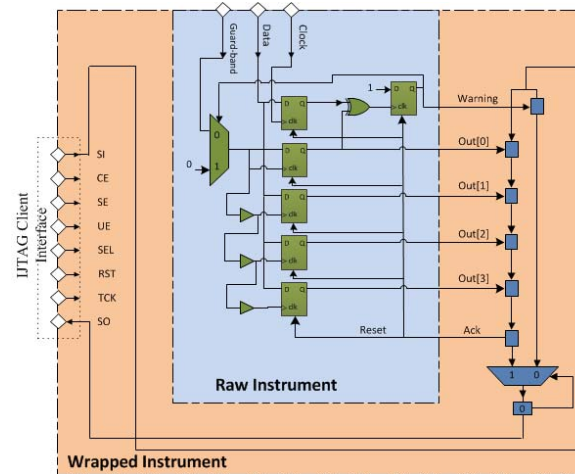

Figure 6. Raw intermittent resistive fault (IRF) monitor and the IJTAG wrapped embedded instrument.
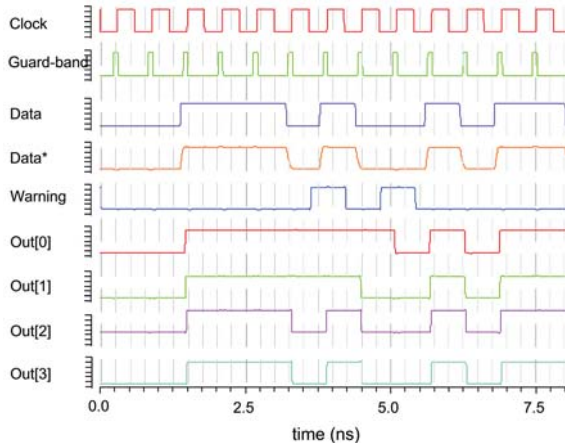
Figure 7. Simulation results of the IRF embedded instrument, including the warning signal.

The amount of violation for each IRF is being stored in the monitor register, which are "1100" and "1000", respectively. It means the first IRF is more severe. The detection of IRFs opens the possibility to enhance the dependability *beyond* current standards. As the location of IRFs is fixed, repair options via e.g. bypass are feasible. We published an initial version of an IRF monitor in [21].

IV. THE IJTAG INFRASTRUCTURE

In order to standardize the access methodologies of the growing number of embedded instruments integrated in SoCs, a consortium introduced the IEEE 1687 standard. IJTAG [11] presents a reconfigurable scan network infrastructure for an optimized access path to the instruments Test Data Registers (TDRs) as shown in the previous embedded instruments. In addition, two languages are introduced, the Procedural Description Language (PDL), which one can use to document the instruments access procedures; the Instrument Connectivity Language (ICL) is used to document the network organization. A provider of a wrapped instrument gives instrument-level ICL and PDL files describing both the TDRs organization and the instrument access procedure respectively; they are further used to construct a chip-level ICL file along with the system-level procedure that processes on the runtime instruments data (e.g. a lifetime prognostics procedure). To reuse the instruments, the standard defines a process referred to as the *retargeting* process. To access a certain TDR, a so-called retargeter implemented in software [22] or in hardware [23], which analyses the network organization provided in ICL, and generates a set of scan vectors to configure the network to include the required TDR in the active scan path. For simplicity, this IJTAG controller has not been included in Figures 1 and 8. An essential
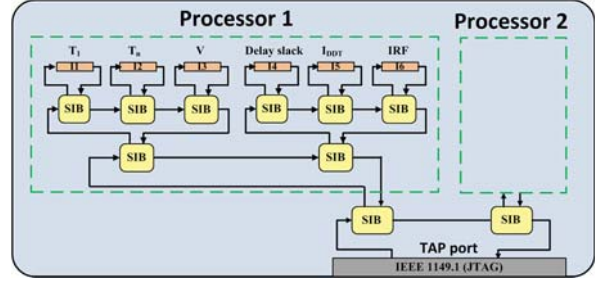

Figure 8. Our SoC IJTAG infrastructure, including six embedded instruments per core: temperature (T_i), voltage (V), delay slack, power-supply current (I_{DDT}) and intermittent resistive fault (IRF).

component of the IJTAG network is the Segment Insertion Bit (SIB), which allows for including and excluding attached scan segments, and consequently allows a scalable hierarchical network organization. Figure 8 shows our case of a 3-levels SIB hierarchy connecting the instruments TDRs (our temperature, voltage, delay slack, I_{DDT} and IRF monitors) that are contained in the two-processor cores.

In reference [11], we discussed our IJTAG integration of embedded instruments in detail. Using, in addition, instruments access schedules [24], one can even construct an optimized IJTAG network hierarchical organization automatically.

Figure 9 shows a simple access procedure written in PDL for the IRF embedded instrument shown in Figure 6, including a simple logical synchronization mechanism between the IJTAG controller and the instrument. This controller continuously polls on the warning flag until a warning is raised (lines 4-7); then it reads the output data and concurrently writes a '1' in the acknowledge register in order to notify the instrument to reset its warning and data outputs (lines 8-10). Finally the controller resets the acknowledge flag in the next scan cycle (lines 12-13). The data provided by the IJTAG connected embedded instruments we subsequently use in a lifetime prediction algorithm, deciding at which moment to start isolating and replacing processor cores *before failure*. A lifetime increase of a factor of three can be accomplished here, thereby significantly increasing the dependability.

```
1   iPDLLevel 1
2   iProcsForModule IRF_Monitor
3   set Status 0
4   while { $Status == 0} {
5       iRead IRF_Monitor.Warning
6       iApply
7       set Status [iGetReadData IRF_Monitor.Warning] }
8   iRead IRF_Monitor.Out
9   iWrite IRF_Monitor.Ack 0b1
10  iApply
11  set IRF_Out [iGetReadData IRF_Monitor.Out]
12  iWrite IRF_Monitor.Ack 0b0
13  iApply
```

Figure 9. Simple example of a PDL file of the IRF embedded instrument.

V. Conclusions

In safety-critical systems, like in automotive, designers increasingly use many-processor core SoCs. We have shown the design of a dependable many-processor SoC for Imminent Collision Detection in cars. This paper deals with the design of highly dependable processor cores in this SoC, with no down-time, by using several embedded instruments, IJTAG infrastructure and lifetime prognostics (software). We presented several IJTAG-compatible instruments in detail, including a PDL example description. We verified the EI designs by simulation, and currently a 40nm TSMC dual-core SoC is under construction. By this approach, the MP-SoC lifetime is significantly increased.

Acknowledgments

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