Applying IJTAG-Compatible Embedded Instruments for Lifetime Enhancement of Analog Front-Ends of Cyber-Physical Systems

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***Abstract*—In safety-critical cyber-physical systems, analog front-ends combined with many-processors are being increasingly employed. An example is an imminent collision detection chip for cars. Such a complex system requires zero downtime and a very high dependability despite aging issues under harsh environmental conditions. By on-line monitoring the health status of the processor cores and taking appropriate counteractions if required, we have accomplished this goal in the past via IJTAG compatible embedded instruments and appropriate embedded software. This paper extends this approach to the analog / mixed-signal frontends of these systems, thereby creating a new uniform approach in design & test methodology, as well as a streamlined fault management. An IJTAG-compatible voltage monitor is introduced, for measuring aging-generated offset in OpAmps and SAR ADCs, as well as a delay-monitoring embedded instrument for detecting timing issues in ADCs. In addition, two-stage counter measures, like digitized recalibration and subsequent replacement, are presented to increase the lifetime by factors of the analog front-end of Cyber-Physical Systems-on-Chips.**

***Index Terms*— IJTAG embedded instruments, Analog front-ends, IEEE 1687, offset voltage & delay monitors, dependability, PDL , ICL**

I. Introduction

Infield testing, aging monitoring and failure prediction will be essential in the future especially for safety in the transportation industry [1]. Cyber-Physical Systems-on-Chip (CPSoC), including analog/mixed-signal front & back ends and many-processor cores increasingly find their way in applications in automotive safety-critical systems. Unfortunately, the overall dependability of these complex systems is decreasing [2]. Hence, especially in safety-critical applications under harsh environmental conditions, on-chip on-line monitoring and counteractions during lifetime are a prerequisite to maintain a high dependability.

A promising example of such an application is the Imminent Collision Detection (ICD) system in cars. Recently, Mercedes-Benz introduced their so-called PRE-SAFE system in their top-level line [3]. It is an (expensive) pure safety system confirming that a collision is unavoidable within fractions of seconds and guarantees the system only takes any drastic measures in the case of a real collision. It is obvious that this type of systems should require a *very high* dependability with *zero* downtime.

In a previous paper [4], the degradation of the system clock frequency has shown to be a major issue in the *digital* processor cores of a CPSoC during lifetime because of aging; the degradation is strongly dependent on local temperature and voltage stressors. This degradation can be observed using slack-delay embedded instruments (EIs) in critical paths (after aging) as well as on-line monitoring the actual supply-voltage and local temperatures via dedicated embedded instruments. By integrating these EIs into an IJTAG network [4], following the IEEE 1687 standard [5], one can guarantee a consistent monitoring, configuration and data management to the internal processors and external world. Based on our previous measurement results of IJTAG-compatible embedded instruments, one can actually *predict* on-chip the *remaining lifetime* of processor cores (prognostics) [6] by looking at the *degradation trends* in the measurements results via embedded software. It is emphasized that these are not warning flags from an EI in the case a failure has occurred. After the prognostics decision, one can apply isolation and substitution procedures with spare cores, realizing zero mean downtimes and an increased lifetime by a factor of three in the case of a 4-processor core SoC requiring only two processors for data processing [7].

However, the dependability of a CPSoC, like the ICD, depends on *all* parts of the system over time, not only the digital processor cores. Experience has shown that conventional Analogue Front Ends (AFE), incorporating sensors, actuators, OpAmps, filters and data converters, often suffer from aging, in particular from offset drift and timing problems [8]. The increased introduction of digitally-assisted mixed-signal IPs and embedded instruments as well as advanced (embedded) digital signal processing features hold a promise to also improve

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their dependability. This paper extends the approach used for digital processing cores [7] to the analog frontends of these systems, thereby creating a new uniform approach in design & test methodology, as well as a streamlined fault management for highly dependable CPSoCs.

The setup of this paper is as follows. First, a short introduction of the architecture of our low-cost imminent collision detection CPSoC is given. Next, the effects of NBTI aging on analogue front-end IPs are shown. Subsequently, two chosen embedded instruments as being used in our the analogue / mixed-signal front end are discussed. These new IJTAG-compatible embedded instruments are an *offset* and a *delay* EIs. Of the first monitor, the paper will also provide a flow diagram for its PDL access procedure [5]. Next, the chosen IJTAG infrastructure of our CPSoC is shown as well as simulation results of counteractions at the architectural level for enhanced dependability under aging. Finally, conclusions are given.

II. Design of the Dependable ICD CPSoC

The recently available ICD systems require, unfortunately, a quite expensive (radar) sensory environment [3]. A cheap version for lower-end cars makes use of low-cost Anisotropic Magnetic Resistors (AMR) in combination with cheap acoustic sensors/actuator as used for parking, and a number of digital processors [9]. The magnetic sensors detect another nearby car via distortion of the magnetic field in *combination* with ultrasonic reflections. The short time period before impact, a fraction of a second, gives room for preparing counteractions like upright positioning of the chair, forward move of headrest to avoid whiplash, pre-fastening of the seatbelt, and pre-inflating of the airbag. We have used four Open-Core Plasma processor cores as digital signal processing resources (Figure 1), which are interconnected via a network interface (NI) to a fault-tolerant network-on-chip (NoC), including four routers (R). The health of each core is being monitored by eight IJTAG-compatible embedded instruments, among them four temperature embedded instruments labelled T [4].

In (two) processor cores, many non-trivial calculations take place [9], especially for the AMR sensors, to accomplish in the end a *robust* and *reliable* collision prediction via sensor fusion of both families of sensors. It is obvious that the cores play a vital role in the system, where zero mean down time and high dependability are prerequisites. The four-cores implementation has therefore an overcapacity in computational power and hence one can consider two of them as redundant, to be used for automatic repair via

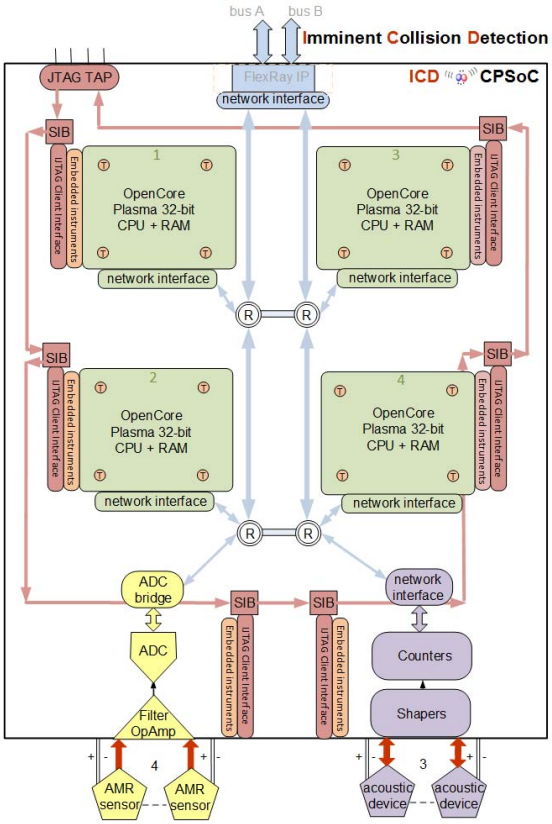

Figure 1. Schematic set-up of the Imminent Collision Detection (ICD) CPSoC, using four Plasma processor cores, and four AMR sensors and three ultrasonic sensors/actuator externally

isolation, spare-core insertion supported by run-time mapping software [7].

The focus of this paper is on the IJTAG-compatible embedded instruments around the analogue / mixed-signal parts (Figure 1). Segment insertion bits (SIB) connect the IJTAG client interfaces of the EIs to the JTAG TAP controller [5]. The sensory data comes from four AMR sensors and two acoustic sensors/actuator and they are connected via their AFEs to the CPSoC via a bridge/NI to the NoC. For the AMRs, the analogue front ends consist of OpAmps/filters and a data converter.

III. Aging of Analogue Front Ends

Front (and back) ends, usually consist of sensors and actuators, often in combination with operational amplifiers, filters and data converters (ADC & DAC). For simplicity this paper will confine itself to front ends, without losing generality. With regard to dependability, sensors are the most critical parts as, by nature, they have to directly interact with the physical environment. Because of the low signal levels and noise from sensors, the amplifiers/filters and ADCs are usually closely located to them. As a result, their mission profile will not be favourable, and hence they are expected to be more susceptible to wear out /aging as compared to the other

(digital) parts. Subsequently, some examples will be provided of aging in a sensor, OpAmp and SAR-ADC.

A. Aging in Sensors

Because of their direct interaction with the environment, sensors are quite aging dependent. Our previous aging research with respect to AMR sensors [10] has shown that drift, even after initial calibration, changes over time. Figure 2 shows the measurement results of their offset in the case of two (45^0 shift in orientation) Wheatstone bridges consisting of magneto-resistive components. It shows ~60μV/V changes in the beginning, and less after 1700 hours of stress. Most sensor types show drift of offset during aging, especially if temperature (-20^0C – 70^0C) and voltage stresses are present. Any drift can lead to malfunctioning systems in a car.

We have shown [10] that measuring (bridge) voltages (voltage monitor) can be used as basis for drift monitoring and based on this data counteract with full compensation. Also the concept of coil-assisted flipping can be used.

In the case of our ultrasonic (piezoelectric) sensors/actuator, also aging will take place; although their behaviour in terms of drift is usually good, their performance will degrade [11]. This of course also depends on their actual implementation; piezo-*resistive* ones are more sensitive to drift. Our key parameter (delay) can be observed digitally for potential recalibration, so a delay-monitor embedded instrument will be required.

B. Aging in Operational Amplifiers

Conventional operational amplifiers (OpAmps) in advanced CMOS technology age in terms of their offset and gain values, because of the NBTI (Negative Bias Temperature Instability) aging of the used nanometer transistors [8]. The simulated offset over time of a 65nm CMOS OpAmp, employing our specially developed analogue-signal NBTI model, shows a rapid increase in the first years and a slower increase later on [8]. A voltage monitor embedded instrument should be able to measure these values (in our case a 20mV offset-voltage range).

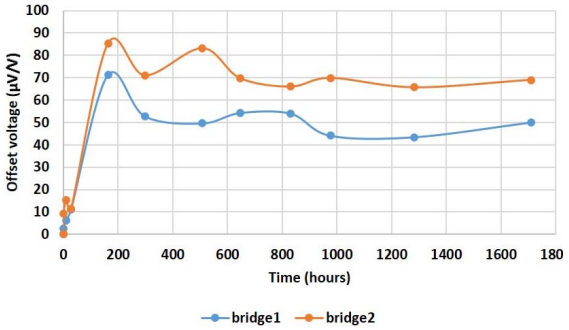

Figure 2. Measured offset changes in two AMR sensor bridges (45^o) due to aging resulting from stress temperatures and voltages

C. Aging in Successive Approximation Register ADC

Conventional SAR ADCs in advanced CMOS technology (65nm) age in terms of their offset and their timing, because of the NBTI aging of the used nanometer transistors [8]. Figure 3 shows the behaviour of our SAR-ADC after 10 years of time, operating at 125^0C. The timing error (~ 0.5ns) is primarily due to the increased delay from the self-timing asynchronous SAR logic. The 4-LSB error at the ADC output is a result of decision errors due to the aging-induced offset in the comparator. A voltage monitor EI and a delay monitor EI could measure these changes and, depending on the prognostics software, decide on counteractions. In the next paragraph two IJTAG-compatible embedded instruments will be introduced that can monitor offset voltage and delay changes that occur in AFEs.

IV. The Used Embedded Instruments in AFE

The choice, number and location of embedded instruments is a far from trivial process, requiring much work in advance. Temperature (T) and supply-voltage (V) embedded instruments are major health monitors for all IPs since local high temperatures and voltage stress accelerate aging and hence reduce dependability due to phenomena such as e.g. NBTI [4]. The supply-voltage monitors for instance, can be shared thereby reducing their number. In literature, many implementation forms can be found of these [4]. In the previous paragraph on aging of AFEs, the offset-voltage monitor and delay monitor were suggested as good choices for monitoring the health of analog/mixed/mixed-signal front ends, and will therefore be discussed now.

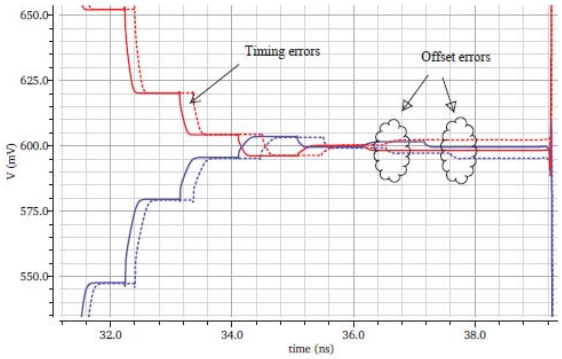

Figure 3. Simulated offset and timing changes due to NBTI aging of a 65nm CMOS standard SAR Analog-to-Digital Converter using an analogue -signal NBTI model

A. Offset-Voltage Embedded Instrument

In the case of offset-voltage monitoring, Figure 4 shows an IJTAG-compatible approach for monitoring offset voltage (and gain) via the principle of feedback [8]. Our embedded instruments are divided into raw (original) instruments and their IJTAG wrapper. Its basic operation has resemblance with the principle of successive approximation, where the analogue offset value is compared (comparator/detector) with a (10-bits) digitally-controlled DAC. Most of the digital (β) generation and handling is carried out by an embedded processor via the IJTAG network.

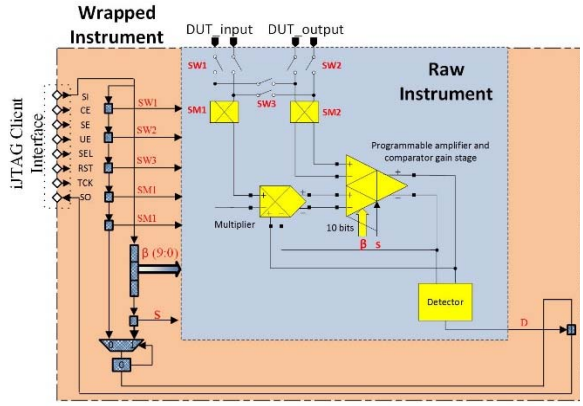

Figure 4. Raw and IJTAG-wrapped voltage embedded instrument

The functional flow of the EI operation is shown in Figure 5. First, the EI is connected to the DUT (OpAmp or ADC in our case) via the electronic switches SW1 and SW2 (Figures 4, 5). The switch mixers SM1, SM2 and SM3 are reset to zero. These are the same kind of switch-mixers as being employed in chopper-stabilization circuits. Next, programming of the β value is based on a binary searching method to find the desired value of β which basically inverts the detector. If this value cannot be found, the sign (S) of β is set to a negative value and the search has to continue again. If the value can still not be found, it means that no real solutions exist for these SM1 and SM2 combinations. By changing the settings for either SM1 or SM2 and repeat the same procedure, it will be possible to find all offset solutions. Finally, the results (β and S) are available in the embedded-processor registers, and otherwise an error will be reported. The analog equivalent of β is the value of the monitored offset. The above functional flow can been directly translated into a PDL description [5] for this embedded instrument.

Simulations of the offset-voltage EI in 65nm CMOS TSMC technology have shown the correct behaviour of the circuit; the offset-voltage range is from 200μV – 70 mV, with an accuracy of ~ 100μV [8].

B. Delay Embedded Instrument

The IJTAG-compatible delay monitoring EI for our 10-bits SAR ADC is shown in Figure 6. Simulation results using the 40nm TSMC technology library are

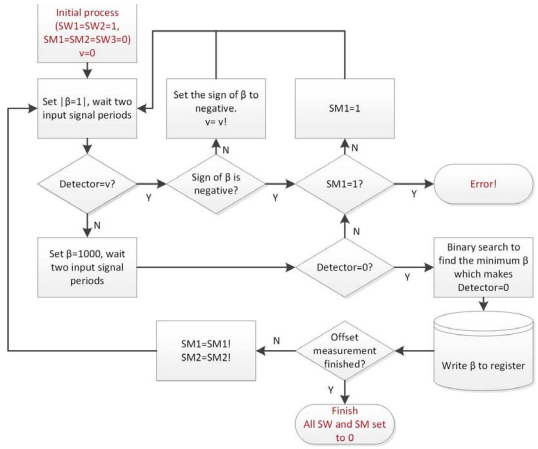

Figure 5. Flow diagram of the voltage embedded instrument measurements and the basis of its PDL description

shown in Figure 7. The monitor takes two signals from the SAR ADC, one from the comparator of the SAR ADC labeled 'from_SAR' and other the signal 'Sampling_clk'. If the internal signal 'Monitor_En=1', the EI will first count (4-bits) until the value '1010' to verify if the conversion by the ADC has been completed. In the case the counter reaches the value '1010', the signal 'finish' will change from a logic '0' to '1'. To monitor the time difference between the 'finish' signal and 'Sampling_clk', the 'delay' pulse is generated (Figure 7). This pulse is then applied to a Time-to- digital Conversion (TDC) circuit that converts it to a (thermometric) digital code. The 'delay' signal passes through the delay line which consists of buffers and when the negative edge of the signal 'delay' occurs, the value in the delay line is captured into the D-flip flops. The reliability simulation of the SAR-ADC shows (Figure 3) that the total delay induced by (NBTI) ageing is around 500ps; hence the resolution of the TDC is set to be 58ps and it can measure a maximum width of the delay pulse up to 464ps.

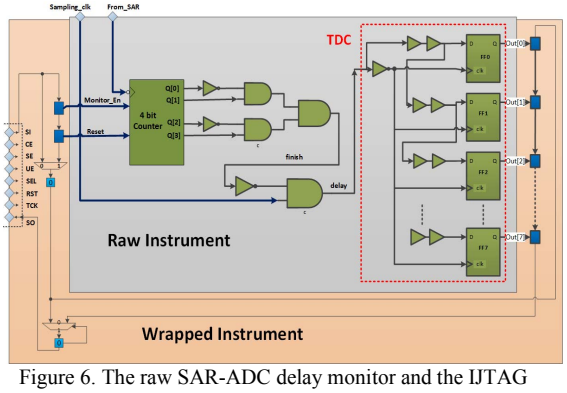

Figure 6. The raw SAR-ADC delay monitor and the IJTAG wrapped embedded instrument extension

V. THE IJTAG INFRASTRUCTURE

To standardize the access methodologies of the growing number of EIs integrated in e.g. CPSoCs, a consortium introduced the IEEE 1687 standard [5].

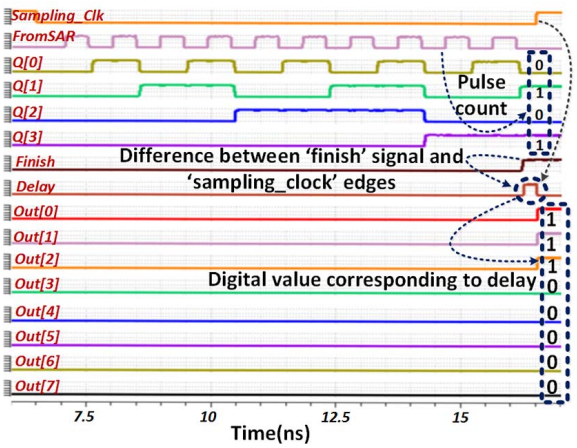

Figure 7. Simulation results of the delay embedded instrument using 40nm TSMC CMOS processing

IJTAG presents a reconfigurable scan network infrastructure for an optimized access path to the embedded instruments' Test Data Registers (TDRs) as shown in the previous EIs. In addition, two languages have been introduced, the Procedural Description Language (PDL), which can be used to document the instruments access procedures, while the Instrument Connectivity Language (ICL) is used to document the IJTAG network organization [5].

A provider of wrapped EIs gives instrument-level ICL and PDL files describing both the TDRs organization and the instrument access procedure respectively; we developed these for the offset EI and ICD chip. They are further used to construct a chip-level ICL file along with the system-level procedure that processes on the runtime instruments data (e.g. a lifetime prognostics procedure). To reuse the instruments, the standard defines a process referred to as the *retargeting* process [5].

To access a certain TDR, a so-called retargeter is implemented in for instance software, which analyses the network organization provided in ICL, and generates a set of scan vectors to configure the network to include the required TDR in the active scan path. An essential component of the IJTAG network is the Segment Insertion Bit (SIB), which allows for including and excluding attached scan segments, and consequently allows a scalable hierarchical network organization.

Figure 8 shows our case of a 3-levels SIB hierarchy connecting the embedded instruments TDRs (our offset-voltage and delay EIs) that are contained in the analogue/mixed-signal IPs. In Figure 8, the (bottom) hierarchy of the IJTAG network is shown, being the AMR sensors #N (N=1,..4, Figure 1), and the ultrasonic sensors #M (M=1,..3, Figure 1); for simplicity only one of each is shown. The AMR sensor is connected to an offset-voltage EI, as is the OpAmp/filter, for monitoring the offset. The ADC is connected to an offset-voltage and delay EI for monitoring offset and timing degradation respectively.

Figure 5 shows the control flow graph for the PDL access procedure [8] of our analogue offset-voltage EI, indicating how to operate this particular instrument.

VI. System-level considerations

As previously discussed, our whole infrastructure of embedded instruments, IJTAG network, and embedded prognostics software running on an embedded processor (e.g. Plasma) has been introduced to get a significant lifetime enhancement and *zero* down time of our automotive CPSoC. This is in contrast with normal fault-reacting systems [7], and their fault- management systems exhibiting a significant down time.

In the case of the analog/mixed-signal part of a CPSoC, the sitiuation is much more difficult than in a pure digital situation [7]. As we have seen, phenomena like NBTI aging results in this case in changing key system parameters of IPs (OpAmps, filters, ADCs & DACs), like offset, gain and changing frequency behaviour. As stated before, the EIs are used to measure the *trend* in key-parameter degradation. Based on that, the prognostics software decides via data fusion [6] when to start counteractions, *before* an actual failure occurs. We use a two-stage scenario which, to some extend, is similar to the pure digital case [7]. In the digital case, workload reduction, clock frequency and voltage reduction are used. This cannot be used in the analogue/MS case without completely changing system parameters. The first step is here therefore using *recalibration* of the digitally-assisted mixed-signal IPs, controlled and monitored by the embedded (prognostics) processor. A classical recalibration solution is using a simple current-controlled DAC connected to the first differential stage of the IP. Simulations have confirmed their correct behaviour. However, recalibration has its limitations in terms of maximum range. If that maximum has been reached, a replacement of a non-aged IP has to be performed via

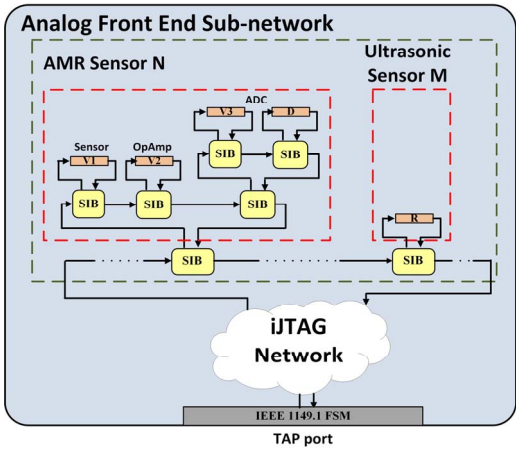

Figure 8. Our CPSoC IJTAG infrastructure of the AFE, including some embedded instruments per IP: voltage (V) and delay (D). The TDR labelled R is a 10-bits register. The IJTAG Network cloud consists of the embedded instruments infrastructure required for the four digital PLASMA processor cores (Figure 1).

isolation and bypass similar to the digital case [7]. Figure 9 shows four possible aging-degradation scenarios, as well as the application of our two-stage repair approach. First, key parameters are monitored and digitally tuned if changing; when the maximum tuning range is accomplished, a bypass and spare IP counter action is carried out [12]. One can see from the figure that the CPSoC remains within its green boundaries (of an arbitrary performance parameter P) of correct operation. It also shows that the different degradation mechanisms trigger tuning and replace countermeasures at different times. The lifetime improves roughly by a factor of four at the cost of more sophisticated embedded instruments monitors (2 spare IPs each), software and embedded computational resources, all translating into more Silicon area. Also very important is that now the design and test approach of the CPSoC is uniform, thus enabling a common fault-management strategy.

VII. Conclusions

In safety-critical systems, like in automotive, designers increasingly use analogue front-ends in combination with many-processor core CPSs. We have shown the design of a dependable four-processor CPSoC for Imminent Collision Detection in cars. This paper deals with the design of highly dependable analogue front-end IPs, with no down-time, by using several embedded instruments interconnected by an IJTAG infrastructure. First, the effect of aging has been shown in a sensor, an OpAmp and a SAR-ADC. Two IJTAG-compatible EIs have been presented, an offset voltage and a delay embedded instrument. The EI designs and IJTAG infrastructure have been verified by simulation. By our proposed method, we have now a uniform approach for the digital and analogue/mixed-signal IPs, and a streamed fault-management technique for both. The lifetime has been significantly increased.

Acknowledgments

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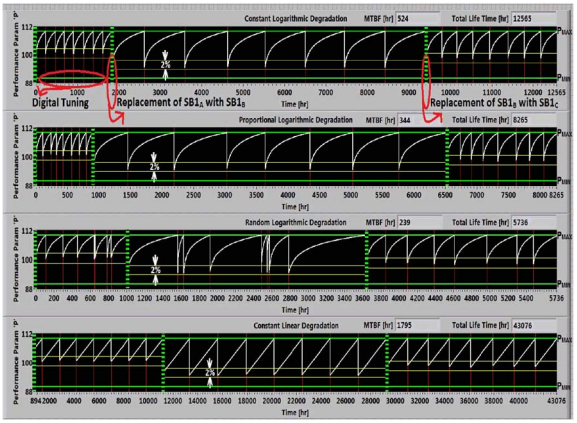

Figure 9. LabView simulations of a redundant and digital IP recalibration for highly dependable mixed-signal CPSoC. Results show four different degradation scenarios.

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