A Digital Sine-Weighted Switched-Gm mixer for Single-Clock Power-Scalable Parallel Receivers

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Abstract— **This paper presents a mixed A/D architecture for parallel channelized RF receiver applications. Its power consumption scales with the number of active receivers and hence with the available overall data rate. A digital sine-weighted switched-Gm mixer with a DDFS per channel is proposed as a zero-IF mixer. The DDFS of all channels are programmable via a Look up Table and are driven by a single central clock. Each channel also exploits a 2-path filter to increase selectivity and interference robustness. To demonstrate the concept two parallel receivers were implemented in a 28nm UTBB FD-SOI CMOS, with 9.5mW/receiver, achieving 40dB of dynamic range, 13dB NF and better than 75 dB inter-receiver isolation.**

Keywords—Parallel receivers, Mixer-DAC, Direct Digital Frequency Synthesis, Harmonic rejection, N-path filter, low power CMOS design, scalable power consumption.

I. INTRODUCTION

During the last decade, a trend has been to integrate ever more concurrently working parallel RF receivers on the same chip. This has been initiated with TV cable tuners in the 50-1000MHz range, and is now a key feature for several applications, such as carrier aggregation for 4G cellular communications, channelized satellite receivers and upcoming 5G applications. When implemented using traditional analog TV tuners, the two key challenges related to the wide bandwidth are: clean LO-generation for multiple simultaneous frequencies and harmonic mixing. In [1], the LO-generation problem was addressed by combining Direct Digital Frequency Synthesis (DDFS) exploiting a DAC and band-pass filter in the reference path of each PLL. For rejecting harmonics, a Harmonic Rejection Mixer (HRM) along with an RF tracking filter were implemented. Each tuner requires its own PLL and inductor VCO, so that many parallel analog tuners would take a lot of chip area, while also introducing interference issues between the different uncorrelated frequencies.

Digitizing the whole spectrum, also known as Full Spectrum Capture (FSC) [2], moves the channel selection and processing to digital. It allows a high number of received channels on the same chip, while only one clock is required. However, this solution puts a heavy burden on the ADC and digital signal processing, leading to a high power consumption. Moreover, the ADC power consumption is fixed and high as it always samples the entire band, even if only a few channels are needed, which is the case in many use scenarios. If the spectrum is continuous and at a rather low frequency (such as cable TV in
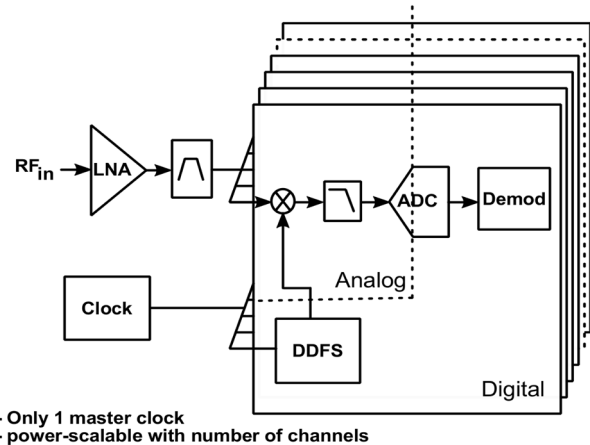

Figure 1: DDFS-based power-scalable and duplicable receiver.

the 50-1000MHz band), FSC may still be effective, but it becomes unpractical and inefficient when the spectrum becomes sparse or when only a few channels are needed. A more power efficient and power-scalable solution is wanted, fitting to a range of data demands, while also addressing the problem of multiple clock generation and interference between the channels.

The architecture we propose in this paper relies on a single central clock that drives the DDFS of each channel (see fig. 1), similar to [3]. However, our focus is on upcoming multi-channel moderate performance (~40dB dynamic range) parallel reception applications, whereas [3] targets a traditional >60dB dynamic range TV application (>60dB worst case Harmonic rejection with a 10 bits DDFS). Our goal is to demonstrate that the solution in fig. 1 is efficient compared to FSC, as its power dissipation scales with the number of received channels. Moreover, it is different from [3] at circuit level to make it more power efficient. Due to the relaxed dynamic range and harmonic rejection constraints, an 8-bit DDFS plus mixer-DAC is sufficient, which can be realized compactly at low power (relaxed component mismatch requirements). The spectrum is split in channels of 5-50MHz, so that power efficient ADCs with <10fJ/conversion can be used, allowing for a few times oversampling and relaxed baseband filtering (<3rd order), while

the ADC consumption can still be below 1mW for a 100MS/s 10bit ADC [5].

The target of this paper is to demonstrate that multiple I/Q receivers including DDFSs and mixer-DACs can be realized with a single master clock, at <10mW/Channel with a channel dynamic range >40dB, which will be sufficient for many upcoming applications. To demonstrate the parallel receiver potential, we have integrated two receiver chains to test mutual interference, and have exploited FDSOI 28nm technology for the design, as it has low power signal processing capabilities and good MOSFET characteristics even at short channel lengths.

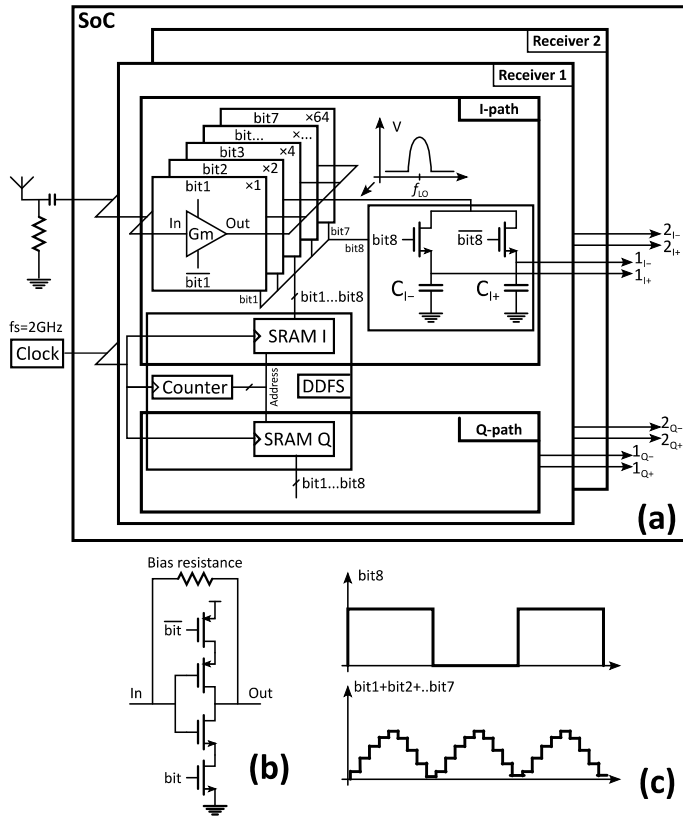## II. MIXER-DAC IMPLEMENTATION

Figure 2: implemented parallel two-channel receiver (a); unit Gm slice with bias resistance (b); SRAM data (c)

Fig. 2(a) presents the proposed implementation of the mixer-DAC. It exploits 7 binary scaled transconductances that are all driven by the same RF-voltage (node In), while summing their currents at the output. An 8th bit directs the output current to either the 1_{I+} or 1_{I-} output, i.e. as a sign bit (see below). The output current is thus the product of the analog input voltage and the digital code (DDFS output) that varies over time as a sampled walking sinewave, realizing a multiplying-DAC behavior. The DDFS is implemented here just by an SRAM and an address counter clocked by a single central clock. There is no regular output DAC, as in a traditional DDFS, but instead this

DAC is merged with the mixer, i.e. it acts a multiplying DAC. The mixer essentially is single ended simplified version of the switched transconductor mixer proposed in [6], with binary weighting added.
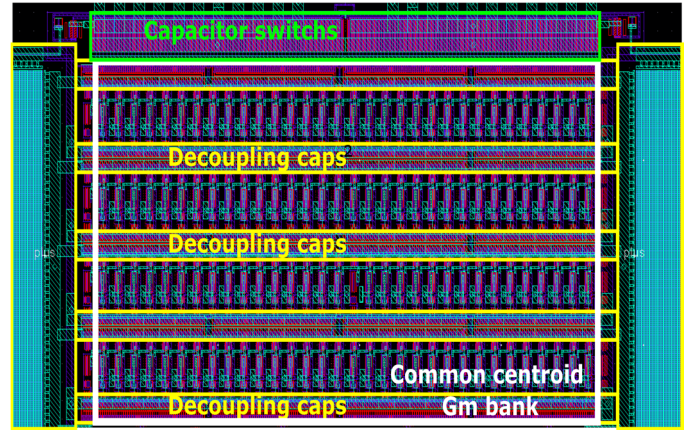

Figure 3: 7 bits Gm-DAC common centroid Gm bank layout including 127 unit gm blcok and decoupling capacitors

This weighting is implemented putting identical switched-Gm mixer slices in parallel, one Gm slice is shown in fig. 2(b). If enabled, it operates as a linear and low noise CMOS inverter-transconductor, which has favorable properties like high linearity, class-AB behavior and current re-use. bit and $\overline{\text{bit}}$ are switched between VDD and ground, allowing for low switch-resistance regardless of the RF-input signal. To minimize power, a single ended switched transconductor is used, but a differential output voltage is created, similar to what happens in a single balanced analog mixer. The differential load impedances consist of two capacitors, C_{I+} and C_{I-} connected to the 1_{I+} and 1_{I-} baseband outputs. Intuitively, bit 8 can be seen as a sign-bit but also as the LO-signal of a mixer or chopper, see fig.2 (c). Indeed, this switch acts like a chopper for the flicker noise of the Gm-blocks. Moreover, the two switched capacitors act like an N-path band pass filter [4], i.e. they present a high impedance to the Gm at the channel-dependent switching frequency of bit 8 and a low impedance elsewhere. Only the wanted signal therefore develops significant voltage swing at the output of the Gm blocks. This improves the robustness of the receiver for other interfering channels non-linearity. To improve the out-of-band signal shunting to ground, a low switch resistance is wanted, thus the bit 8-transistors are large. However, as their output is at baseband, and the parasitic capacitance is in parallel to big baseband capacitors, this is not problematic.

The number of DAC bits affects the theoretical maximal output SNR, i.e. $\text{SNR}_{\text{out}} = 6.02\,N + 1.76$ dB, 49.9 dB for an 8 bits DAC. Two parallel tuners receiving two uncorrelated frequencies were implemented. The DDFS concept allows to create any LO frequency compliant with Nyquist theorem from a single central clock: fs>2fmax (fs=2GHz in our case).

To have experimental freedom to try different waveforms, we implemented a rather big 64Kb SRAM in this demonstrator. To reduce mismatch, we used a common centroid layout for the Gm bank (fig. 3), Gm dummies and a set of decoupling capacitor

rows between each two Gm rows. To reduce clock phase mismatch between the different DAC cells, a balanced clock tree is used, For I/Q phase mismatch reduction, one counter was used to address both the I and Q SRAMs, and only one driver is used to drive both the I and Q clocks. A serial to parallel interface was used to set SRAMs data. Input matching was realized through an external matching resistance.

III. Measurements

The presented measurement results are at PCB connector level and thus include losses and noise coming from PCB and off-chip matching-resistance and using an external clock of 2GHz. Fig.4 shows the measured gain versus LO-frequency. It drops gradually from 33dB at 0.1GHz to 23dB at 1GHz due to charge sharing between the baseband capacitors and the parasitic output capacitance of the Gm-blocks, the NF increases accordingly from 7dB at 0.1GHz to 13dB at 1GHz.
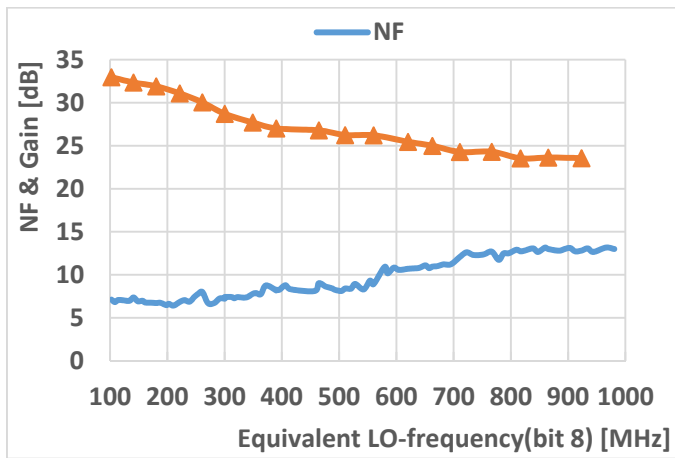

Figure 4: measured NF and conversion gain versus equivalent LO-frequency (bit 8), for a constant IF-frequency=500kHz

In fig. 5 the NF and gain versus IF-frequency is depicted. Thanks to the 8th bit chopping, the flicker noise corner frequency is measured at 20kHz instead of the usual hundreds of MHz in short length technologies such as 28nm FDSOI. The 1st order Gm-C low pass filtering shape is also depicted in the same figure, with a 3MHz cut off frequency, as expected for a 100pF baseband capacitor and 3.7mS average Gm. Harmonic Rejection Ratio (HRR) remains above 41dB for the 100MHz-1GHz spectrum band, as shown in fig. 6. Fig. 7 shows the IIP3 versus offset frequency: it varies from +2 dBm for 6MHz offset, to +16 dBm for 900MHz offset, which bears out the Gm linearity enhancement due to N-path filtering, mentioned earlier. The inter-receiver LO coupling rejection, versus the difference between the two receivers' bit8 frequencies is shown in fig.8, Rx1 LO (LO1) was set to 100MHz and Rx2 LO (LO2) to 100MHz+Δf. Two tones were set at RF input: fin1 at LO1+80kHz and fin2 at LO2+90kHz. The rejection ratio is then the ratio between the output signal of Rx1 at 80kHz and the output of the same receiver at 90kHz that is down-converted due to the coupling of LO2 to Rx1.

The inter receiver LO coupling rejection shows a better than 75dB rejection. That, combined to the use of a single central clock, makes the proposed solution potentially suitable for parallel reception, and demonstrator performance/consumption can be extrapolated to an N-parallel tuner.

Table.1 compares the demonstrator to the state of the art receivers for the same frequency range. The achieved noise figure is in the same range than for others, but as expected/targeted the clean dynamic range is less (roughly >40dB versus >60dB for others) to reduce power consumption. Each I/Q receiver consumes 9.5mW: 5mW for analog (Mixer DAC plus drivers) and 4.5mW for digital (SRAM plus counter), which is 26x-34x lower than for the high performance designs. Note that this power dissipation scales with the number of active channels, while for FSC the 300mW is always needed (for the ADC power alone!). Hence, our proposed solution is certainly more power efficient up to a certain limit (here 26 channels). However, the exact break-even point depends on factors like required dynamic range, ADC energy efficiency and peak-to average ratio considerations, and is subject of a further work.
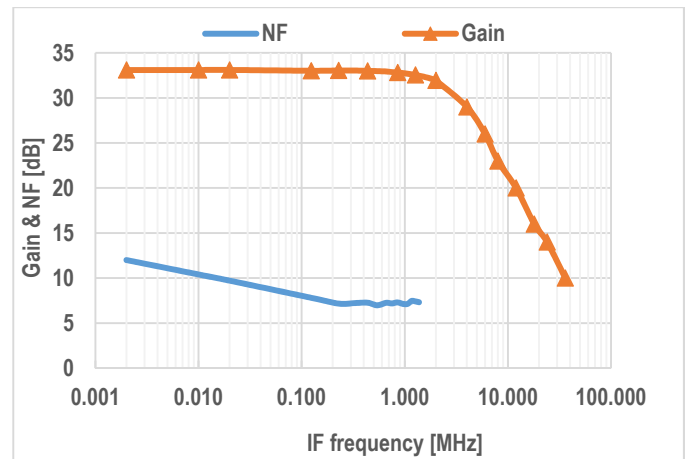

Figure 5: measured NF and conversion gain versus IF frequency at constant equivalent LO-frequency(bit 8) =100MHz
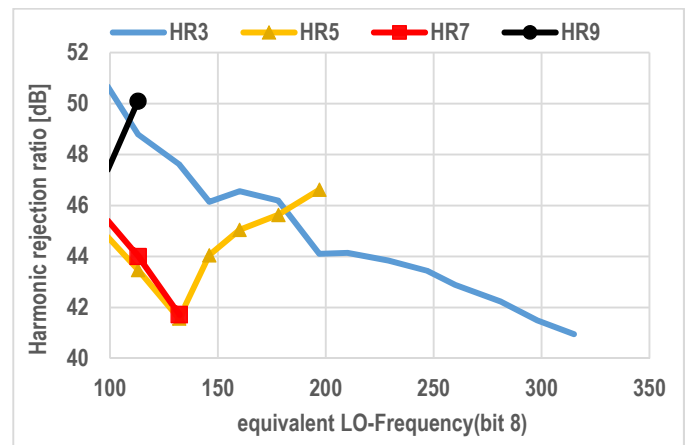

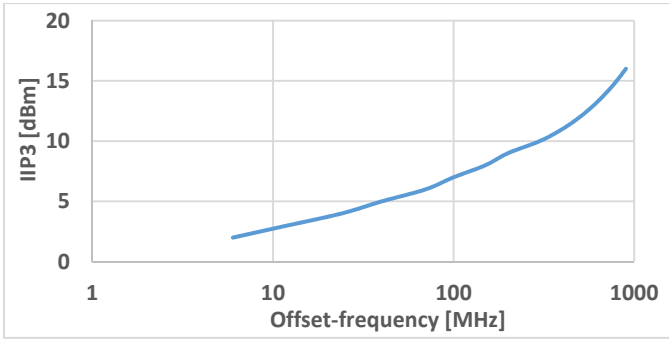Figure 6: measured harmonic rejection ratio: 3rd, 5th, 7th and 9th harmonics

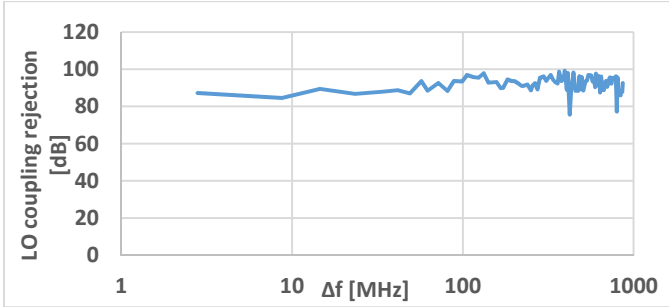Figure 7: measured IIP3, versus offset frequency f1=fLO+1/2*delta-f+fIF and f2=fLO+delta-f+fIF

Figure 8: measured rejection of Rx2-fundamental coupling to Rx1. Rx1 LO (LO1) was set to 100MHz and Rx2 LO (LO2) to 100MHz+Δf. Two tones were set at RF input: fin1 at LO1+80kHz and fin2 at LO2+90kHz. The rejection ratio is then the ratio between the output signal of Rx1 at 80kHz and the output signal of the same receiver at 90kHz that is down-converted due to the coupling of LO2 to Rx1

	This work	[1]	[2]	[3]
Architecture	low IF mixer DAC	low IF mixer	Full spectrum Sampling	low IF mixer DAC
Frequency range [MHz]	100-1000	48-1000	48-1000	48-1000
Number of channel	2	2	158	1
Power Consumption [mW]	19*	650	300**	450
Power Consumption /Channel [mW]	9.5*	325	1.9**	450
Scalable power consumption	yes	yes	No	yes
Gain [dB]	23-33	-	-	-
IIP3 [dBm]	2-16	-	-	20
NF [dB]	7-13	5-7	25.4(W/o LNA, W/ digital)	13
HRR [dB]	41<....<51	65 (with RF tracking Filter)	-	60
Image Rejection [dB]	42	62	70	65
Second receiver spurs on receiver1 rejection [dB]	<-75	-	-	-
Total Die area [mm²]	1	10	1	1.2
IC Technology	28nm FDSOI	65nm CMOS	28nm CMOS	0.13um CMOS

* including digital DDFS

**only ADC power consumption (W/o LNA nor digital)

Table 1: Comparison table, with multi-channel receivers

IV. Conclusion

This paper motivates and demonstrates an architecture to realize power efficient reception in channelized receivers using only one central clock. Unlike Full Spectrum Capture, the power consumption is not constant, but scalable with the number of channels and hence with total data-rate. The architecture exploits a digital sine-weighted switched-Gm Mixer-DAC for power efficiency, followed by current mixer with embedded 2-path filter for improved interference robustness and low 1/f noise. The digital sine is generated via a look-up table that drives the Mixer-DAC. Two 6MHz receiver channels are realized on a demonstrator chip covering 100-1000MHz, achieving 23-33dB Gain, 7-13dB NF, >42 Image Rejection, >41dB worst case Harmonic Rejection, and better than <-75dB cross-talk spurs between the channels. Each channel consumes <9.5mW, 5mW for analog and 4.5mW for the SRAM and counter (digital sine generation). This makes the solution suitable for power critical applications with variable data-rate requirements.
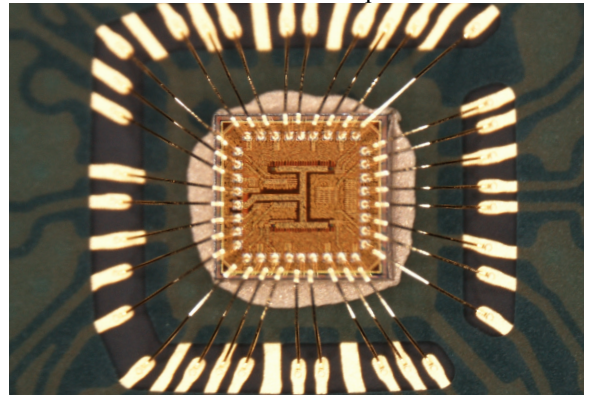

Figure 9: 1 mm² Die micrograph of the implemented two parallel tuners.

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