Perimeter effects from interfaces in ultra-thin layers deposited on nanometer-deep p^+n silicon junctions

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Abstract - Interface states at metal-semiconductor or semiconductor-semiconductor interfaces in ultra-thin layers deposited on nanometer-deep p^+nsilicon junctions that are contacted by metal, can be beneficial for suppressing the injection of majority carriers from the bulk. The effect is more pronounced as the p^+n junction depth becomes smaller and it dominates the electrical characteristics of ultrashallow junctions, as, for example sub-10-nm deep pure boron (PureB) diodes. The properties of the perimeter of such an interface play a critical role in the overall electrical characteristics. In this paper, a TCAD simulation study is described where nanometer-deep p^+n junctions have an interface hole-layer that forms an energy barrier at the semiconductor-semiconductor interface. The suppression of bulk electron injection is analyzed with respect to the barrier height and the p^+n junction depth. Perimeter effects are investigated by 2D simulations showing a detrimental impact on the parasitic majority carrier injection from the bulk in structures with nanometer deep p^+n junctions. Other than employing a guard ring, reduction of the perimeter effects by shifting the position of the metal electrode was considered.

I. INTRODUCTION

The properties of metal-semiconductor or semiconductor-semiconductor interfaces define the electrical characteristics of many semiconductor devices. An example is given bymetal-semiconductor devices where the Schottky-barrier height is solely defined by the atomic structure of the interface [1], [2]. Bipolar transistors with a polysilicon (poly-Si) emitter also make use of the interfacial properties of the poly-Si/Si transition for suppressing the minority carrier (hole) injection from the base into the emitter[3] and increasing the current gain. In poly-Si emitters, the physical mechanisms governing the minority carrier transport are mainly affected by the formation of a thin oxide layer at the poly-Si/Si interface or the recombination of the minority carriers via interface states for devices without a deliberately grown oxide layer [4]. On the other hand, the hetero-emitter-like behavior of phosphorus doped poly-Si emitters is exploited to form a barrier both in the valence and conduction band which can suppress the hole injection from the base[5]. Apart from a band offset, in heterostructure devices the interface states can be filled with electrons or holes thus bending the band significantly [6], [7]. Other mechanisms which impact the carrier transport and where the interface can play a role include tunneling to and from interface states and tunneling through barriers formed at the interface[8].

It can be assumed that the interface properties in the pure amorphous boron (PureB) devicesare responsible for the exceptional electrical characteristics of these devices.A potential barrier at the PureB/Si interface is formed due to an interface hole-layer [9] and suppresses the electron injection from the bulk.While being CMOS compatible [10], the PureB deposition technology allows the formation of a nanometer-deep p^+n junctions [11]. Such a shallow p^+n junction depth is expected to suffer from a large electron injection from the bulk, which would increase the saturation current density to the values larger than 10^{-14} A/μm^2, as found in Schottky-like devices [12]. However, in PureB diodes the saturation current density is measured to be lower than 10^{-19} A/μm^2[10], [12] and is comparable to the saturation current density of devices with deep-diffused pn-junctions. The presence of an effective blocking mechanism is also confirmed by the high effective emitter Gummel number measured in pnp-transistors where PureB layers are incorporated in the emitter region [10], [12]. The effective blocking mechanism of the PureB layers is a subject of ongoing research, which also yielded the wide-bandgap model of the PureB layer [13]. However, this model is made obsolete since the latest ellipsometry measurements yielded an optical bandgap lower than that of Si with values similar to the ones reported for amorphous boron layers [14], [15].

The efficient suppression of the majority carrier injection from the bulk by an interface blocking mechanism, as is the case for the PureB devices, can be deteriorated by the perimeter effects. Photodiodes fabricated with PureB layers deposited at either 400° C or 700° C without the guard ring (GR) show several orders of magnitude higher currents in the forward regime than the PureB diodes where the GR is added to the periphery [16]. This behavior is also attributed to the inherent properties of the PureB layers and the interface to Si. The PureB/Si interface is terminated at the perimeter, which

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allows a higher injection of electrons. The Al pits cannot be formed at the periphery since it is shown that the PureB servesas a diffusion barrier for pure Al deposition [17]. Moreover, the use of the Al saturated with 1-2 % of Si can completely prevent the formation of the pits.

In this paper, a pure Si test structure is proposed with the interface hole-layer which islocated in a several nanometers deep p^+ region of a p^+n-junction diode. This structure is used to analyze the impact of the perimeter on the potential barrier formed by an interface hole-layer which is responsible for suppression of the electron carrier injection. The impact of both oxide interface charge and the oxide layer thickness on the termination of the interface region at the perimeter is examined. Methods for eliminating detrimental perimeter effects are proposed.

II. Suppression of Electron Injection by an Interface Hole-Layer

The impact of aninterface hole-layer located in the p^+ region of a p^+n-junction diode is analyzed on a pure Si test structure based on the material, geometrical and doping parameters found in PureB devices. The PureB layer can be used as an abundant source for diffusion of boron into the Si and the junction depths from sub-10 nm to several hundreds of nanometersare attainable by controlling the annealing time and temperature[10]. The thickness of the PureB layer is set by the duration of the diborane (B_2H_6) gas exposure and thegrowth rate of the PureB layers is found to be equal to 0.4 nm/min for adeposition performed at 700° C[11]. Depending on the application of the devices, PureB layer thickness is varied between 10 nm and 2 nm, while even the latter allows a complete coverage of the Si surface [11]. The concentration of carriers in the PureB layers is not yet measured, while the concentration of holes in amorphous boron layers fabricated using different deposition techniques is found to vary in the range between 10^{16}cm^{-3}[18]and 10^{18} cm^{-3}[19].Other properties such as bandgap[14], [15], mobility[19] and affinity of the PureB layers are neglected for simplicity and the default Si values are used.

The test structure is defined and simulated in Sentaurus Device [20] TCAD software. In simulations,the p^+region, corresponding to the as-diffused boron, is Gaussian with peak concentration, N_{p+}, at the surface of 10^{19} cm^{-3}andpn-junction depth, y_j, varied between 1 nm and 500 nm defined at a background concentration of 10^{15} cm^{-3}. The interface region is defined between the bulk-Si region and the low-doped top-Si layer which has a fixed thickness, t_{pt}, of 5 nm. The doping of the top-Si layer, N_{pt}, equals 10^{18} cm^{-3} and is set to model the hole concentration measured in amorphous boron layers[19]. The total thickness of the simulated structure is 10 µm. The cross-section of the simulated structure is depicted in Fig. 1 and the doping profile of the structure with y_j = 10 nm is shown for reference. The top-Si/bulk-Si interface is also indicated.

In diodes with shallow p^+n-junctions, the properties of the metal contact such as work-functionare important for the behavior of the device. In our simulations, we usedan aluminum metal contact with work-function of 4.1 eV [20]. The band alignment and the formation of the Al/Si barrier follows the Schottky model for contacts [3] while

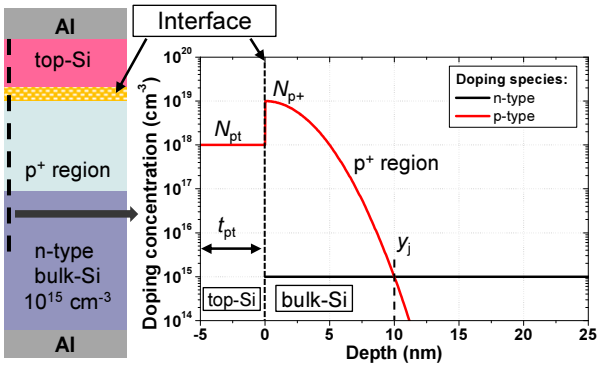


Figure 1. Cross section of a 1D test structure with simulated doping concentration profile.

the thermionic emission model is used to account for the carrier transport over the barriers [20].The simulations are also performed using the Schottky-barrier lowering model, together with the tunneling of the carriers to the anode contact[20]. Fermi-level pinning at the Schottky contact was neglected. For comparison, some of the simulations are performed using an ideal ohmic contact to Si. The electron and hole lifetimes in the Shockley-Read-Hall model equal 10^{-3} s to account for the low saturation current density characteristics typical of PureB photodiodes [10], [12].

A potential barrier for electrons is formed by a negative fixed charge at the interface with concentration N_I. The negative charge attracts holes, which then form an interface layer of holes that bends the band and forms a potential barrier at the interface. In Fig. 2, the band diagram of a device with an Al/Si contact and having a potential barrier formed by a fixed interface charge of$N_I = 5\times10^{12}$ cm^{-2} is compared to the band diagram of the device without this barrier. The band diagram is plotted for the device with $y_j = 10$ nm at forward diode voltage $V_D = 0$ V. For reference, the band diagram of the device with an ideal ohmic contact is also shown. An increase of the potential barrier due to the hole-layer at the interface is clearly seen to be capable of suppressing the electron injection

We analyzed the impact of the parameters of the device such as y_j and N_I on the suppression of the electron

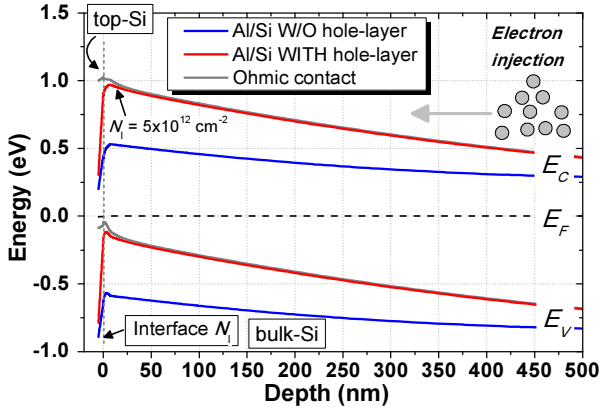


Figure 2. Simulated energy band diagram ($V_D = 0$ V and y_j =10 nm) illustrating the formation of the potential barrier due to the interface hole-layer with $N_I = 5\times10^{12}$ cm^{-2}. Band diagram of the device with an ohmic contact is shown for reference.

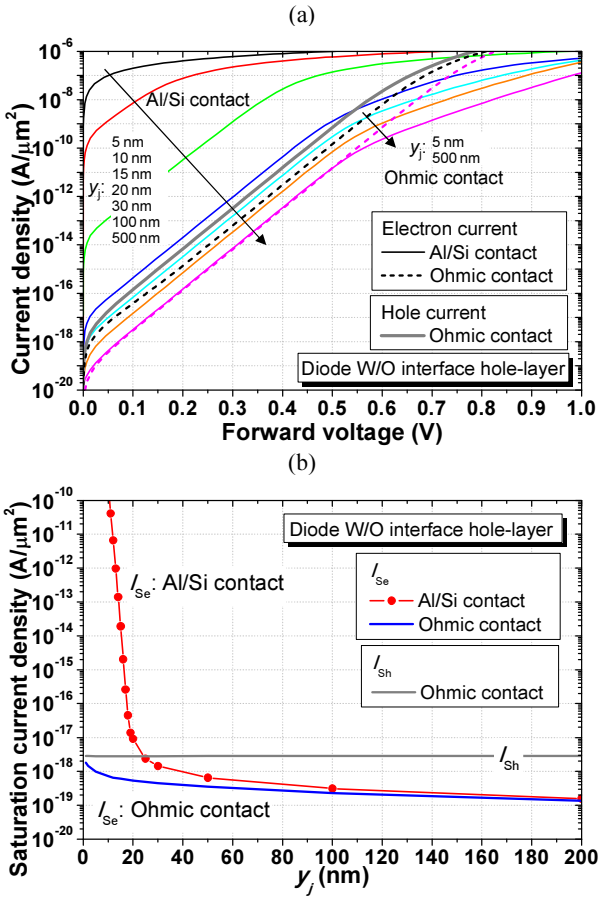


Figure 3. (a) Current-voltage characteristics of the simulated structure for y_j between 5 nm and 500 nm for the device with Al/Si contact and ideal ohmic contact to Si. (b) Extracted electron and hole saturation current density with respect to y_j.

injection by simulating the current-voltage characteristics of the diode. Simulated current-voltage characteristics of the devices with an Al/Si contact without the interface hole-layer (N_I=0) are shown in Fig. 3a. For y_j< 20 nm, the Al work-function lowers the potential barrier for electronsand a large electron current can flow, dominating the total diode current. However, for y_j > 20 nm a barrier is formed which can suppress the electron injection and the diode current is defined by the hole current. For the device where an ideal ohmic contact to Si is defined, there is no impact from the Al work-function and a barrier capable of suppressing the electron injection is formed even for y_j = 5 nm. The saturation current density of both electrons, I_{Se}, and holes, I_{Sh}, is extracted with respect to y_j and is shown in Fig. 3b. For y_j> 150 nm, the I_{Se} of the device with Al/Si contact is equal to the I_{Se} of the device with the ohmic contact to Si.

In the simulatedpure Si test structure, the suppression of the electron injection from thebulk is achieved by introducing a large concentration of holesat the interface. The potential barrier formed in this way can lower the I_{Se} of the diode to become comparable or lower than I_{Sh}. Electron and hole saturation current densities are extracted for devices with Al/Si contacts and anN_I interface charge that is assumed to be at the top-Si/bulk-Si interface. The results are shown in Fig. 4. For the device with y_j = 10 nm, an N_I larger than 6×10^{12} cm^{-2} is needed to lower I_{Se} below

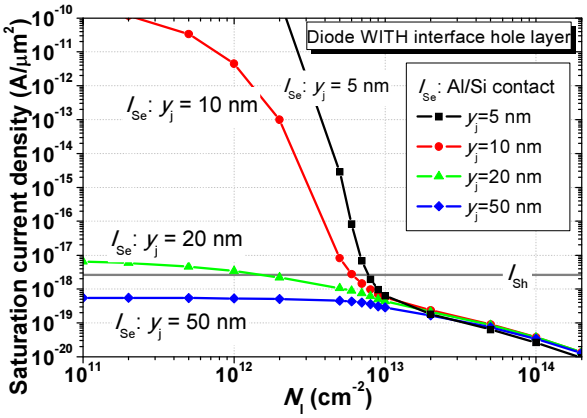


Figure 4. Electron and hole saturation current density for devices with an Al/Si contact with respect to the interface charge concentration responsible for the formation of the potential barrier. Devices with y_j = 5, 10, 20 and 50 nm are shown.

the I_{Sh} values, whereas for deeper pn-junctions, those values are even lower.

III. Impact of Perimeter Effects on the Potential Barrier at the Top-Si/Bulk-Si Interface

In order to study the perimeter effects, we performed 2D simulations in Sentaurus Device [20]. The cross section of the 2D structure is depicted in Fig. 5. The simulated device is 2 μm wide, whereas the intrinsic diode width is set to 1 μm implying that the top-Si layer and the p^+ regionare equally wide. The Gaussian profile of the p^+ region extends laterally with a factor of 0.5. The whole perimeter is covered by oxide with thickness t_{ox}. The part of the top-Si region can also be covered by oxide which is defined by parameter d_{ox}. In this way, the aluminum contact is removed from the edge of the intrinsic diode. The default value ofd_{ox} is 0 meaning that the aluminum covers the whole intrinsic diode region. The concentration of positive oxide interface charge [21]is defined as N_{ox}.

The perimeter effects can impact the potential barrier formed at the interface due to the 2D distribution of charge. Also, if the positive oxide interface charge is located in the vicinity of the interface hole-layer or if the oxide layer is sufficiently thin, electrons are accumulated at the oxide/Si interface. These electrons compensate the charge in the hole-layer thus leading to a decrease of the potential barrier. At the same time, the accumulated electrons form a channel which can steer the electron current towards the already lowered potential barrier thus increasing the electron injection. The electron and hole

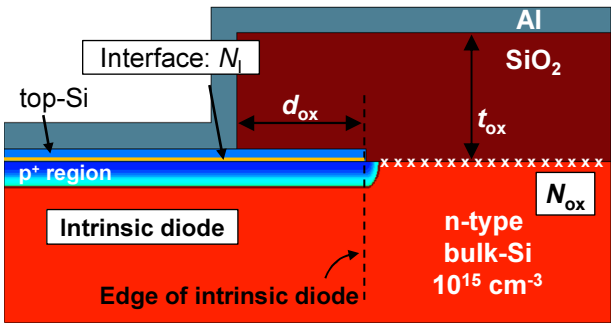
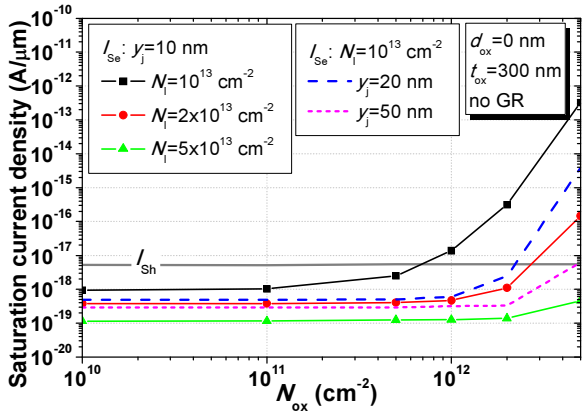


Figure 5. Cross section of a 2D test structure used to analyze the impact of perimeter effects on the potential barrier at the interface.

(a)



(b)

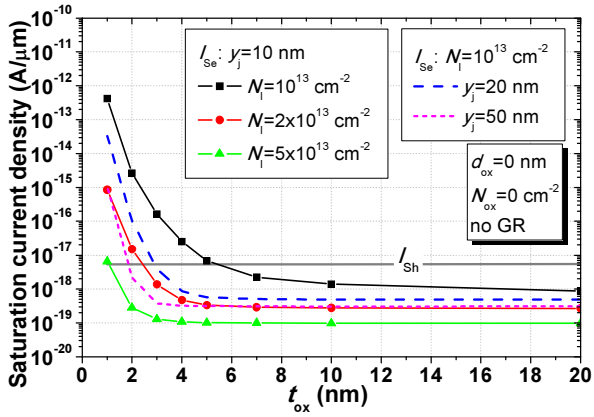


Figure 6. Electron and hole saturation current density of a 2D device for junction depths of y_j = 10 nm, 20 nm and 50 nm and $N_I = 10^{13}$ cm^{-2}, 2×10^{13} cm^{-2} and 5×10^{13} cm^{-2} with respect to (a) oxide/Si interface charge, N_{ox} and (b) oxide thickness, t_{ox}.

saturation current density for junction depths of y_j = 10 nm, 20 nm and 50 nm and $N_I = 10^{13}$ cm^{-2}, 2×10^{13} cm^{-2} and 5×10^{13} cm^{-2} with respect to the oxide/Si interface charge, N_{ox} is shown in Fig. 6a. The impact of the oxide thickness on I_{Se} and I_{Sh} for the same y_j and N_I is shown in Fig. 6b. For the device having y_j = 10 nm and $N_I = 10^{13}$ cm^{-2}, the perimeter effects start to considerably increase I_{Se} for values of $N_{ox} > 7\times10^{11}$ cm^{-2} or $t_{ox} < 5$ nm which can then dominate the diode current.The lowering of the barrier due to the perimeter effects is analyzed by plotting the band diagram of the intrinsic diode and the band diagram at the edge of the intrinsic diode, which is shown in Fig. 7. The barrier lowering, ΔE_B, for the simulated device with parameters indicated in Fig. 7 is found to equal 0.17 eV. In reality, both the oxide/Si interface charge and thin oxide participate in deteriorating the barrier at the perimeter of the device, while the 3D effects found at the sharp corners of devices with rectangular layout can further decrease the barrier.

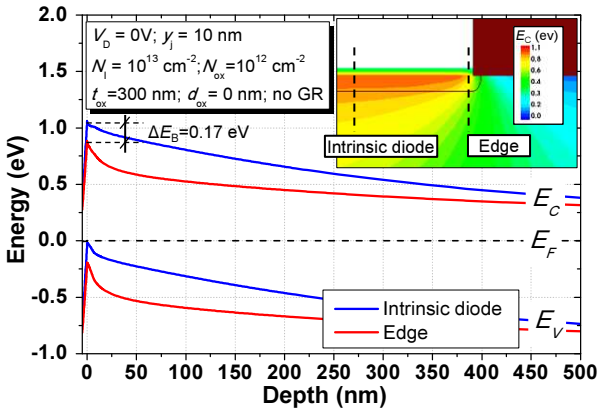
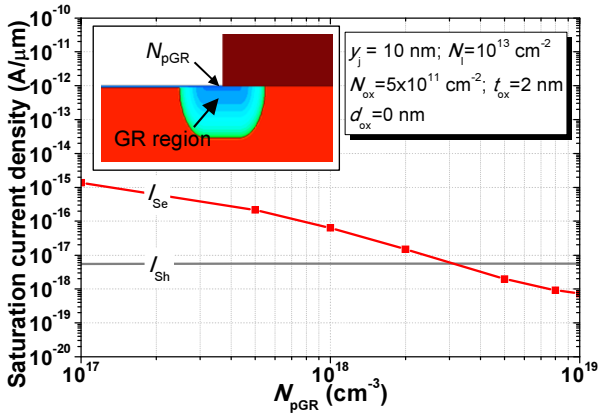


Figure 7. Band diagram of the intrinsic diode and at the edge of the intrinsic diode region indicating a lowering of the potential barrier.

Elimination of the perimeter effects is performed by means of GR formation at the edge of the intrinsic diode or by increasing the distance between the aluminum contact and the edge of the intrinsic diode. Both methods can lower the increased electron saturation current density. In our simulations, the GR region has a Gaussian doping profile with the junction depth of y_{jGR} = 300 nm defined at a bulk doping concentration of 10^{15} cm^{-3}. The Gaussian profile extends laterally with a factor of 0.5. The peak concentration of the GR region, N_{pGR}, is located at the surface (y=0 nm). The impact of the N_{pGR} on successful elimination of the perimeter effects is analyzed and shown in Fig. 8a. The 2D device is defined having y_j = 10 nm, $N_I = 10^{13}$ cm^{-2}, $N_{ox} = 5\times10^{11}$ cm^{-2}, t_{ox}=2 nm and d_{ox} = 0 nm. The results show that the peak surface concentration of such a GR region needs to be higher than 3×10^{18} cm^{-3} in order to efficiently decrease I_{Se} to be lower than I_{Sh}. On the other hand, increasing the distance between the aluminum contact and the edge of the intrinsic diode lowers the I_{Se} significantly. The aluminum sink electrode, which originally decreases the barrier for electrons in

(a)



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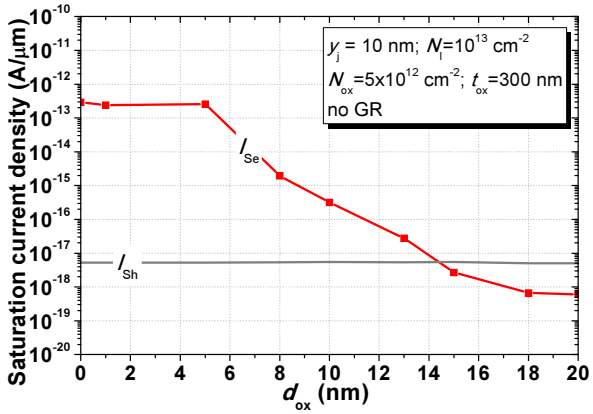

Figure 8. Electron and hole saturation current density of a 2D device with respect to the (a) peak concentration of the GR region; (b) distance between the aluminum contact and the edge of the intrinsic diode, d_{ox}.

devices with nanometer deep pn-junctions is thereafter moved away and is not subjected to the perimeter effects. The extracted I_{Se} and I_{Sh} for a device with y_j = 10 nm, N_I = 10^{13} cm^{-2}, N_{ox} = 5×10^{12} cm^{-2}, t_{ox}=300 nm and no GR region are shown in Fig. 8b. The parameter d_{ox} for which I_{Se} is lower than I_{Sh} needs to be larger than ≈15 nm. This also sets the lower limit at which the perimeter effects can efficiently be suppressed.

IV. CONCLUSION

In this paper, we analyzed the impact of a layer of holes at an interfacelocated in the p^+ region of p^+n-junction diodes on the suppression of electron injection from the bulk. The layer of holes causes the formation of a potential barrier capable of reducing the otherwise large electron saturation current density found in devices with Al/Si contacts having a shallow pn-junction depth lower than 20 nm. For a device with an Al/Si contact with a junction depth of 10 nm and the thickness of the top-Si layer of 5 nm, an electron saturation current density lower than 10^{-18} A/μm^2 can be achieved for an interface hole-layer with a concentration larger than 6×10^{12} cm^{-2}.

The perimeter effects in devices employing a layer of holes can have detrimental effects on the suppression of the electron injection. Both interface oxide charge and thin oxide layers can lower the potential barrier and form a channel at the oxide/Si interface steering the electrons toward the lowered barrier at the edge of the intrinsic diode. These perimeter effects can be even more pronounced at the edges ofdevices having a circular or rectangular layout due to 3D effects. In the devices where a GR is employed, the perimeter effects can be efficiently suppressed. In this paper the peak doping concentration of the GR needed to suppress these effects for the simulated structure is found to be larger than 3×10^{18} cm^{-3}. At the same time, if part of the intrinsic diode is covered with oxide thus increasing the distance between the aluminum contact and the perimeter, the perimeter effects can be eliminated. The distance that the aluminum contact must be shifted with respect to the edge of the intrinsic diodecan be as low as 15 nm.

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