Thin-Film Layers with Interfaces that reduce RF Losses on High-Resistivity Silicon Substrates

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***Abstract*—Radio-Frequency (RF) losses on High-Resistivity Silicon (HRS) substrates were studied for several different surface passivation layers comprising thin-films of SiC, SiN and SiO_2. In many combinations, losses from conductive surface channels were reduced and increasing the number of interfaces between thin-films was found to be beneficial. In some cases the surface losses were completely eliminated. For example, with plasma-enhanced chemical-vapor deposition (PECVD) α-SiC layers up to a few tens of nm thick and exposed to nitridation or SiN growth at 850ºC to form a SiC:N interface layer, values for the total losses of 1.6 dB/cm were achieved. Analysis of these layers was performed by using temperature dependent measurements of the RF losses on Coplanar Waveguides (CPWs), the capacitance-voltage characteristics and the sheet resistance along the Si surface. The overall results can be explained by assuming that the thin-films are so defected that they allow vertical current paths to highly-resistive interface layers where both fixed and mobile charge can be stored.**

Keywords— capacitance-voltage measurements, high-resistivity silicon, interface, nitidation, RF losses, sheet resistance, SiC, SiN, temperature dependence, thin-film

I. INTRODUCTION

Crystalline high-resistivity silicon (HRS) substrates are nowadays routinely used for radio-frequency (RF) circuits and microwave Coplanar Waveguide (CPW) transmission lines due to the low cost and wide availability. While the bulk HRS substrate contains very few charge carriers, surface channels limit the performance. To suppress such parasitic conduction losses, several passivation techniques have been developed including argon implantation [1], poly- [2] or amorphous-Si deposition [3], and combinations with specially designed Rapid Thermal Processing (RTP) treatments [4] to improve thermal stability of the passivating layers. With these methods the charge carriers that gather at the Si interface in inversion or accumulation layers are forced to move in a layer of disordered Si that has very high resistivity.

In this paper, we examine combinations of SiC, SiN and SiO_2 layer stacks deposited by chemical-vapor deposition (CVD) as passivation layers on HRS. In earlier work [5, 6] it was shown that all these layers have a beneficial effect with respect to reducing surface-channel losses as compared to thermal oxide layers. Except for the SiC layers, they are all routinely used in standard (Bi)CMOS processes. However, integration of SiC as an RF passivation layer in a bipolar process has been demonstrated [7]. For the layers studied in this paper, far the best results were achieved with thin layers of nitridated plasma-enhanced CVD (PECVD) SiC layers, less than 50 nm thick, coated with another insulating dielectric layer. On the basis of measurements of the RF losses and the sheet resistance R_{SH} along the conducting surface channels, it was concluded that surface currents are completely conducted away from the Si to flow along the nitridated SiC surface. The presence of SiC:N compounds suggested a possible n-doping by nitrogen, thus changing the surface from an insulating to a highly resistive layer.

In addition to RF losses and the R_{SH}, the layer stacks were also studied here by applying *C-V* measurements. From the overall results, conclusions are drawn on which mechanisms are responsible for the very efficient suppression of parasitic surface currents.

II. DEVICE FABRICATION

The HRS substrates were p-type 100-mm (100) wafers with a resistivity of 2-4 kΩcm. Regions for substrate contacting and the source/drain of the MISFET ring structures were implanted through 30 nm oxide and annealed at 900ºC. This oxide was removed before deposition of a variety of layer stacks containing combinations of thermal oxide, PECVD and low-pressure (LP)CVD SiO_2, LPCVD SiN, and PE- and LPCVD SiC. Two qualities of thermal oxide were used: a 30-nm-thick insulating gate-quality oxide and poor quality oxide that was leaky at this thickness. The LPCVD SiN was a low-stress Si-rich SiN deposited at 850ºC. The PECVD SiC was deposited at 400ºC. The resistivity of our SiC was in the 10^{13} Ωcm range [6]. Both the PECVD and LPCVD SiC layers were studied in [6] where it was found that the deposited LPCVD SiC layer is polycrystalline and the PECVD layer is amorphous. Instead of depositing SiN on the SiC, some of the SiC depositions received a nitridation by exposure to NH_3 at 850ºC to form a SiC:N interface layer. After the layer-stack depositions, contact windows were etched and an Al/Si(1%) metallization was sputtered and patterned by plasma etching. The processing is completed by an alloy in forming gas at 400 ºC.

III. MEASUREMENT TECHNIQUES

The RF losses were determined by S-parameter measure-

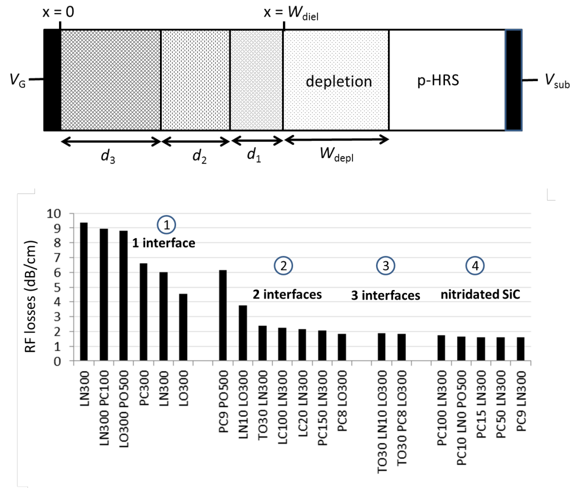

Fig. 1. Top: Schematic of a dieletric stack with 3 layers of thickness d_1, d_2, and d_3. Bottom: Compilation of the maximum RF losses at 30 GHz of a variety of different layer stacks belonging to the groups (1) to (4) decribed in the text. Nomenclature: P = PECVD, L = LPCVD, C = SiC, N = SiN, O = SiO_2, the number indicate thickness in nm.

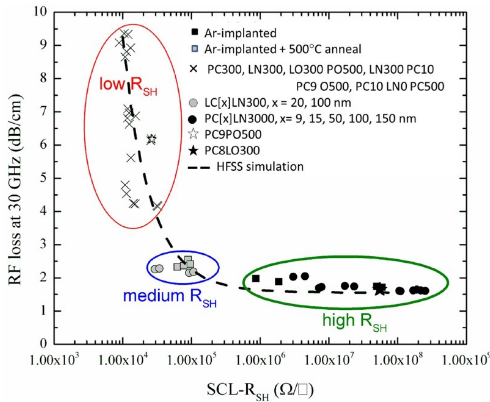

Fig. 2. Measured RF losses at 30 GHz as a function of R_{SH} for samples with Ar^+-implanted Si and/or layer stacks composed of different combinations of SiC, SiN, and SiO_2, together with HFSS simulation results; taken from [5].

ments on CPW transmission lines for substrate biasing up to 75 V. The length of the CPW transmission lines was 0.95 cm, the width of the ground planes 400 µm, the signal line 50 µm and the slot gap 23 µm. The CPWs were designed with a characteristic impedance of 50 Ω. Direct information on the current flows along the surface were extracted from *I-V* measurements on ring-gate MISFET test structures for gate voltages, V_G, from 0 to 25 V. The use of these structures for the extraction of the R_{SH} of inversion-layer currents along the Si surface is described in detail in [9, 10]. The drain was swept in steps of 50 mV to stay in the linear part of the output resistance. Additionally, HFSS simulations [11] were executed at 30 GHz frequency with the R_{SH} as an input parameter to verify the experimental results.

The *C-V* measurements were performed on circular Al dots with a diameter of 400 µm using a gate voltages V_G of -10 V to 10 V or -20 V to 20 V when DC leakage currents allowed. A measurement frequency of 30 kHz was found to be low enough to minimize attenuation of the measured capacitance that otherwise is readily caused by the high substrate resistance.

Temperature dependent measurements of the RF losses were performed at 30ºC, 50ºC, 75ºC and 100ºC chuck temperatures with a substrate bias, V_{sub} = 0 , -25 V, -50 V, and -75 V. The DC measurements were conducted on the same wafer using structures that were situated close to each other.

IV. Results and Discussion

The RF losses for a number of layer-stack combinations are compiled in Fig. 1. Four groups are identified, organized from highest to lowest losses:

1) The "1-interface" group is composed of a 300-nm-thick first layer of insulating SiN, SiC, or SiO_2. Losses are from 5 dB/cm to 9 dB/cm. Past work [12] has shown that the density of interface states can be correlated to the losses.
2) The "2-interface" group has a layer-stack of first a thin layer of PECVD/LPCVD SiC or SiN, or poor-quality oxide, that is expected to be leaky, covered by a second deposited insulating layer. Losses of 2 dB/cm to 6 dB/cm were found.
3) The "3-interface" group, has a layer-stack of first 30 nm poor-quality thermal oxide covered by a thin layer of SiC or SiN, all covered by a final layer of LPCVD oxide, resulting in losses of 1.85 dB/cm. This value is lower than the sample from the "2-interface" group that only has a thick layer of SiC or SiN on top of the oxide with losses of 3.75 dB/cm.
4) The "nitridated-SiC" group has a nitridated PECVD SiC (SiC:N), covered by SiN or SiO_2.With a SiC thickness less than 50 nm, the losses are 1.6 dB/cm [5].

A number of these layer stacks were studied in [5] by comparing RF losses to R_{SH}. The results, summarized in Fig. 2, show a fixed relationship between the two parameters. For example, the samples in the nitridated-SiC group had MΩ/sq R_{SH} values. In the work presented here, many of the layers were also examined by *C-V* measurements . All layer stacks, except those in the nitridated-SiC group, displayed a maximum capacitance that corresponded to the expected capacitance of the given dielectric layer stack, C_{diel}. Therefore, it can be assumed that mobile charge is able to gather at or near the Si surface in these cases. In contrast, the nitridated-SiC group the samples had a very low bias-independent capacitance.

To better understand the behavior of the SiC:N layers, the selection of stacks listed in Table I was studied by temperature dependent measurements. In the table the minimum and maximum capacitance, C_{min} and C_{max}, at 30ºC are also listed along with the flatband voltage V_{FB}. The V_{FB} is determined by the metal-semiconductor work function difference Φ_{MS}, any fixed/mobile charge, Q_{diel}, in the dielectric stack, and any interface/dielectric trapped charge. At the Si-dielectric interface the interface traps can be charged and discharged, depending on the surface potential. If the first layer of the dielectric stack is leaky, the second interface between the first and second dielectric layers may also be in electrical communication with the Si surface. Ignoring the role of interface states and assuming only one type of dielectric, the V_{FB} can be calculated

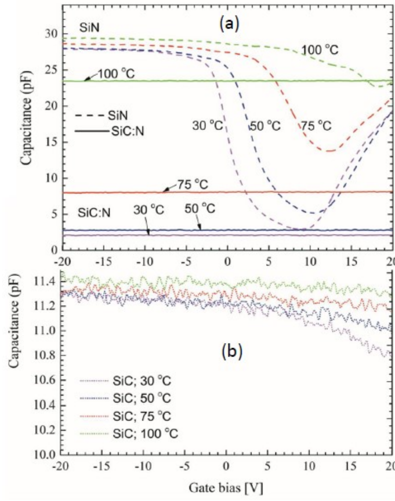

Fig. 3. Measured capacitance as a function of gate bias for samples SiN300 (a), SiC-O500 (b) and SiC:N300 (a); for temperatures 30ºC, 50ºC, 75ºC and 100ºC.

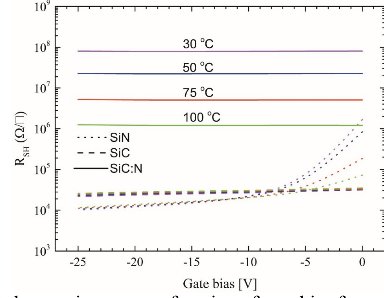

Fig. 4. Measured sheet resistance as a function of gate bias for samples SiN300, SiC-O500 and SiC:N300; for temperatures 30ºC, 50ºC, 75ºC and 100ºC.

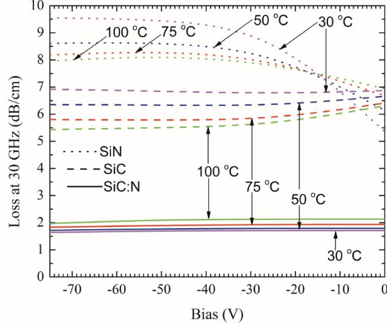

Fig. 5. Measured RF losses at 30 GHz as function of gate bias for samples SiN300, SiC-O500 and SiC:N300; for temperatures 30ºC, 50ºC, 75ºC, 100ºC.

as [13]

$$V_{FB} = \Phi_{MS} - \gamma Q_{diel}/C_{diel} \quad (1)$$

where γ is a weighing factor introduced to account for the charge distribution throughout the dielectric. If all charge is at $x = 0$, i.e., the metal interface, then $\gamma = 0$. For all charge at $x = W_{diel}$, i.e., at the Si interface, $\gamma = 1$. Assuming that all the fixed charge is located at $x = W_{diel} - d_1$ then it will have a large impact for $d_1 = 9$ nm and much less impact for $d_1 = 100$ nm. Moreover, for increasing d_2, i.e., increasing total W_{diel}, the V_{FB} shift will also be decreased.

TABLE I: TARGETED LAYER THICKNESS OF SELECTED LAYER STACKS AND PARAMETERS EXTRACTED FROM C-V MEASUREMENTS AT 30 °C

Sample Name	Layer Stack			C-V data		
	SiC (nm)	*SiN (nm)*	*PECVD SiO_2(nm)*	*V_{FB} (V)*	*C_{min} (pF)*	*C_{max} (pF)*
SiN300	-	300	-	0	3.1	28.4
SiC:N300	9	300	-	< -20	2.5	2.5
SiC-O500	9	-	500	~ 20	< 10.9	11.2
SiC100:N	100	300	-	2.5	2.7	29.3
SiC:N50	15	50	-	- [a]	6.4	- [a]
SiC:N150	15	150	-	< -20	4.6	4.6

[a] not measurable due to high DC leakage current

The temperature dependence of samples SiN300, SiC:N300 and SiC-O300 is shown in Fig. 3 for *C-V* measurements, in Fig. 4 for RF losses, and in Fig. 5 for R_{SH}. In Fig. 3a the temperature dependence at 30°C is compared for samples SiN300 and SiC:N300. The very low, constant capacitance value, $C_{min} = C_{max} = 2.5$ pF, of the SiC:N300 sample lies close to the C_{min} of the SiN300 sample. Moreover, the increase in C_{min} with temperature shows similar behavior for both samples. This behavior is expected for the SiN300 sample that has a standard *C-V* characteristic going from accumulation into depletion and then inversion as V_G increases. When the temperature is increased there is an increase in charge generation in the substrate which increases the rate at which the inversion layer is formed and it becomes difficult to reach full depletion. Hence the depletion width decreases. This is particularly true for HRS substrates that have very long carrier lifetimes. For measurement frequencies much lower than the 30 kHz used in Fig 3a, the fast formation of the inversion layer completely prevents the formation of a depletion layer and information is lost about V_{FB}. For the SiC:N300 sample, a measurement at 10 kHz and 100ºC increases the C_{min} to 29 pF, which is the value of C_{diel}.

From this discussion of how the essentially constant *C-V* curves of the SiC:N300 sample follow C_{min} of the SiN sample, it is concluded that the depletion is being induced by a netto positive charge in the dielectric layers, which would need to be compensated by a negative voltage to reach V_{FB}. No dip is seen in the capacitance up to -20 V, so by assuming that the main source of the V_{FB} shift is positive charge, Q_f, stored at the SiC:N interface, equation (1) was used to calculate that Q_f would then have to be larger than 5×10^{12} cm^{-2}.

The influence of Q_f on V_{FB} will decrease for increasing SiC or for decreasing SiN thickness. Indeed, as seen in Table I, for samples SiC100:N, SiC:N50 and SiC:N150, C_{min} is higher than for SiC:N300. For SiC100:N a clear dip appears in the curves and V_{FB} is shifted to 2.5 V. The SiC:N50 and SiC:N150 samples were quite leaky, limiting the reliable measurement range and inhibiting an exact determination of V_{FB}.

The temperature dependence of the RF losses and R_{SH} follow the same trends as the *C-V* measurements. As can be seen in Fig. 6 they also have the same relationship to each other as the variety of room-temperature measurements shown in

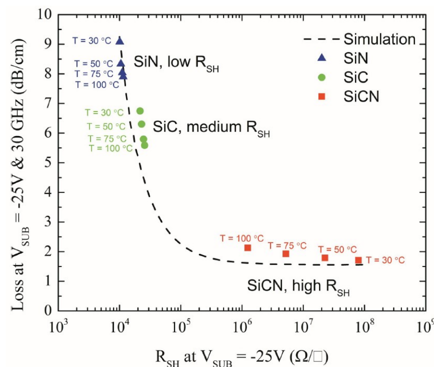

Fig. 6. Measured RF losses at 30 GHz as a function of sheet resistance.

Fig. 2. By comparing Figs. 3, 4 and 5, it becomes clear that there is only bias dependence of both parameters when changes in the depletion width are visible in the *C-V* measurements. It is strongest for the 30ºC measurement of the SiN300 sample in the region 0 to –20 V where almost full depletion is first formed followed by the building up of an inversion layer. The losses increase with temperature when the Si is in depletion but decrease when an inversion layer dominates the surface channel currents. The latter behavior is in contrast to what would be expected from the temperature coefficient α of the resistivity which is normally negative in defect-free lightly-doped c-Si [14]. The proximity of the interface and associated traps can be the reason for nevertheless having a positive α. In contrast, a negative α is found at the voltages where depletion is formed, which can be due to an increasing number of inversion electrons collecting at the Si interface.

For the SiC-O500 sample the losses over the whole voltage range are decreasing with temperature to the same degree as seen for the SiN300 sample. Despite this, the *C-V* curves are almost constant with temperature, only showing a small splitting of the curves at $V_G = 20$ V that could suggest the onset of a transition from accumulation to depletion/inversion. However, a corresponding change in sign of the temperature coefficient does not appear so probably the loss behavior is dominated by surface charge currents over the whole range. The almost voltage independent behavior of the losses and R_{SH} can be caused by a very high interface state density plus some leakage of current to the SiC-SiO_2 interface.

For the SiC:N300 sample, the losses are very low, 1.6 dB/cm at 30ºC, and increase to only 2 dB/cm at 100ºC. This increase is correlated to the decreasing depletion width observed in the *C-V* measurements that is caused by an increase in charge generation in the Si substrate. The effect on the losses can have several causes. Obviously the high R_{SH} indicates that charge is still mainly flowing in the nitridated SiC interface but at the higher temperatures it may have more energy to electrically communicate with the Si interface giving a small current flow along this low resistance path. Changes in sheet resistance of the SiC:N interface itself or the conduction through the SiC layer could also be playing a role.

V. Conclusions

From the many combinations of SiC, SiN and SiO_2 thin-film stacks studied in this paper it can be concluded that an efficient suppression of the RF/microwave surface losses on HRS can be achieved by covering the Si surface with leaky thin-films that can channel the Si surface charge to interfaces between the dielectrics. To achieve such an interface effect, two properties are important: they must be able to store charge that may otherwise accumulate at the Si surface and the sheet resistance along the interface must be high, preferably in the MΩ/sq range. The beneficial suppression of the losses appears to be increased as the number of interface layers is increased. The most efficient combination was found for a first layer of up to 50-nm-thick nitrated PECVD SiC layers. It is probable that the nitridation at 850ºC, either from NH_3 exposure or from SiN deposition, gives an n-type nitrogen surface doping of the SiC. This could well explain the very high positive charge at the nitridated SiC interface whether it is covered with SiO_2 or SiN. The thin SiC:N surface layers had losses of 1.6 dB/cm which is even lower than the 1.7 dB/cm achieved by amorphizing the surface Si with heavy Ar^+ implants [5]. This could be the result of the extra series capacitor across the wide depletion region induced by the positive fixed charge. For temperatures going up to 100ºC the losses increase very slightly to 2 dB/cm, which is correlated to increased charge generation in the Si substrate. This work also makes clear that the R_{SH}, in contrast to *C-V* measurements, is a suitable DC tool for predicting RF losses.

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