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Depletion-mode quantum dots in intrinsic silicon

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We report the fabrication and electrical characterization of depletion-mode quantum dots in a two-dimensional hole gas (2DHG) in intrinsic silicon. We use fixed charge in a SiO_2/Al_2O_3 dielectric stack to induce a 2DHG at the Si/SiO_2 interface. Fabrication of the gate structures is accomplished with a single layer metallization process. Transport spectroscopy reveals regular Coulomb oscillations with charging energies of 10–15 meV and 3–5 meV for the few- and many-hole regimes, respectively. This depletion-mode design avoids complex multilayer architectures requiring precision alignment and allows us to adopt directly best practices already developed for depletion dots in other material systems. We also demonstrate a method to deactivate fixed charge in the SiO_2/Al_2O_3 dielectric stack using deep ultraviolet light, which may become an important procedure to avoid unwanted 2DHG build-up in Si MOS quantum bits. *Published by AIP Publishing.*
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In order to perform sufficient operations in a quantum computer,[1] the quantum bits are required to be long-lived. Group IV semiconductors not only hold promise for very long spin coherence times[2–5] but also may take advantage from the scalability provided by the semiconductor industry. These benefits have attracted much attention[6–11] to quantum dots (QDs) in group IV material systems as a framework for a solid-state scalable spin-based quantum computer.[12] Recently, hole transport in QDs became a subject of particular interest, both experimental[13–19] and theoretical,[20–22] since the hyperfine interaction is strongly suppressed, while the spin-orbit coupling enables all-electrical spin manipulation[23] boosting scalability of hole-based qubits. However, enabled electrical spin control makes them vulnerable to charge noise that leads to dephasing and decoherence of the spin states. Elimination of electrically active defects at the location of the QDs is essential to extend the hole spin coherence time. In Si planar QDs, nanometer-sized Coulomb islands are electrostatically defined in a gated MOSFET-type structure at the Si/SiO_2 interface. The disorder and defects at this interface can be detrimental to the robustness and reliability of hole spin qubits.

A low-temperature ($\sim 400\,°C$), hydrogen treatment is traditionally used to deactivate defects at the Si/SiO_2 interface. One way to implement it is based on hydrogen diffusion during atomic layer deposition (ALD) of Al_2O_3 thin films.[24] We have successfully used this approach recently[25] to improve the quality of silicon QDs. This method can lead to building up of a negative fixed charge Q_f in Al_2O_3,[26] strong enough to induce 2DHG at the Si/SiO_2 interface. Here, we demonstrate a method to neutralize it and give a hint on the mechanism of this phenomenon. Besides, here we utilize Q_f to create depletion-mode QDs in intrinsic silicon.

To show the effect of negative Q_f buildup, we use intrinsic Si ($\rho \geq 10\,k\Omega\,cm$) with predefined ohmic contacts to highly doped p^{++} silicon areas and 7 nm of thermally grown SiO_2 as a substrate. After deposition of 5 nm of Al_2O_3 by thermal ALD (TMA/H_2O, at $T = 250\,°C$) on the substrate, we anneal it in an argon atmosphere (100 Pa, 30 min, $T = 400\,°C$). Figure 1(a) shows a schematic cross-section of the fabricated substrate. Q_f builds up in Al_2O_3 during annealing. Although there is no consensus on its origin, one possible explanation[27] is that the initial growth regime of a

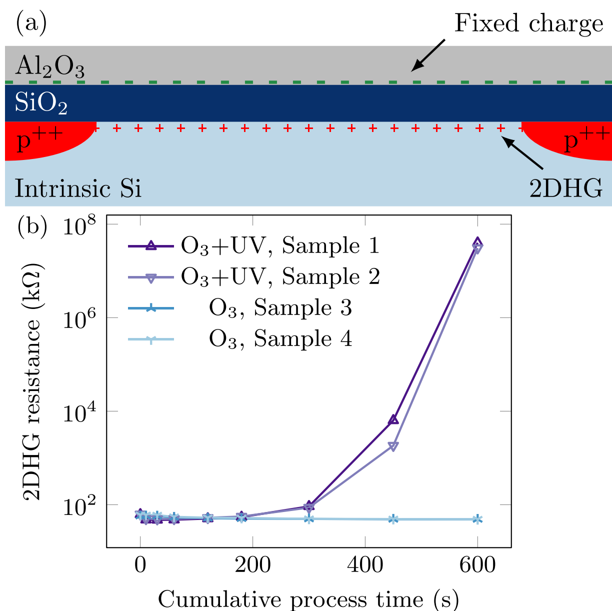

FIG. 1. (a) Schematic cross-sectional view of the device structure. Fixed negative charge in Al_2O_3 deposited by ALD on SiO_2 induces a two-dimensional hole gas (2DHG) at the Si/SiO_2 interface. The highly p-type doped regions are used to measure a resistance of the induced 2DHG. (b) The increase in the resistance of a 2DHG under the influence of UV light and ozone ("△," "▽" symbols). Control samples exposed to ozone ("Y," "⅄" symbols) do not show a significant change in the resistance; measurements are done at $T = 4.2\,K$.

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few first ALD cycles being non-stoichiometric provides an excess of oxygen atoms and deep charge traps at the SiO_2/Al_2O_3 interface. Electrons fill these traps during annealing, providing a net number of fixed charges per unit area in the range[26,27] of 10^{12}–$10^{13}\,cm^{-2}$. This is enough to induce the two-dimensional hole gas (2DHG) at the Si/SiO_2 interface in our devices and short ohmic contacts at temperatures down to a few mK.

Besides using Q_f to create depletion-mode QDs, we also present a method to neutralize it and eliminate the corresponding 2DHG using deep ultraviolet light (UV). We expose annealed samples in a UV ozone generator (wavelength $\lambda_{UV} = 254\,nm$) and measure the 2-point resistance of 2DHG between ohmic contacts R_{2DHG} *ex situ* at $T = 4.2\,K$. Figure 1(b) shows R_{2DHG} after 9 iterative steps of exposure up to a total cumulative process time of 600 s. After exposure to UV light and O_3, two different samples ["△," "▽" symbols in Fig. 1(b)] demonstrate the same behavior. After approximately 10 min of cumulative exposure to UV light and O_3, the R_{2DHG} restores back to the resistance common for intrinsic Si at this temperature. In contrast, two control samples only exposed to O_3 ["Y," "⅄" symbols in Fig. 1(b)] demonstrate a slight decrease in R_{2DHG}. A possible explanation of the observed neutralization is that high-energy UV radiation promotes diffusion of oxygen[28] in Al_2O_3, which improves stoichiometry of the film, eliminating charge traps and the Q_f in it, as well as the induced 2DHG. The results in Fig. 1 show that post-anneal UV exposure is an essential treatment of the enhancement-mode QDs in intrinsic Si, as it allows avoiding short circuits via 2DHG in hole- and ambipolar-QDs.[25,29]

At the same time, we propose below to take advantage of the induced 2DHG. We see that the negative Q_f present in Al_2O_3 after annealing induces a 2DHG without any applied gate voltage. This 2DHG, combined with only a single layer of gate electrodes, is the ingredient necessary to create depletion-mode type QDs, similar to devices created in GaAs/AlGaAs[30] or Si/SiGe heterostructures.[31,32] The following paragraphs describe a proof-of-principle of the creation of such devices in intrinsic Si and feature two gate designs that can be further optimized to realize single-hole occupation.

A depletion-mode quantum dot relies on the presence of a conducting state without applying voltages to electrodes. The already present 2DHG is locally depleted by positive voltages on the gate electrodes to form the tunnel barriers required for a QD.[30] Here, we deposit metallic gates on the substrate shown in Fig. 1(a) using electron-beam lithography, e-beam evaporation, and lift-off techniques. An extra layer of 5 nm Al_2O_3 is deposited on the devices using ALD to protect gates during the annealing step.[29,33]

First, we test the capability of the gate electrodes to locally deplete the 2DHG and pinch off the channel. Figure 2(a) shows the device "ABC" that consists of 10 electrodes coming in from the top and bottom. The electrodes at the far-left (L) and far-right (R) are present in the design for extra tunability. Each vertical pair of the electrodes, designated by the same upper and lower case letters, forms a gate. Figure 2(b) shows current-voltage characteristics of individual gates of the device "ABC." We can see that conduction through the channel can be turned off completely by applying sufficient

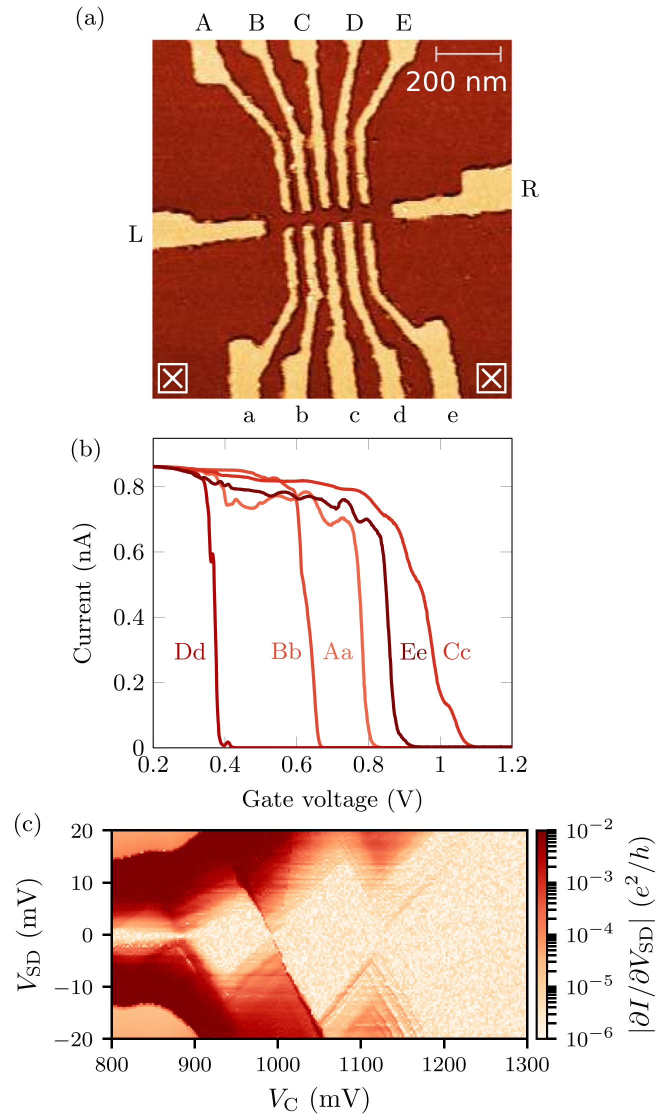

FIG. 2. (a) Atomic force microscopy image of the device "ABC," fabricated on top of the substrate shown in Fig. 1(a). Source/drain ohmic contacts are depicted by ⊠. (b) Current-voltage characteristics of device "ABC," individual vertical pairs of electrodes are swept together, all other electrodes are grounded while sweeping; measurements are done at source-drain bias $V_{SD} = 1\,mV$ and temperature $T = 4.2\,K$. (c) Numerical differential conductance $\partial I/\partial V_{SD}$ plotted vs. V_{SD} and V_C of a QD situated between gates B, b, C, and c. Only the voltage on the gate C is varied for optimal stability. Measurements are taken at $V_{Aa} = -2\,V$, $V_{Bb} = 0.65\,V$, $V_c = 1.52\,V$, $V_{Dd} = V_{Ee} = 0\,V$, $V_L = -1.5\,V$, $V_R = -0.2\,V$, and $T \approx 15\,mK$.

voltages on gate. This voltage depletes the 2DHG not only underneath a pair of top and bottom electrodes but also in between them. By tuning an applied voltage, we can thus form a tunnel barrier between that pair.

Now using a couple of these tunnel barriers, we will form a QD between the two adjacent gates Bb and Cc. The expectation is that, due to the gate geometry, the gaps between B and C as well as b and c are fully depleted except the very center of the structure where an island is formed. At the same time, the gaps between the top and bottom electrodes remain sufficiently conducting to act as two tunnel barriers to the formed island. Figure 2(c) shows the transport spectra of a formed QD. For optimal stability, only the voltage on the electrode C is varied in this measurement. The charging energy of the last visible transition is measured to

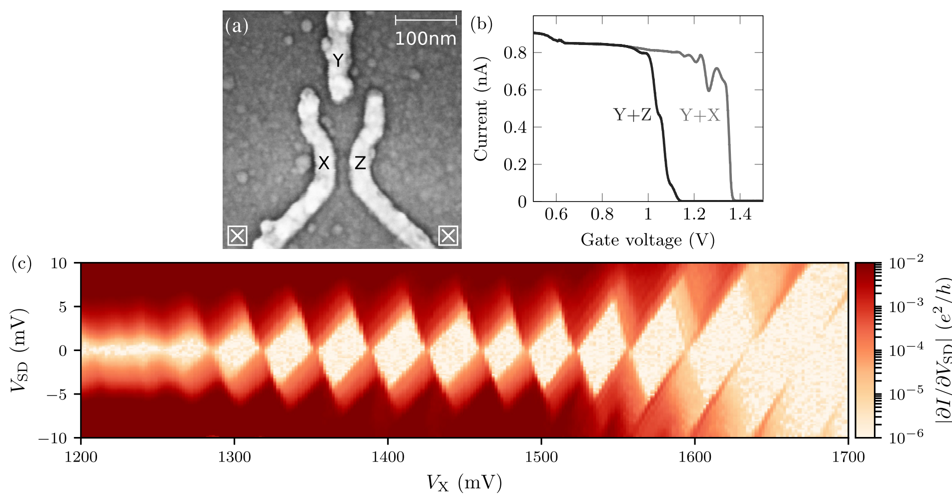

FIG. 3. (a) Scanning electron microscopy image of the device "XYZ," fabricated on top of the substrate shown in Fig. 1(a). Source/drain ohmic contacts are depicted by ⊠. (b) Current-voltage characteristics of the device "XYZ." Pairs of gates X and Y or Z and Y are swept together. The other gate is grounded, while sweeping each pair; measurements are performed at source-drain bias $V_{SD} = 1$ mV and temperature $T = 4.2$ K. (c) Numerical differential conductance $\partial I/\partial V_{SD}$ plotted vs. V_{SD} and V_X of QD in device "XYZ"; measurements are taken at $V_Y = 1425$ mV, $V_Z = 1625$ mV, and $T \approx 300$ mK.

be $E_C \approx 15$ meV and is an indication of reaching the single-hole regime, although only a charge sensing experiment can verify single-charge occupation.[34–36] This value is comparable to the charging energy of previously obtained results for the last electron in Si.[8,25,37,38] The results in Fig. 2 demonstrate that we can form QDs using this approach; the gate design needs further optimization[39] to improve control of a future spin qubit.

To advance results in Fig. 2, we adapt a proven gate design[30] to create the device "XYZ," shown in Fig. 3(a). To measure current-voltage characteristics of the left and right tunnel barriers, we grounded one of the bottom gates Z or X and sweep voltage together on the two other gates, i.e., X and Y or Z and Y, respectively. Figure 3(c) shows transport spectra of a QD formed between the gates. Well-defined non-distorted Coulomb diamonds with charging energies of $E_C \sim 3$–5 meV demonstrate the formation of a many-hole QD. This E_C corresponds to an electrostatically defined Coulomb island with a size of $d \approx 60$–70 nm based on a parallel plate capacitor model, which is close to the lithographical dimensions of the QD ($\sim$75 nm). These results show that we can form a robust hole-QD using a straightforward process and simple design. Further reduction of the lithographical dimensions of this design, which is already optimized for spin-qubit performance,[39] may allow reaching the few-hole regime.

To summarize, we have demonstrated that we can eliminate a 2DHG induced by fixed charge in Al_2O_3 by a deep-UV light treatment. This phenomenon potentially has a great impact on the MOS electron-QD community as many groups are starting to use ALD and might unintentionally induce a 2DHG in their samples with no possibility to detect it. Another important application for this technology is fine tuning of the bandgap bending that can improve coupling of nuclear spins to a microwave resonator.[40] Finally, hybrid-mode devices, where ALD-oxide will replace source/drain accumulation gates of the enhancement-mode devices to induce a 2DHG, simplifying fabrication and increasing the yield, can utilize the same phenomenon.

We have also shown transport characteristics of a single-layer depletion-mode hole-QD. Transport measurements indicate that we can fabricate QDs in the many-hole regime as well as QDs showing signs of the few-hole regime, where the last visible charge-transition has a charging energy $E_C \approx 15$ meV.

Initially, depletion-mode QDs were made in group IV semiconductors by doping, incompatible with long coherence times, or by use of epitaxial heterostructures. The design and device, as presented here, make for a very simple system to create depletion-mode QDs in undoped Si without the need for accumulation gates. The well-defined Coulomb diamonds when a single quantum dot is formed are promising, and optimization can push this design even further. This optimization should take care to absorb the lessons learned in previous designs[30] and is an easy path to tunable arrays of QDs[32] reaching single-hole occupation. Our fabrication method reliably passivates electrically active defects by hydrogen annealing, reducing charge noise, the primary source of qubit decoherence.[41] An additional advantage of a single-layer depletion-mode device is that it avoids damage from any electron-beam lithography[42] in the areas where the dots are actively formed. The open nature of the design means that future experiments could more easily couple external sources of light into the structure, for example, to optically address individual ions in silicon[43,44] and transfer quantum states between distant nodes of a quantum internet.[45] Conversely, by using positive fixed charge in another gate dielectric stack, e.g., SiO_2/HfO_2, one could create electron-based depletion-mode QDs.[27] Given these features, the depletion-mode design has its place alongside the enhancement-mode design[6,8] and could prove extremely useful in experiments in intrinsic Si.

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