Selective SiO_2 etching in three dimensional structures using parylene-C as mask

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This abstract describes an application of an easy and straightforward method for selective SiO_2 etching in three dimensional structures, which is developed by our group. The application in this abstract is the protection of the buried-oxide (BOX) layer of a silicon-on-insulator (SOI) wafer against SiO_2 hard mask stripping in BHF after deep reactive ion etching (DRIE) in the device layer, where the BOX layer serves as etch stop. It enables further processing like refilling of trenches and other structures with preservation of the BOX layer, which can serve as sacrificial layer or electrical isolation. The BOX layer protection is done with parylene-C. This is a poly(monochloro-*p*-xylylene) polymer, which is traditionally used to coat implantable devices [1], used as protective packaging material in (chemical) sensors [2], or as actual shapeable material in devices [3]. The presented method adds mask material for selective SiO_2 etching to the list.

To demonstrate this method, a simulated BOX layer is used. First, a plane 100 mm <100> double side polished Si wafer was cleaned in HNO_3 and HF (step A in figure 1), after which a 1 µm SiO_2 layer was grown via wet thermal oxidation at 1150°C of the wafer (step B). This layer was patterned with a pattern of 3 µm wide trenches via conventional I-line photolithography and SiO_2 etching in an Adixen AMS100 reactive ion etching system (step C). The trenches were etched 57 µm deep with a BOSCH process using an SPTS DRIE system (step D). After stripping of the photoresist and fluorocarbons in a TePla GIGAbatch 360M barrel etcher using an oxygen plasma and cleaning in HNO_3, a layer of 400 nm SiO_2 was grown via dry thermal oxidation at 1000°C (step E). This configuration mimics a SOI wafer with a device layer of 50 µm and a BOX layer of 400 nm. Then, a 2 µm thick conformal layer of parylene-C was deposited via CVD in an SCS PDS2010 system (step F). The dimer precursors were first vaporized at 175°C, and subsequently pyrolized at 690°C to create monomers. These monomers were deposited and subsequently polymerized on the surface in a vacuum chamber at 25°C. The chosen thickness is more than half the trench width, ensuring full filling of the trenches. The substrate was put horizontally into the same TePla system to reduce the effects of plasma inhomogeneity in the plasma chamber, and it was etched for 20 minutes in an O_2 plasma, which induces etching via aromatic ring opening [4] (step G). Here we take advantage of the fact that the plasma inside a barrel etcher is not directed towards the surface. The length of this isotropic etch step relates to the amount of parylene-C retraction. This gives us the possibility to shape the SiO_2 in three dimensions. After this step, the hard mask was removed via wet etching in BHF (step H) and the remaining parylene-C was stripped using a 95°C piranha solution (H_2SO_4:H_2O_2, 3:1) (step I). Inspections were done using the scanning electron microscope (SEM) of a FEI Nova 600 NanoLab system and a FEI Sirion HR-SEM.

Results are summarized in figures 2 to 5. All shown cross-sections were made by breaking, except the parylene-C filled trench. This one was made via dicing. The initial SiO_2 hard mask and the simulated BOX layer are visible on the SEM image shown in figure 2. The parylene-C filled trench is shown in figure 3. The dicing deformed the elastic parylene-C and disrupted the interfaces with the Si. figure 4 shows the bottom of the trench after parylene-C etching and hard mask stripping in BHF. It is visible here that the parylene-C bulk is etched almost completely to the bottom and that a thin film remains at the bottom and on the sidewalls, protecting the simulated BOX layer against BHF. After parylene-C stripping in piranha, it is clearly visible that the SiO_2 remained intact at the bottom of the trench (figure 5), but is removed from the top (figure 6).

It can be concluded that the proposed method is indeed a suitable method for the protection of the BOX layer when a SiO_2 hard mask needs to be removed after trench etching and that it can be translated to mask material for selective SiO_2 etching in three dimensions, which is future research.

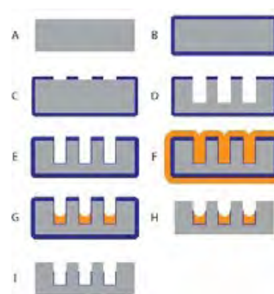

Figure 1. Schematic representation of the process steps explained in the abstract.

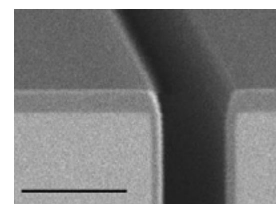

Figure 2. SEM image of the hard mask and the simulated BOX layer. Scale bar is 5 µm.

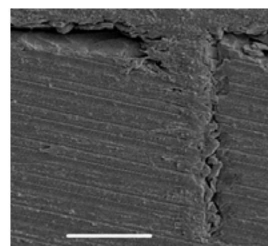

Figure 3. SEM image of a trench filled with parylene-C. Sample was prepared by dicing. Scale bar is 20 µm.

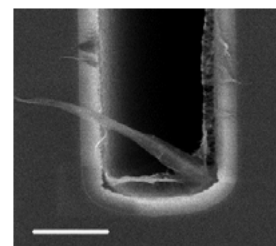

Figure 4. SEM image of the bottom of the trench after BHF etching of hard mask. Scale bar is 2 µm.

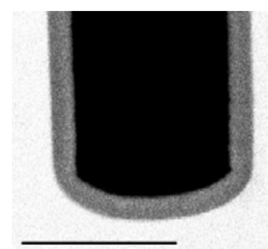

Figure 5. SEM image of the bottom of the trench after BHF etching of hard mask and parylene-c stripping. Scale bar is 3 µm.

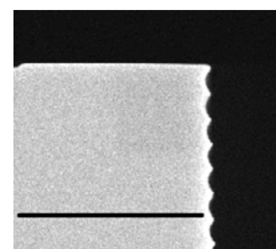

Figure 6. SEM image of the top of the trench after BHF etching and parylene-C stripping. Scale bar is 2 µm.

[1] T.Y. Chang, V.G. Yadav, S. De Leo, A. Mohedas, B. Rajalingam, C.-L. Chen, S. Selvarasah, M.R. Dokmeci, A. Khademhosseini, Langmuir 23 (2007) 11718-11725.
[2] L. Li, A.J. Mason, IEEE Sensors (2010) 1613-1616.
[3] Y. Suzuki, D. Miki, M. Edamoto, M. Honzumi, J. Micromech. Microeng. 20 (2010) 104002.
[4] E. Meng, P.-Y. Li, Y.-C. Tai, J. Micromech. Microeng. 18 (2008) 045004.