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Observations on the recovery of hot carrier degradation of hydrogen/deuterium passivated nMOSFETs

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ABSTRACT

Degradation due to hot-carrier injection and the recovery due to annealing in air have been investigated in long channel nMOSFETs, where the passivation of the dangling bonds at the Si/SiO_2 interface in the post metal anneal step is done with hydrogen or deuterium. The devices with deuterium passivation exhibit less degradation than the devices with hydrogen due to the well-known isotope effect. However, the recovery of hot-carrier induced degradation by thermal annealing in air is found to be independent of the isotope. An Arrhenius activation energy (E_a) of around 0.18 eV for threshold voltage (V_T) recovery for both types of devices was calculated, indicating that the recovery mechanism may be the same.

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1. Introduction

Hot-carrier degradation (HCD) is associated with the build-up of interface defects at or near the Si/SiO_2-interface. During fabrication, the dangling bonds of the Si-atoms at the interface are passivated with H-atoms. It is well established that when exposed to carriers with sufficient energy ("hot carriers"), the Si-H bond can be broken and a charged P_b-center is created, see *e.g.* [1]. These defects are distributed over the channel, however, the majority of defects will arise near the drain, where the carriers are the most "hot" and have the highest chance to induce the desorption of hydrogen atoms. An increase in the number of defects will cause a shift in the threshold voltage, ΔV_T, due to charge trapping in the new interface defects. The interface defects increase the coulomb scattering, degrading the mobility. As a consequence, the transconductance, g_m, and the linear drain current, $I_{d,lin}$, will be lower [2]. The passivation of the dangling bonds at the interface with deuterium instead of hydrogen ensures a better reliability and stress resistance, which is better known as the isotope effect [3].

Defects can also arise in the gate oxide, where a Si–O bond can be broken. This broken bond creates a dangling bond at a trivalent Si-atom or O-atom (E′ -center), which functions as a charge trap with possible states −e, 0 and +e. Trapped charge will cause a negative or positive shift in the electric characteristics of the device. Holes are more easily captured by an E′ -center than electrons, what results in a parallel negative shift in V_T. The formation of new E′ -centers in the gate oxide may further result in an increase of the gate current, I_g [4].

The shift in V_T due to the creation of interface defects depends on the applied bias/electric field, temperature (T) and stress time (t), which can be described using an Arrhenius dependence and a power law dependence, respectively [5], leading to Eq. (1).

$$\Delta V_T = A e^{-\frac{E_a}{k_B T}} t^n \tag{1}$$

where A is a bias dependent parameter, E_a is the activation energy, k_B is the Boltzmann constant and n is a degradation-type dependent constant. The activation energy is a signature of the temperature dependency of the reaction.

The recovery of a device is dependent if a bias opposite to the applied stress is applied [6]. In this work, the recovery in air without an applied bias is investigated as function of several anneal temperatures, T_a.

The recovery process may not follow the same principles as during degradation and can thus not be described by Eq. (1). Yet, Arrhenius behavior can still be expected when diffusion and reaction mechanisms determine the recovery [2]. It is expected that during

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recovery mostly N_{it}-defects will be passivated and that slow traps play a minor roll [7]. Consequently, V_T will decrease and g_m and $I_{d,lin}$ will increase as function of anneal time, t_a. Furthermore, HCD will be worse at lower temperatures for long channel devices (negative E_a), while recovery will be higher for a higher temperature (positive E_a).

In this article, we study the slow, long-term recovery of HCD of nMOS transistors. The motivation behind this work lies in the pursuit of self-healing transistors, see *e.g.* [8,9]. Since the primary actor in HCD, the hot carrier itself, is absent during our recovery experiments, it is safe to assume that the physical mechanisms governing recovery are different. It is further safe to assume that recovery is accelerated by temperature, in view of the many reports in literature documenting HCD repair after high temperature anneals (see *e.g.* [10]). This is in contrast to the reduction of HCD creation in long channel devices with increasing stress temperature [2]. Future work will investigate the isotope effect in combination with periodic recovery using a more direct approach to measure N_{it} (*e.g.* charge pumping) or a faster method (*e.g.* On-the-fly). Different other degradation and recovery mechanisms (Si–O bond breaking, slow/fast-traps, charge (de-)trapping) can then be excluded with a higher degree of certainty, which will result in more clarity on the repassivation of Si–D bonds after degradation.

2. Experimental

The devices under study were nMOSFETs with a width of $W = 10.0\,\mu m$, a length of $L = 0.35\,\mu m$ and a gate oxide thickness of $t_{ox} = 7$ nm. A mixture of O_2 and D_2 was used during the oxidation step to create the gate oxide and a mixture of H_2 or D_2 with N_2 was respectively used for the post metal anneal step for the passivation of the dangling bonds at the interface. For further documentation of the devices, see [11]. Since the slow, long-term degradation and recovery of HCD were investigated, measurements were done using the measure-stress-measure (MSM) method. Measurements were done in normal mode (integration time) with a Keithley 4200-SCS and a Keithley 4200-PA Remote PreAmp, where the drain voltage was kept at $V_{ds} = 0.1$ V and the gate voltage was swept from $V_{gs} = 0$ V to $V_{gs} = 3$ V with steps of 10 mV. During stress, a constant voltage stress (CVS) was applied to the device at 25 °C for a cumulative time of 10^4 s, creating the shift in de I_d-V_{gs} curve of Fig. 1.

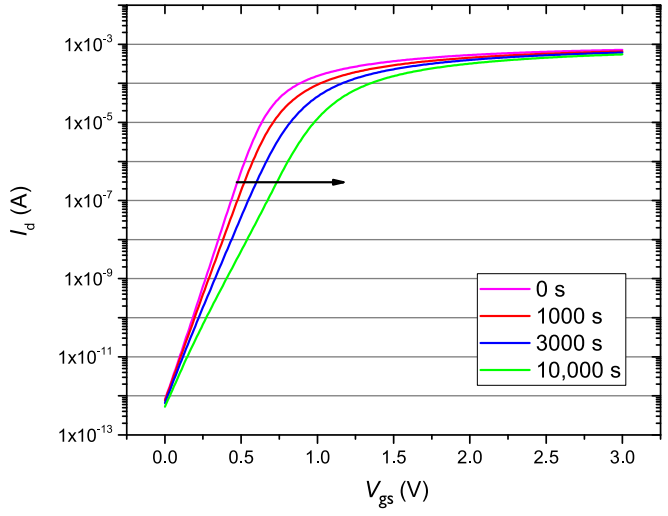

Fig. 1. I_d-V_{gs} curve after different cumulative stress times of the H-passivated device. V_T and the subthreshold swing become larger for an increase in the stress time. Stress was done at $T = 25$°C, where $V_{ds} = 4.5$ V, $V_{gs} = 2.1$ V and the measurement at $T = 25$°C, where $V_{ds} = 0.1$ V.

During stress, the applied source-drain voltage was kept at $V_{ds} = 4.5$ V and the gate-source voltage was kept at ($V_{gs} = 2.1$ V), where the bulk current $|I_b|$ is maximum. There was a delay of 1 s between the stress and measurement phase.

The non-parallel shift of Fig. 1 in the subthreshold characteristics demonstrates significant degradation, accompanied with a V_T shift. This is a signature of interface state creation. No change in the gate current I_g is observed, (~15 nA before and after 10^4 s stress), suggesting that bulk trap creation is negligible at these stress conditions.

The threshold voltage, calculated using the maximum transconductance method [12], was investigated for different stress/anneal cycles. A degradation in mobility will cause the shift in V_T. The threshold voltage shift (ΔV_T) due to degradation is defined as described in Eq. (2):

$$\Delta V_T(t) = V_T(t) - V_T(0) \tag{2}$$

where t is the degradation time. At $t = 0$ s, the device is in its pristine, unstressed state. After the device was stressed, it was heated with a M300 thermochuck from Att Systems (temperature ramp rate: 0.1 $^{\circ C}/_{s}$) to 200 °C and annealed for 1500 s in air and subsequently stressed again for different cycles, as shown in Fig. 2a.

The recovery as function of anneal time was investigated by first stressing a pristine device at $T = 25$° C. After stressing, the wafer was brought to an elevated temperature (T_a). Upon reaching T_a; V_T, g_m and $I_{d,lin}$ are measured. Subsequently, V_T, g_m and $I_{d,lin}$ are measured periodically as function of anneal time in air for five different temperatures (50, 85, 120, 150 and 175 °C – one device per temperature). $I_{d,lin}$ is measured at $V_{ds} = 0.1$ V & $V_{gs} = 2.0$ V. The threshold voltage shift during recovery is also defined as described in Eq. (2). However, in this case is $t = t_a$. At $t_a = 0$ s, the device is at the moment that T_a is reached and the degradation is maximum at that temperature. Δg_m and $\Delta I_{d,lin}$ for recovery are calculated in similar fashion. The measurement process is shown in Fig. 2b.

Measurements done on similar devices ($W = 10.0\,\mu m$, $L = 0.2\,\mu m$ & $L = 0.25\,\mu m$) only showed negligible degradation due to BTI [11]. It is thus assumed that the degradation is mostly caused by hot carriers.

3. Results and discussion

The unstressed H/D-passivated nMOSFETs have the same V_T. Stressing at room temperature ($T = 25$°C) at maximum $|I_b|$ for a

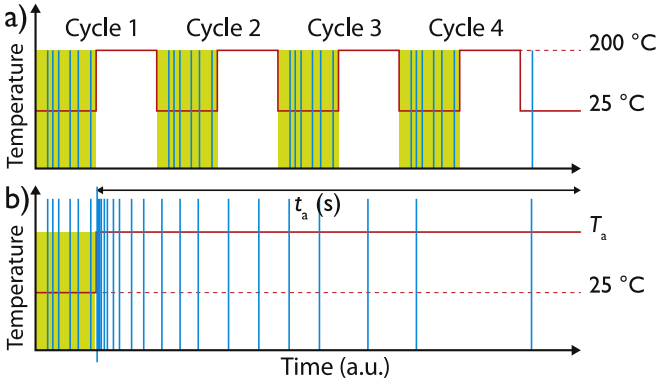

Fig. 2. a) The measurement process to investigate different anneal/degradation cycles; b) the measurement process to investigate the temperature dependence of recovery as function of the time – The blue, vertical lines represent the moment of the measurement, green represent the moments that the device is stressed and the corresponding temperature is given in red. T_a is the annealing temperature and t_a is the annealing time.

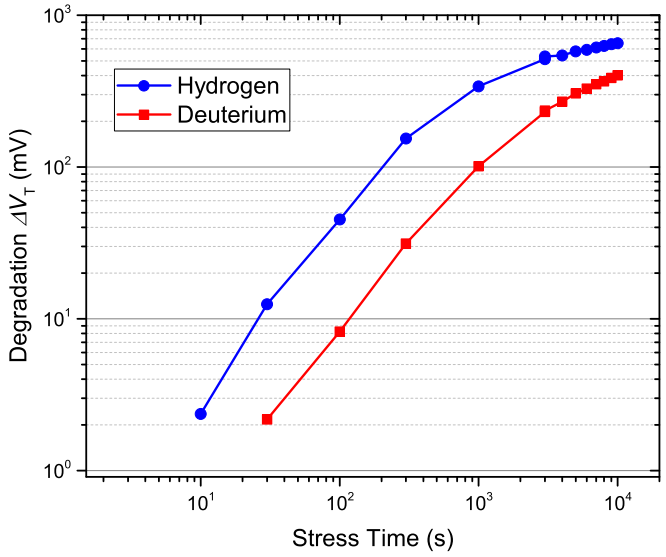

Fig. 3. ΔV_T for an increasing stress time. Measurements and stress done at $T = 25°C$. Stress started at $t = 0$ s. D-passivated devices are more resistant to HCD due to the isotope effect.

cumulative time of $t = 10^4$ s results in a factor ~3 smaller ΔV_T for D-passivated devices than for H-passivated devices, as is shown in Fig. 3.

Fig. 4 shows V_T as function of time for four different stress/anneal cycles. V_T is determined at room temperature, after stressing and after annealing, according to the procedure of Fig. 2a. During annealing, the H- and D-passivated devices have similar levels of recovery, but relatively more for the D-passivated device (there was less degradation). This difference in stress and recovery seems to diminish over subsequent cycles. Over time, the devices seem to behave more and more alike, stress and recovery-wise.

If only N_{it}-repassivation takes place, the recovery of g_m should be proportional to the recovery of V_T. The transconductance is plotted as function of the threshold voltage for the different cycles in Figs. 5 and 6 for the H- and D-passivated devices, respectively. After starting a new cycle is started, the V_T should decrease and g_m should increase again, which is visible in both figures. Taking into account the margin

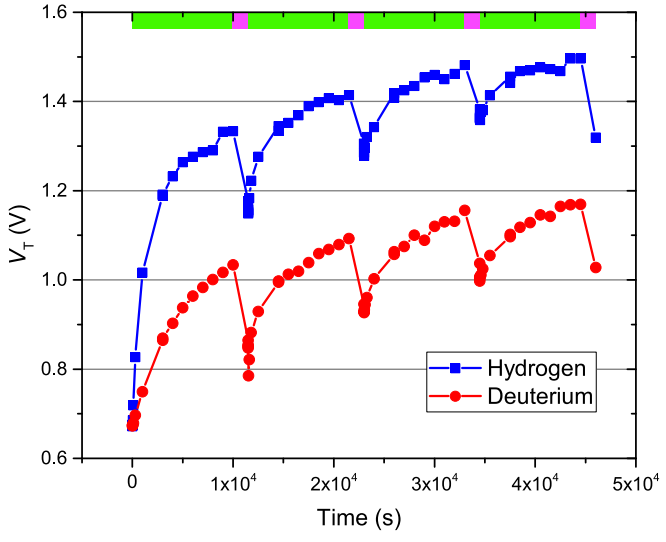

Fig. 4. The threshold voltage as function of time. After each 10^4 s of stress (green), the device is annealed at 200 °C for 1500 s (magenta). Stress and measurements are done at $T = 25°C$.

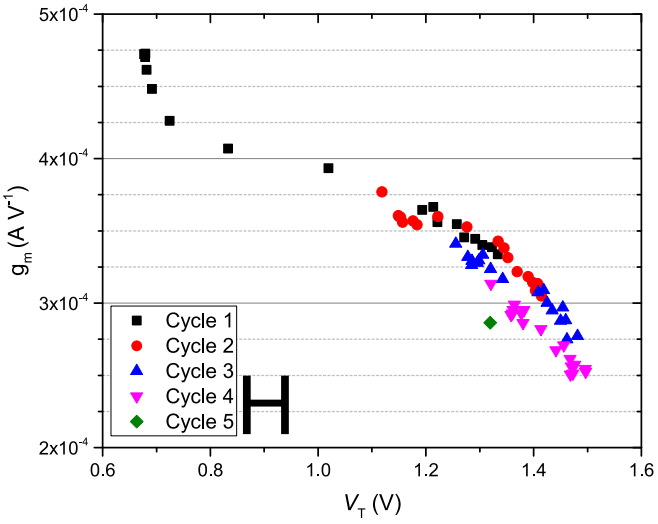

Fig. 5. Transconductance as function of the threshold voltage for the H-passivated device for different degradation/anneal cycles, both are measured at $T = 25°C$.

of error, these figures indicate that the majority of the recovery is due to repassivation of N_{it}.

3.1. Threshold voltage recovery

The rest of the data is acquired using the procedure of Fig. 2b. Degradation of the devices caused an increase in V_T. During recovery by annealing, V_T should decrease again, which results in a negative ΔV_T. The recovery of V_T at an elevated temperature in air is shown in Figs. 7 and 8 for H- and D-passivated devices, respectively. The recovery for both types of devices appears to follow a $\log(t_a)$ dependency.

3.2. Transconductance recovery

Degradation resulted in a decrease in g_m. During recovery, the g_m will increase again, which results in a positive Δg_m. The recovery of the peak transconductance as function of t_a is shown in Figs. 9 and 10 for the H- and D-passivated devices, respectively. The figures show the normalized transconductance, which is normalized to the value of g_m at $t_a = 0$ s. There is an increased level of scattering around 10^4

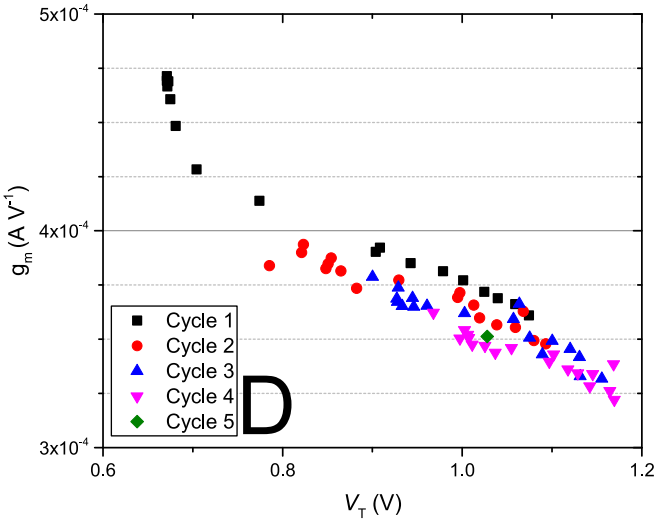

Fig. 6. Transconductance as function of the threshold voltage for the H-passivated device for different degradation/anneal cycles, both are measured at $T = 25°C$.

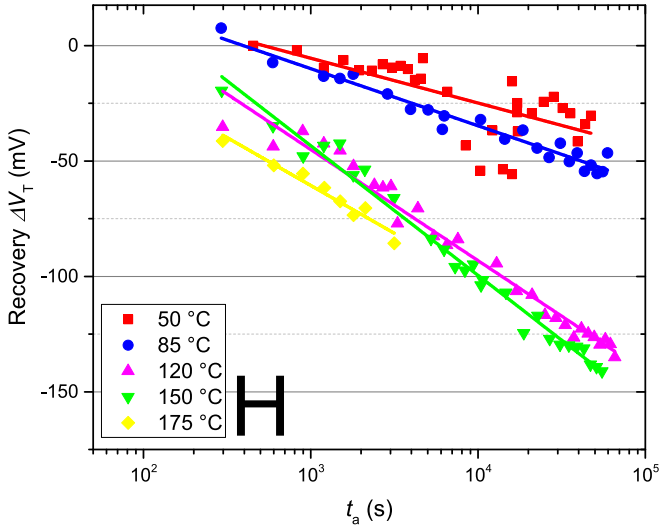

Fig. 7. Recovery of the threshold voltage of the H-passivated devices after 10^4 s of stress at $T = 25$°C and at $V_{ds} = 4.5$ V & $V_{gs} = 2.1$ V at different T_a at a drain voltage of $V_{ds} = 0.1$ V. The lines are a guide for the eye.

s for Fig. 9 and around $2 \cdot 10^3$ s for Fig. 10. This is also present in the data for V_T and $I_{d,lin}$, but less pronounced. The exact origin still needs to be figured out, but could currently not be pinpointed.

Compared to the previously treated ΔV_T data, these Δg_m data show less pronounced dependencies on both temperature and time. The data suggests a $\log(t_a)$ or a t_a^n dependence for the recovery of the transconductance for the more elevated temperatures. The exact dependence is not clear from the data, however a $\log(t_a)$ dependence is more likely, considering the data of the recovery of V_T and $I_{d,lin}$.

3.3. Recovery of $I_{d,lin}$

Degradation resulted in a decrease of $I_{d,lin}$, which should recover during annealing, creating a positive $\Delta I_{d,lin}$. $I_{d,lin}$ is determined at $t = 0$ s upon reaching T_a and is used as the starting value where maximum degradation was present. The recovery as function of t_a is shown in Figs. 11 and 12 for both types of devices.

As with the recovery of ΔV_T, the recovery behavior of $\Delta I_{d,lin}$ indicate a $\log(t_a)$ dependence. A higher elevated temperature will lead

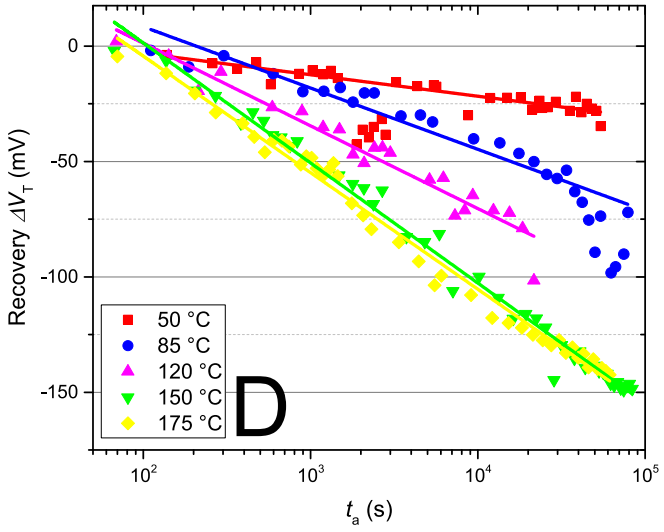

Fig. 8. Recovery of the threshold voltage of the D-passivated devices after 10^4 s of stress at $T = 25$°C and at $V_{ds} = 4.5$ V & $V_{gs} = 2.1$ V at different T_a at a drain voltage of $V_{ds} = 0.1$ V. The lines are a guide for the eye.

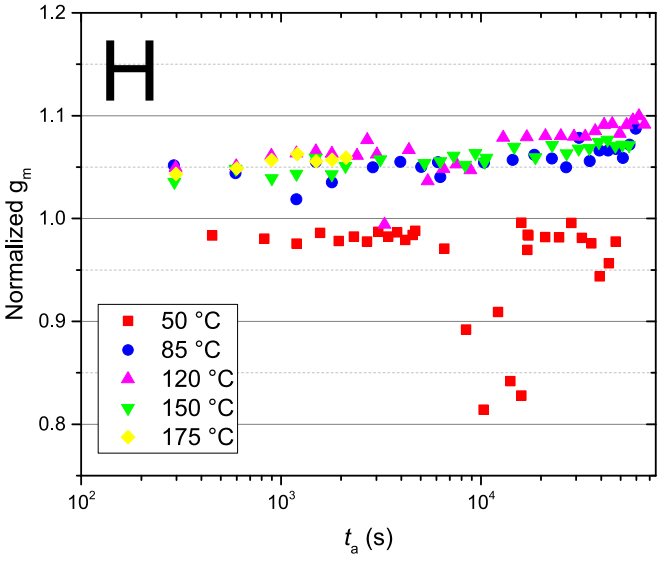

Fig. 9. The relative recovery of the transconductance as function of the anneal time for the H-passivated device after 10^4 s of stress at $T = 25$°C and at $V_{ds} = 4.5$ V & $V_{gs} = 2.1$ V at different T_a at a drain voltage of $V_{ds} = 0.1$ V.

to a higher recovery rate and the data suggests further that the absolute amount of recovery is almost the same for both devices. The H-passivated devices endured more degradation, so the relative recovery is smaller than for the D-passivated devices.

3.4. Activation energy

The temperature dependence of the recovery of V_T is shown in Arrhenius representation in Fig. 13. For this figure $|\Delta V_T|$ is determined at $t_a = 3$ ks from a fit (guide for the eye) of Figs. 7 and 8. Using Eq. (1) and Fig. 13, the activation energy can be determined as $E_a = 0.176$ eV and $E_a = 0.181$ eV for H- and D-passivated devices respectively, which suggests a similar activation energy.

This suggests that the recovery of HCD for both types of devices is caused by a similar process, regardless of the used isotope during the

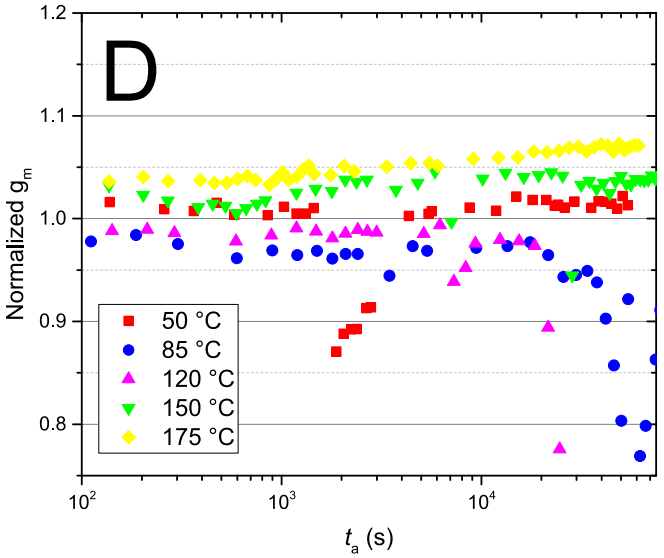

Fig. 10. The relative recovery of the transconductance as function of the anneal time for the D-passivated device after 10^4 s of stress at $T = 25$°C and at $V_{ds} = 4.5$ V & $V_{gs} = 2.1$ V at different T_a at a drain voltage of $V_{ds} = 0.1$ V.

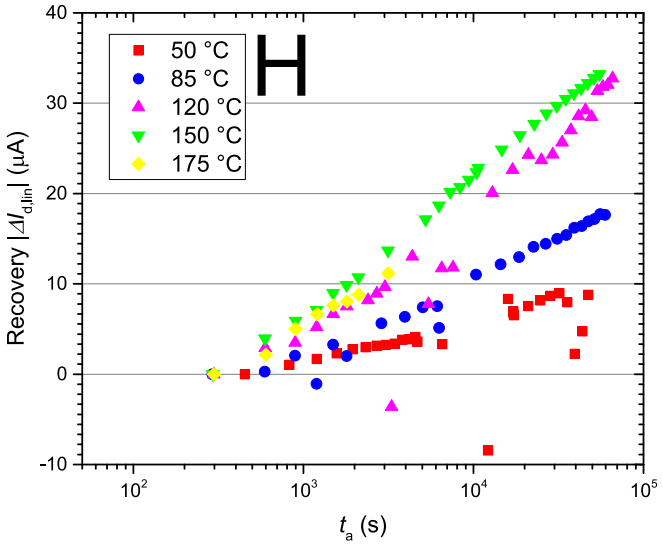

Fig. 11. Recovery of $I_{d,lin}$ at $V_{gs} = 2$ V of the H-passivated devices at different T_a for increasing anneal time after 10^4 s of stress at $T = 25$°C.

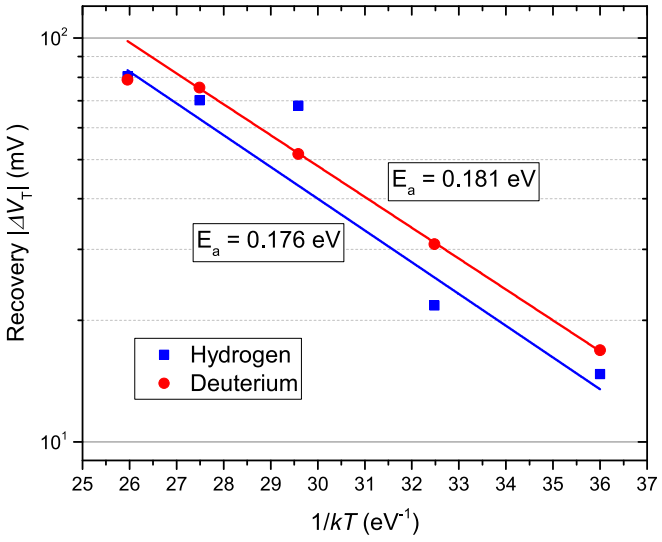

Fig. 13. Arrhenius relationship between $|V_T|$ at $t_a = 3 \cdot 10^3$ s and the recovery temperature.

passivation step: the adsorption of H-atoms at the interface to repassivate dangling bonds. Hydrogen will probably be introduced by diffusion from the surrounding dielectric, which will always contain H-atoms due to the various fabrication steps that involve hydrogen [13]. Deuterium has a lower diffusion coefficient [14,15], making it easier for hydrogen atoms to reach and to repassivate dangling bonds at the Si/SiO_2 interface.

4. Conclusions

The time dependent recovery of different electrical parameters in hot-carrier stressed H- and D-passivated nMOSFETs is observed at different anneal temperatures in air. During annealing, the H- and D-passivated devices have similar levels of recovery, but relatively more for the D-passivated device. This difference in stress and recovery seems to diminish over subsequent stress/anneal cycles. Over time, the devices behave more and more alike. The activation energy of the recovery for both types of devices are, within the experimental uncertainty, the same, suggesting that the same type of recovery mechanism takes place. An explanation is that for both types of devices H-atoms are introduced near the P_b-centers, passivating the dangling bonds, effectively changing the D-atoms at the Si/SiO_2 interface in the D-passivated devices for H-atoms. The abundant H-atoms in the gate oxide itself and the surrounding materials may be responsible for the observed recovery, by diffusing through the material stack and repassivate the dangling bonds.

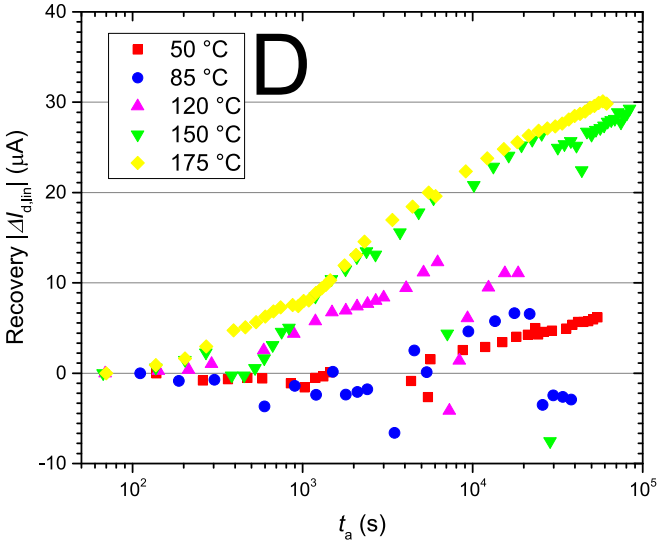

Fig. 12. Recovery of $I_{d,lin}$ at $V_{gs} = 2$ V of the D-passivated devices at different T_a for increasing anneal time after 10^4 s of stress at $T = 25$°C.

References

[1] G.J. Gerardi, E.H. Poindexter, P.J. Caplan, N.M. Johnson, Interface traps and P_b centers in oxidized (100)silicon wafers, Appl. Phys. Lett. 49 (6) (1986) 348–350.
[2] S.E. Tyaginov, I. Starkov, H. Enichlmair, J.M. Park, C. Jungemann, T. Grasser, Physics-based hot-carrier degradation modeling, Electrochem. Soc. Trans. 35 (4) (2011) 321–352.
[3] K. Hess, I.C. Kizilyalli, J.W. Lyding, Giant isotope effect in hot electron degradation of metal oxide silicon devices, IEEE Trans. Electron Devices 45 (2) (1998) 406–416.
[4] G.S. Ristic, Influence of ionizing radiation and hot carrier injection on metal-oxide-semiconductor transistors, J. Phys. D. Appl. Phys. 41 (2). (2008)023001.
[5] M. Rafik, X. Garros, G. Ribes, G. Ghibaudo, C. Hobbs, A. Zauner, M. Muller, V. Huard, C. Ouvrard, Impact of TiN metal gate on NBTI assessed by interface states and fast transient effect characterization, 2007 IEEE International Electron Devices Meeting, 2007, pp. 825–828.
[6] F.E. Pagaduan, A. Hamada, C.Y. Yang, E. Takeda, Hot-carrier detrapping mechanisms in MOS devices, Jpn. J. Appl. Phys. 28 (11A). (1989)L2047.
[7] G. Pobegen, Recovery From Hot Carrier Induced Degradation Through Temperature Treatment, Springer International Publishing, Cham, 2015, 221–230.
[8] J. Schmitz, Self-healing in semiconductors, Future Trends in Microelectronics, Mallorca, Spain, 2015,
[9] D.I. Moon, J.Y. Park, J.W. Han, G.J. Jeon, J.Y. Kim, J. Moon, M.L. Seol, C.K. Kim, H.C. Lee, M. Meyyappan, Y.K. Choi, Sustainable electronics for nano-spacecraft in deep space missions, 2016 IEEE International Electron Devices Meeting (IEDM), 2016, 31.8.1-31.8.4.
[10] J.C. King, C. Hu, Effect of low and high temperature anneal on process-induced damage of gate oxide, IEEE Electron Device Lett. 15 (11) (1994) 475–476.
[11] C. Salm, A.J. Hof, F.G. Kuper, J. Schmitz, Reduced temperature dependence of hot carrier degradation in deuterated nMOSFETs, Microelectron. Reliab. 46 (9) (2006) 1617–1622.
[12] D.K. Schroder, Semiconductor Material Device Characterization, 2nd edition ed., Wiley-Interscience. 1998.
[13] G.I. Isai, ECR Plasma Deposited SiO_2 and Si_3N_4 Layers: A Room Temperature Technology, June 2003.Ph.D. thesis, Enschede.
[14] H. Park, C.R. Helms, The effect of annealing treatment on the distribution of deuterium in silicon and in silicon oxide systems, J. Electrochem. Soc. 139 (7) (1992) 2042–2046.
[15] L. Nuccio, Diffusion of Small Molecules in Amorphous SiO_2: Effects on the Properties of the Material and on its Point Defects, February 2009, http://www1.unipa.it/lamp/NuccioPhDThesis.pdf. Ph.D. thesis, Palermo.