Electrostatic Doping in Semiconductor Devices

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***Abstract*— To overcome the limitations of chemical doping in nanometer-scale semiconductor devices, electrostatic doping (ED) is emerging as a broadly investigated alternative to provide regions with a high electron or hole density in a semiconductor device. In this paper, we review various reported ED approaches and related device architectures in different material systems. We highlight the role of metal and semiconductor workfunctions, energy bandgap, and applied electric field and the interplay between them for the induced ED. The effect of interface traps on the induced charge is also addressed. In addition, we discuss the performance benefits of ED devices and the major roadblocks of these approaches for potential future CMOS technology.**

***Index Terms*— Charge-plasma, doping, electron–hole bilayer (EHB), metal workfunction, MOSFET, p-n junction, reconfigurable FET, Schottky barrier (SB), semiconductor–metal interfaces, silicon-on-insulator (SOI), tunnel FET, ultrathin body (UTB).**

I. Introduction

DOPING semiconductor materials by incorporating chemical impurities has been key to the development of today's cutting edge device technologies [1]. However, with device dimensions of only a few nanometers, the conventional impurity doping faces challenges. The formation of junctions with extremely high doping gradients (a few nm/decade) is practically difficult [2], [3]. At nanometer scale, a dopant concentration above its solid solubility limit would be required to achieve sufficiently low channel and contact resistances. In addition, random doping fluctuations and the resulting variability have been the key concern for manufacturing nanoscale devices and circuits with high yield [4]–[6].

The accurate control of doping type, level, and spatial distribution in nanostructures, such as a nanowire, is also challenging because of their complex growth dynamics and geometrical constraints [7], [8]. For any nanoscale device, the requirement of a high carrier density along with unintentional and undesired ionized dopants in the active region points toward impurity free doping solutions.

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In the case of alternative emerging material systems, such as wide bandgap semiconductors (e.g., GaN, SiC, and ZnO), it is still difficult to obtain either p-type or n-type regions via impurity doping. This is mainly because of deep donor or acceptor levels or dopant passivation via complex formation [9]–[12]. The chemical doping route is also not straightforward for many other semiconductor materials, such as carbon nanotubes (CNTs) and emerging 2-D materials [graphene, phosphorene, silicene, and transition metal dichalcogenides (TMDs)] [13], [14]. For example, tunneling FETs (TFETs) based on ultrathin channels and 2-D materials are potential contenders for beyond-CMOS technology as they promise sub-60-mV/decade subthreshold slope [15]. However, their full potential has still not been realized experimentally. The reason for their limited performance lies in the difficulty in realizing highly doped junctions with a steep profile and low defect density, which is critical to an efficient tunneling process [14], [16].

Consequently, various approaches have been proposed in recent years to influence the electron and hole concentrations by means other than chemical doping. In many of these approaches, electrostatic interaction between the semiconductor and a different material at the interface governs the carrier density. We therefore refer to these approaches as "electrostatic doping (ED)."

These approaches include devices, such as Schottky barrier (SB) MOSFETs [17], [18], charge plasma (CP)-based ultrathin body (UTB) devices [19]–[22], reconfigurable FETs based on silicon (Si) nanowires [23]–[25], FETs based on graphene [26]–[29], CNT [30]–[32] and 2-D materials [33], [34], and electron–hole bilayer (EHB)-based TFETs [35]–[37]. ED potentially offers ultrasharp junctions with a well-controlled carrier concentration profile and a reduced defect density. These features make ED an attractive alternative to conventional impurity doping for a broad range of electron devices.

This paper presents an overview of various reported ED concepts, and is organized as follows. In Section II, we first define the ED concept. Thereafter, we review various reported ED approaches under three proposed categories based on the nature of the underlying electrostatics. Here, we focus on the electrostatics for different types of metal–semiconductor (MS) systems. Furthermore, in Section III, we focus our discussion on the performance of potential ED devices for future CMOS technology and address the major challenges and possible drawbacks of the ED techniques. Section IV summarizes our findings.

II. Electrostatic Doping Concept

ED is a technique in which charge carriers (electrons or holes) are induced in a semiconductor material as a

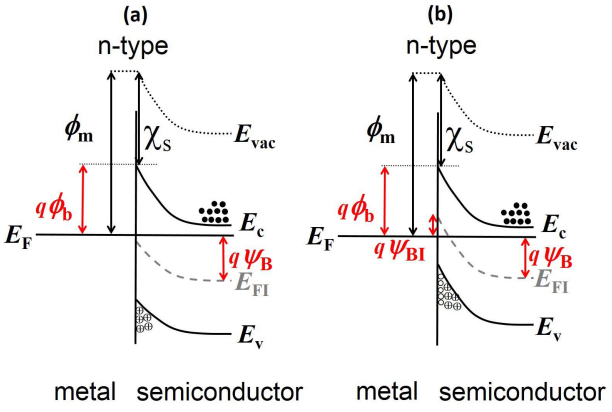

Fig. 1. Schematic energy band diagrams for (a) traditional n-type Schottky contact. A depletion layer is formed at the MS interface. (b) n-type Schottky contact with excessive band-bending near the interface resulting in inversion (p-type) charge in an n-type semiconductor (see Eq. (3)). A shallow p-n junction is formed near the MS interface. A similar situation can be obtained with Schottky contacts on a p-type semiconductor. Filled circles: electrons. Open circles: holes. Circles with a + sign: donor charge.

result of its band alignment near its interface with another (semi)conducting material. In the ED approach, the relative separation, between the Fermi level and the semiconductor energy bands, that governs the active doping concentration, is controlled by the potential and the workfunction of the electrode adjacent to the semiconductor body rather than by the chemical impurities as in conventional doping. The electrostatic condition at the MS interface, which influences the band alignment, is a strong function of the metal workfunction (ϕ_m), the semiconductor's energy bandgap (E_g), electron affinity (χ_s), and workfunction (ϕ_s). In addition, the applied electric field, if any, also influences the electrostatic properties near the interface. Note that, in this paper, we only focus on metal (or metallic compound) induced ED; other heterostructure-based doping like polarization doping, e.g., in III-nitrides [38] is beyond the scope of this paper.

We subdivide the ED approaches into three categories: 1) SB-based devices; 2) workfunction-induced doping; and 3) bias-induced doping. In Sections II-A–II-C, we will review these ED techniques as applied to different devices and material systems.

A. Schottky Barrier-Based Devices

SB-based devices are devices in which the current is limited by one or more Schottky contacts. The physics of an SB formed at the MS interface has been well described earlier [39].

An SB with height $q\phi_b$ is formed when $\phi_m > \phi_s$ for an n-type semiconductor [Fig. 1(a)] and $\phi_m < \phi_s$ for a p-type semiconductor, where q is the elementary charge. The SB height (SBH) $q\phi_b$ equals $(\phi_m - \chi_s)$ for n-type and $(E_g - \phi_m + \chi_s)$ for p-type semiconductor. The presence of this potential barrier ϕ_b at the MS interface results in the fundamental difference in the operation of SB devices from p-n junction devices. For the former, the MS interface, hence ϕ_b, fully controls the majority unipolar current [39]. The electron or hole emission in SB devices is governed by thermionic emission over the barrier and (thermionic) field emission through the barrier in contrast to p-n junction-based devices, where processes, such as drift-diffusion and band-to-band tunneling (BTBT) of both electrons and holes, control the current.

However, for an ideal unipolar Schottky type operation, it is essential to limit the band bending such that for an n-type semiconductor, at the interface, the intrinsic Fermi-level E_{FI} falls below the Fermi level E_F, which implies that $\phi_b \leq u_T \cdot \ln(N_c/n_i)$, where N_c is the conduction band effective density of states, n_i is the intrinsic carrier concentration, and u_T is the thermal voltage ($=kT/q$, where k is Boltzmann's constant and T is the temperature). Excessive band-bending at the MS interface may result in a p-n junction-type operation as discussed in Section II-B1. Therefore, the limiting conditions at the MS interface ($x = 0$) for a unipolar Schottky-type operation can be expressed as

$$(E_c - E_F)|_{x=0} = q\phi_b \leq kT \cdot \ln\left(\frac{N_c}{n_i}\right) \tag{1}$$

for an n-type semiconductor, and

$$(E_F - E_v)|_{x=0} = q\phi_b \leq kT \cdot \ln\left(\frac{N_v}{n_i}\right) \tag{2}$$

for a p-type semiconductor. E_c and E_v represent the conduction band edge and valence band edge, respectively, and N_v is the valence band density of states. The terms $kT \cdot \ln(N_c/n_i)$ and $kT \cdot \ln(N_v/n_i)$ are approximately equal to $E_g/2$ for most semiconductors.

Next, we discuss two specific examples of SB devices, which could be interesting for future CMOS.

1) Schottky Barrier MOSFETs: The idea to replace doped source/drains (S/Ds) in conventional MOSFETs with metal was first proposed by Nishi [40] in 1966. In 1968, Lepselter and Sze [17] reported the first Si pMOS device, where S/Ds were replaced by PtSi. Thereafter, a series of developments resulted in the metal S/Ds SB-MOSFET [Fig. 2(a)] technology, which basically replaces impurity-doped S/Ds in conventional MOSFETs with metal, typically silicide.

In this transistor, the charge carriers are injected from the metal into the semiconductor channel via thermionic (-field) emission as in a Schottky diode. However, in the SB-MOSFET, the gate field further influences the barrier height and width as shown in Fig. 3(a) and (b). The SB-MOSFET technology is claimed to offer several benefits for sub-30-nm scaling, such as a low parasitic S/D resistance, sharp junctions, better control over the OFF-state leakage current, elimination of parasitic bipolar action, and low thermal budget processing [18]. Furthermore, the use of midgap silicides allows the realization of SB-pMOS and SB-nMOS devices, as required for the CMOS technology. Recently, in [41], the SB-FINFET was realized featuring a 6-mV/decade subthreshold swing at room temperature. The concept of SB-MOSFETs has also been adopted in CNTs [31], [32], [42]. For a thorough review on SB-MOSFET technology refer to [18].

2) Reconfigurable SB-MOSFETs: The idea of using SB contacts for ED is also embraced by the research community for applications other than the traditional CMOS. The Si

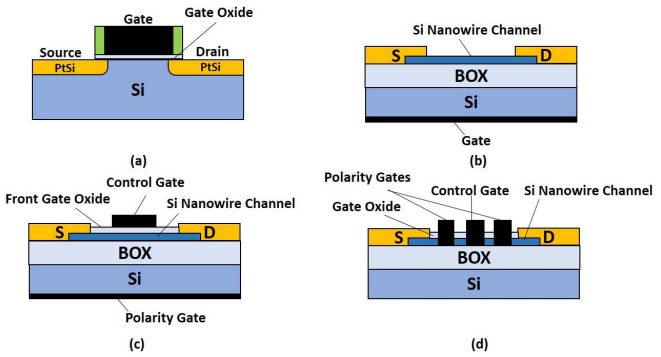

Fig. 2. Schematic cross section of (a) Si-based SB-MOSFET [18], (b) Si nanowire-based SB-MOSFET with single backgate design [43], (c) Si nanowire-based reconfigurable SB-MOSFET with front and back dual gate design [25], and (d) Si nanowire-based reconfigurable SB-MOSFET with dual gate-all-around design [23].

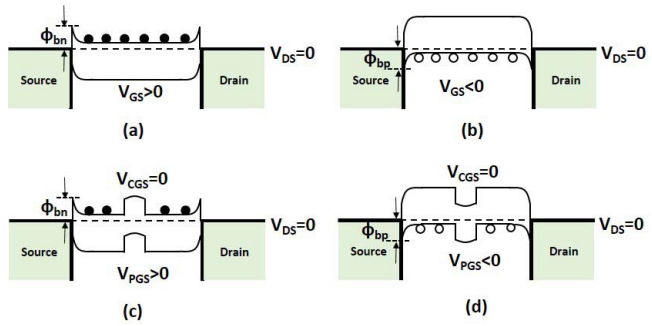

Fig. 3. Schematic energy band diagram: Si-based SB-MOSFET [18] [Fig. 2(a)] for (a) n-type operation ($V_{GS} > 0$ V), (b) p-type operation ($V_{GS} < 0$ V). Si nanowire-based reconfigurable SB-MOSFET [25] [Fig. 2(c)] for (c) n-type operation ($V_{PGS} > 0$ V) and (d) p-type operation ($V_{PGS} < 0$ V). V_{PGS} and V_{CGS} denote the polarity gate and control gate bias, respectively. An electron channel is formed for a positive $V_{(P)GS}$ and a hole channel is formed for a negative $V_{(P)GS}$. The V_{CGS} controls the current in the channel.

nanowire FET [43] with SB source and drain was shown to exhibit ambipolar characteristics [Fig. 2(b)]. The ambipolarity in this device was successfully suppressed by the introduction of an additional terminal (polarity gate) [Fig. 2(c) and (d)]. This terminal offers a new degree of freedom in the device: the polarity of conduction can be controlled, which was utilized in [23]–[25] and [44] to demonstrate a reconfigurable FET operation. In these reconfigurable (or polarity controlled) devices, one gate electrode (control gate) controls the conduction through the channel while the other gate electrode (polarity gate) controls the polarity of conduction [see Fig. 3(c) and (d)].

The choice of the electrode metal in these devices determines the resultant SBHs for electrons (ϕ_{bn}) and for holes (ϕ_{bp}) at the junction. Unipolar operation ($\phi_{bn} \neq \phi_{bp}$) is desirable for conventional SB-FETs, while ambipolar operation ($\phi_{bn} \approx \phi_{bp}$) is interesting for polarity controlled SB-MOSFETs and light emitting devices [45]. Importantly, the current in the devices described so far is limited by the SBH.

B. Workfunction-Induced Doping

Brattain and Bardeen [46] first reported an experimental observation that could be explained as metal-induced doping. In their report, a thin layer of p-type conductivity is believed to be induced near the surface of the n-type bulk Ge via a Schottky point-contact, which resulted in the bipolar-like amplification. Although noticed by only a few readers or authors, later on many reports actually followed this "scaled point-contact transistor" idea as discussed further in this section.

In this section, we first develop the general analytical understanding of workfunction-induced doping in 1-D Schottky contacts. Thereafter, we discuss the case of 2-D gated Schottky contacts, which is important for future CMOS devices, such as ED-TFETs.

1) 1-D Schottky-Based Devices: Excessive band bending near the MS interface may result in charge carrier inversion (similar to gate-induced inversion in MOSFETs) as shown in Fig. 1(b). This will induce a bipolar-type behavior in an otherwise unipolar 1-D Schottky diode, which could be of interest to BTBT devices. As in a MOS capacitor [1], we define the onset of strong inversion near the interface when the inversion charge carrier density is equal to the background doping concentration (N_d for n-type, N_a for p-type) of the semiconductor and derive the conditions for its occurrence.

For an n-type semiconductor, as shown in Fig. 1(b), the condition of strong inversion at the interface would result in E_F to lie below E_{FI} with an energy difference $q\psi_{BI} \geq q\psi_B$, where $q\psi_B = kT \cdot \ln(N_d/n_i)$. The latter represents the relative position of E_F from E_{FI} in the bulk region as defined by the background doping. This leads to the condition that at the interface $\phi_b \geq u_T \cdot \ln(N_c/n_i) + \psi_B$. Therefore, for strong inversion and, thus, bipolar p-n junction like behavior, the following conditions hold.

For an n-type semiconductor

$$\phi_b = (\phi_m - \chi_s)/q \geq u_T \cdot \ln\left(\frac{N_d}{n_i}\right) + u_T \cdot \ln\left(\frac{N_c}{n_i}\right). \quad (3)$$

For a p-type semiconductor

$$\phi_b = (E_g - \phi_m + \chi_s)/q \geq u_T \cdot \ln\left(\frac{N_a}{n_i}\right) + u_T \cdot \ln\left(\frac{N_v}{n_i}\right). \quad (4)$$

Using Boltzmann's approximation ($n \ll N_c$ or $p \ll N_v$), for the hole concentration in n-type semiconductors, we can write

$$p = n_i \cdot \exp\left(-\frac{\psi_{BI}}{u_T}\right) = n_i \cdot \exp\left(\frac{\phi_b - E_g/2q}{u_T}\right)\sqrt{\frac{N_v}{N_c}}. \quad (5)$$

Likewise, for the electron concentration in p-type semiconductors

$$n = n_i \cdot \exp\left(\frac{\psi_{BI}}{u_T}\right) = n_i \cdot \exp\left(\frac{\phi_b - E_g/2q}{u_T}\right)\sqrt{\frac{N_c}{N_v}}. \quad (6)$$

The above-mentioned equations indicate that for a suitable ϕ_m, that governs ϕ_b, charge carriers of opposite polarity type from the background doping can be induced near the interface of a 1-D Schottky contact. This creates a very shallow p-n junction near the MS interface where drift-diffusion or possibly even BTBT governs the current, which is different from conventional SB-based devices, where ϕ_b at

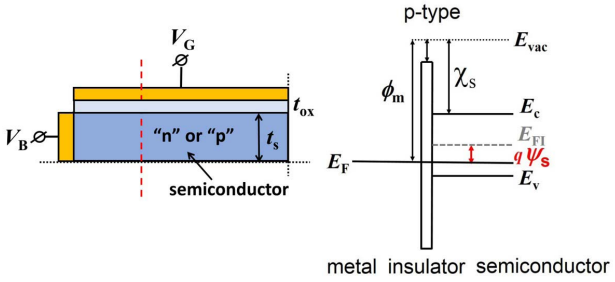

Fig. 4. Schematic cross section of a UTB device with 2-D gated Schottky contact for workfunction or bias-induced ED (left). The energy band diagram for a p-type formed region perpendicular to the gate along the red dashed line (right).

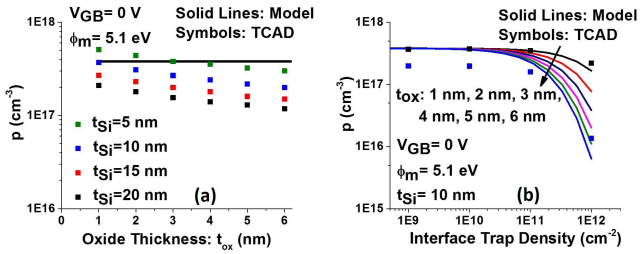

Fig. 5. Induced hole concentration for an Si/SiO_2-gated Schottky structure (see Fig. 4) with $\phi_m = 5.1$ eV for (a) varying oxide thicknesses with ideal interfaces and (b) varying interface trap densities. In the TCAD simulations [50], a uniform distribution of both donor and acceptor traps across the bandgap [1] has been assumed. In the simulations, the carrier density was extracted at a lateral distance of 0.5 μm from the Schottky side contact.

the interface solely controls the emission of charge carriers. Further note that according to (5) and (6), the induced charge carrier concentration is independent of N_d or N_a.

Such 1-D Schottky-based p-n junctions have been reported earlier using TCAD simulations for a vertical bipolar junction transistor (BJT) structure [47] and for a GaAs tunnel diode [48]. For the tunnel diode, however, Fermi–Dirac statistics should be applied and consequently (5) and (6) do not hold. Nonetheless, a suitable ϕ_m is still required for a p-n junction formation.

In the case of an intrinsic semiconductor, where $\psi_B = 0$, (3) and (4) can be transformed into the following equations for p-type doping:

$$\phi_m \geq \chi_s + \frac{E_g}{2} \tag{7}$$

and n-type doping

$$\phi_m \leq \chi_s + \frac{E_g}{2}. \tag{8}$$

By using metals with different workfunctions, it is possible to make an intrinsic semiconductor p-type or n-type locally via the ED approach. The term $\chi_s + (E_g/2)$ is essentially the position of Fermi level in the intrinsic semiconductor, i.e., its workfunction ϕ_s.

2) Gated Schottky-Based UTB Devices: In this section, we discuss the ED concept in devices in which a dielectric layer is placed between the metal and semiconductor body. In addition, the semiconductor device makes use of a fully depleted (FD) UTB devoid of any depletion charge [49]. Fig. 4 shows a schematic cross section of the system under discussion, which is similar to an FD 2-D MOS system.

The potential drop across the device perpendicular to the gate electrode is given by the following equation:

$$V_{GB} = V_{ox} + \psi_s + \phi_m/q - \chi_s/q - (E_c - E_{FI})/q \tag{9}$$

where V_{GB} is the applied gate potential difference between gate and semiconductor body, V_{ox} is the potential drop across the oxide, and ψ_s is the surface potential, i.e., shift in the Fermi-level from its intrinsic position. For not too high carrier concentrations ($n, p \ll N_c, N_v$), $V_{ox} \approx 0$ for an FD UTB with ideal interfaces, and $V_{GB} = 0$ for a purely workfunction-induced doping case.

Then, we obtain

$$\psi_s = (E_{FI} - E_F)/q = \chi_s/q - \phi_m/q - u_T \cdot \ln\left(\frac{n_i}{N_c}\right). \tag{10}$$

Equation (10) is the condition for ED in a UTB-gated Schottky system, which is equivalent to (7) for p-type doping ($\psi_s < 0$) and to (8) for n-type doping ($\psi_s > 0$). Analogous to the p-n junction formation in a 1-D Schottky contact, the concentration of the induced charge can be expressed as

$$p = n_i \exp\left(-\frac{\psi_s}{u_T}\right) \tag{11}$$

$$n = n_i \exp\left(\frac{\psi_s}{u_T}\right). \tag{12}$$

Fig. 5(a) shows the induced hole density against the oxide thickness for an Si/SiO_2-gated Schottky structure (Fig. 4) with $\phi_m = 5.1$ eV [using (7)]. Equation (10) indicates that the induced charge carrier density is independent of insulator and semiconductor thicknesses for UTB devices as $V_{ox} \approx 0$ in our simplified model. However, TCAD [50] produces somewhat different results. This is attributed to the presence of a high amount of mobile charge resulting in a finite V_{ox} (~30 mV at $t_{ox} = 6$ nm and $t_s = 10$ nm). Still, the model is useful for studying trends. For more accurate results, a numerical model can be derived [51], which is beyond the scope of this paper.

Now taking into account the effect of the interface trap charge (Q_{it}), (10) can be modified as

$$\psi_s = \chi_s/q - \phi_m/q - u_T \cdot \ln\left(\frac{n_i}{N_c}\right) + \left(\frac{Q_{it}}{C_{ox}}\right) \tag{13}$$

with $Q_{it} = -C_{it}\psi_s$ (assuming a uniform interface trap density), where $C_{ox} = \epsilon_{ox}/t_{ox}$ and $C_{it} = q^2 D_{it}$ are the oxide and interface trap capacitance per unit area, respectively, and D_{it} is the interface trap density [1]. Rearranging the terms in (13) gives the following condition for the workfunction-induced doping including the effect of interface states:

$$\psi_s = \frac{\left(\chi_s/q - \phi_m/q - u_T \cdot \ln\left(\frac{n_i}{N_c}\right)\right) \cdot C_{ox}}{(C_{it} + C_{ox})}. \tag{14}$$

Equation (14) along with (11) and (12) expresses the essential condition for induced ED in a gated Schottky device with interface trap charge. It shows that the ED reduces with

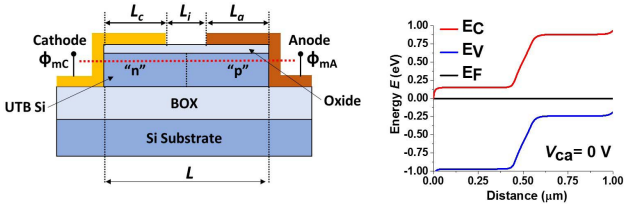

Fig. 6. Schematic cross section of the CP p-n diode (left) and its energy band diagram along the red dotted line at equilibrium (right). $\phi_{mC} = 4.17$ eV and $\phi_{mA} = 5.1$ eV are cathode and anode metal workfunctions, respectively. L_c and L_a denote cathode and anode gate lengths, respectively. L_i denotes the length of the intrinsic region, i.e., the gap between the two electrodes. The thickness of UTB Si (t_{Si}) is 20 nm and gate oxide thickness (t_{ox}) is 5 nm. [19].

an increase in interface trap density. From Fig. 5(b), where the induced charge concentration is plotted against the interface trap density using (14), it can be seen that the effect of interface traps is more pronounced for a larger oxide thickness. The charge concentration is reduced by a maximum of two orders in magnitude when the trap density is increased to 10^{12}/cm^2 for an oxide thickness of 6 nm.

The physics of gated Schottky contacts discussed earlier lays the foundation for the charge plasma (CP) concept as applied to FD UTB devices such as the TFET. This we discuss in the next paragraph.

3) Charge Plasma Devices: Hueting *et al.* [19] proposed to adopt two different workfunction metals to induce different polarities of charge carriers in the semiconductor. The schematic cross section of the so-called CP p-n junction diode is shown in Fig. 6. The CP diode comprises a gated anode and a gated cathode with metals of different ϕ_m values. From (12) to (14), it can be concluded that for the anode region, a high ϕ_m is required, while the opposite holds for the cathode region.

Fig. 6 also shows the energy band diagram of a CP diode along the lateral direction as obtained from 2-D TCAD simulations indicating that a p-n junction has formed. The band diagram is similar to a typical chemically doped p-n junction with some key differences, which were also highlighted in [30]. The quasi-neutral regions of this diode are formed by the ED gates. A typical feature of the lateral ED configuration is that the potential distribution is linear in the intrinsic gap region because of the absence of impurities, unlike a conventional p-n junction, which has a parabolic potential profile in the depletion region. The built-in electric field in an impurity-doped p-n junction is formed by fixed donor or acceptor ions near the junction to balance drift and diffusion components at equilibrium. This built-in field also exists in the CP p-n diode but is primarily formed by the workfunction difference at the edges of the gated regions. Furthermore, the band bending near the electrodes is attributed to the 2-D fringe field effect. Analytical drift-diffusion models for the I–V curves in the CP p-n diode [52] also showed good agreement with TCAD simulations.

In the first experimental realization by Rajasekharan *et al.* [20], Pd was employed for the anode contact and Er for the cathode. The fabricated device showed good rectifying behavior with a low constant leakage current of 1 fA/μm and an ON/OFF-current ratio of around 10^7 at $V_D = 1$ V

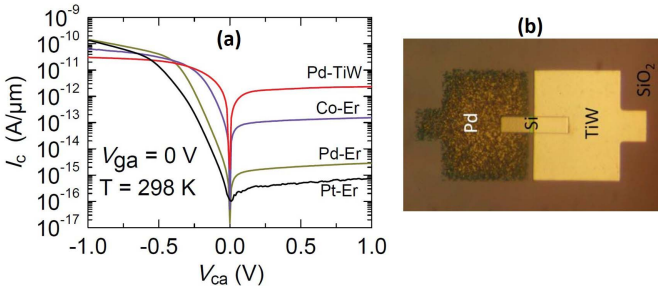

Fig. 7. (a) Current-voltage (I_c–V_{ca}) characteristics for various valence and conduction level metal combinations Pt–Er, Pd–Er, Co–Er, and Pd–TiW on either side of silicon. $L_a = L_c = 0.9$ μm and $L_i = 3$ μm (see Fig. 6). The substrate potential (V_{ga}) was kept at 0 V. (b) Top view of a realized CP diode showing the effect of placing a wafer with high workfunction (Pd) and low workfunction (TiW) metal islands in a chemical etching solution. The combination of the metals with the solution formed an electrolyte cell, which resulted in the corrosion of highest workfunction (Pd) metal [20].

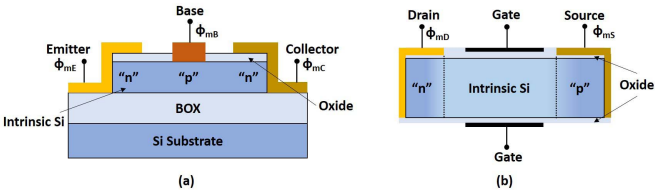

Fig. 8. Schematic cross section of the CP-based (a) lateral BJT [21] and (b) TFET [22]. The "n" and "p" indicate electrostatically doped regions.

forward bias and room temperature. Fig. 7(a) shows the measured I–V characteristics of various fabricated CP diodes with different combinations of anode and cathode metals. The experimental results indicate that both the hole and electron current are important for the CP diode. The current increases as we reduce the anode workfunction by replacing Pt with Pd or Co, or conversely, by increasing the cathode workfunction by replacing Er with TiW. By using the same metal for anode and cathode contact and the substrate as back gate, MOSFET characteristics were obtained [20].

The CP-based ED concept has been extended to various other devices. Kumar and Nadda [21] proposed and investigated the CP-based lateral BJT by replacing the doped emitter, base, and collector regions of a conventional bipolar device with ED regions using metals with different workfunctions as shown in Fig. 8(a). The authors proposed Hf ($\phi_{mE} = 3.9$ eV) for the emitter, Pt ($\phi_{mB} = 5.65$ eV) for the base, and Al ($\phi_{mC} = 4.28$ eV) for the collector electrode, thereby achieving an n$^+$-p-n configuration. The results obtained from 2-D TCAD simulations show similar device characteristics but a higher current gain compared with the conventional impurity-doped counterpart with the same dimensions.

Another device based on the CP concept is the doping-less TFET, proposed by Kumar and Janardhanan [22], shown in Fig. 8(b). Similar to the CP-BJT, again the impurity-doped regions of the conventional TFET were replaced with ED regions by employing metals with a different workfunction: Hf for the n-type drain and Pt for the p-type source. The performance of the CP-based doping-less TFET was found to be similar to the conventionally doped TFET with the same device geometry.

TABLE I
SUMMARY OF VARIOUS REPORTED ELECTROSTATICALLY DOPED MATERIALS AND DEVICE CONCEPTS TILL DATE. THE NOTATION (exp.) DENOTES EXPERIMENTALLY DEMONSTRATED CONCEPT, WHILE OTHERS HAVE BEEN INVESTIGATED VIA MODELING AND TCAD SIMULATION ONLY

Material	SB based devices	Workfunction-induced ED	Bias-induced ED
Si, Si UTB and Si Nanowire	SB-MOSFETs (exp.) [17], [18], FinFET (exp.) [41], Si nanowire based SB-MOSFETs (exp.) [43], reconfigurable FETs (exp.) [23]–[25]	CP based p-n diode (exp.) [19], [20], BJTs [21], [47], [63], [64], TFET [22], IMOS [65], Junctionless transistor [66], Biristor [67], SiGe-on-insulator MOSFET [68], graded channel MOSFET [69]	EH bilayer TFET [35], [36], EH bilayer TFET (exp.) [37]
CNT	SB-MOSFETs [31], [32], [42], Light emitting SB-FET (exp.) [45]		p-n diode (exp.) [30], FET (exp.) [56]
Graphene		Graphene ED [28]	Graphene ED [53], Graphene FET (exp.) [26], [27], [29], [54], [55]
III-V materials	GaN n-type SB-MOSFET (exp.) [70]	GaAs Tunnel diode [48], GaN n-MOSFET [71], InAs TFET [72]	GaAs EH Bilayer (exp.) [73]
Polycrystalline materials		CP based poly-Si TFT [74], IGZO TFT (exp.) [75]	
2-D materials	n-type, p-type SB-MOSFET (exp.) [76], [77]		2-D transistors [33], [34]

Other proposed CP-devices are summarized in Table I. So far most of these architectures have not been experimentally realized. Similar ideas for graphene doping via metal contacts have also been reported [26]–[29], [53]–[55].

C. Bias-Induced Doping

The applied electric field at the MS interface also plays a decisive role in governing the electrostatics and thereby charge induction in the UTB semiconductor. It can be argued whether the principle of bias-induced doping is not simply based on the conventional field effect. However, in conventional FETs, the charge carriers originate from doped semiconductor regions in close vicinity (like doped S/D regions), whereas in the ED concept, the charge carriers originate from a metal electrode, which is in direct contact with the semiconductor body. We hereby again refer to Fig. 4. We have similar conditions as for the workfunction-induced doping (10), with an additional term to account for nonzero V_{GB}

$$\psi_s = V_{GB} + \chi_s/q - \phi_m/q - u_T \cdot \ln\left(\frac{n_i}{N_c}\right). \tag{15}$$

For a bulk or partially depleted channel, similar relations can be obtained using a nonzero V_{ox} term in (9). The term $(\chi_s/q - \phi_m/q - u_T \cdot \ln(n_i/N_c))$ is actually the workfunction difference $(\phi_m - \phi_s)/q$, which is zero in the case of a purely bias-induced ED. In this case, it is easy to understand that a positive V_{GB} will induce n-doping, while a negative V_{GB} will induce p-doping. Furthermore, the effect of interface traps can be accounted for as

$$\psi_s = V_{GB} + \chi_s/q - \phi_m/q - u_T \cdot \ln\left(\frac{n_i}{N_c}\right) + \left(\frac{Q_{it} + Q_{inv}}{C_{ox}}\right) \tag{16}$$

with Q_{inv} is the mobile inversion charge. Again, the interface traps mainly affect the electrostatics, hence ED, but ideally, only the mobile charge should be controlled by the gate. Note that earlier modeling work on the I–V curves of asymmetric double-gate (DG) devices [51] could be used to derive a model for bias-induced doping including traps.

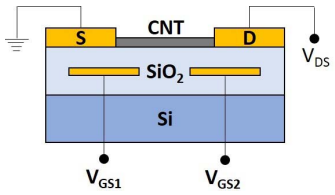

Fig. 9. Schematic cross section of the CNT p-n diode [30]. The split gate configuration was used to electrostatically induce a lateral p-n junction. Biasing $V_{GS1} < 0$ would give a p-type region in the adjacent CNT channel and $V_{GS2} > 0$ would result in an n-type region.

The simultaneous induction of p-type and n-type charged regions in a semiconductor body via an applied field can be realized using a dual (or multiple) gate structure. By biasing two gates with opposite polarities, electrons and holes can be simultaneously induced in a semiconductor body as analytically explained by (15) and (16). Depending on the relative position of such gates, electrostatically induced local bipolar regions have been reported both in lateral [30] and in vertical structures [35] as discussed in the next paragraph.

1) Lateral p-n Junction: Bias-induced ED was first experimentally demonstrated in a CNT system [30] where a lateral p-n junction diode was formed adopting a split gate configuration as shown in Fig. 9. Biasing a first gate electrode with a positive voltage with respect to the CNT body resulted in an n-type doping of a CNT channel region adjacent to it. Similarly, a negative voltage with respect to the CNT body at a second gate resulted in a p-type doping. This led to the formation of a lateral p-n junction diode in the CNT channel. The experimentally fabricated device showed rectifying characteristics of a p-n junction diode with an ideality factor close to one. In addition, the same polarity biases at both gate electrodes resulted in an n-channel or p-channel FET. BTBT was also observed in CNTs [56], demonstrating an ED p-n junction, which could be interesting for the TFET.

2) Vertical p-n Junction: Electron–Hole Bilayer: An opposite polarity gate bias configuration in the vertical direction can be utilized to form bias-induced electron-hole bilayer (EHB) as shown in Fig. 10. This was demonstrated in [57] and [58] using a DG $SiO_2/Si/SiO_2$ system.

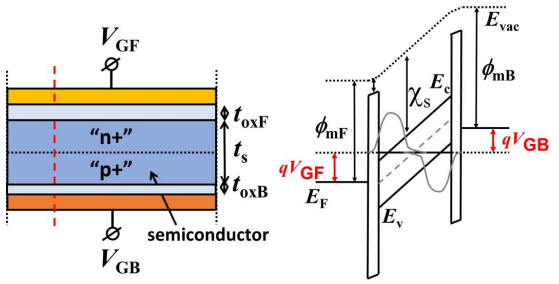

Fig. 10. Schematic cross section of the EHB concept (left). Energy band diagram perpendicular to the gates along the red dashed line (right). By enforcing an opposite polarity bias between the top and the bottom gate, a tunnel junction can be formed. The wave function curves represent the electron (left) and hole (right) distribution in the EHB structure for illustration purposes.

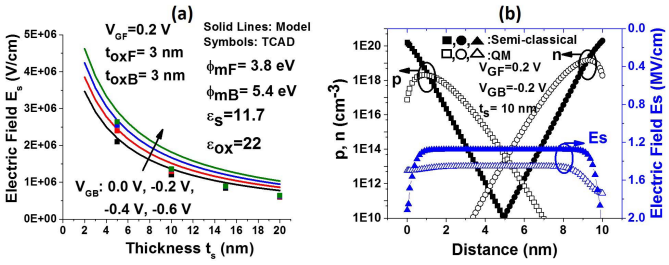

Fig. 11. (a) Vertical electric field in the HfO_2/Si/HfO_2 EHB structure (refer to Fig. 10) for various semiconductor body thicknesses. QM effects have not been taken into account both in the model (17) and TCAD simulation [50]. (b) TCAD simulation of charge carrier distribution and electric field profile in the vertical direction along the red dashed line of Fig. 10 with $t_s = 10$ nm, $V_{GF} = 0.2$ V, and $V_{GB} = -0.2$ V. TCAD simulation of the induced EHB at vertically opposite interfaces of a dual gate structure is shown using both semiclassical (using Poisson only) and QM (density-gradient model [61]) approaches. The detailed quantitative calibration of the QM model in TCAD is not the focus of this paper.

In the case of a relatively thick semiconductor with a partially depleted channel, the two metal gates do not have any electrostatic coupling, and therefore, the bias-induced charge near each gate can be independently described using (15) (for $n, p \ll N_c, N_v$). In the case of a dual asymmetric gate structure with an FD UTB channel, however, the electrostatic interaction between the two gates needs to be taken into account. Analogous to the previous work of Lim and Fossum [59] and assuming a not too high charge carrier concentration, we derive the following equation for the vertical electric field in the semiconductor body for the EHB concept in the coupled dual gate system (see the Appendix):

$$E_s = \frac{(V_{GF} - V_{GB}) - (\phi_{mF} - \phi_{mB})}{\frac{\varepsilon_s}{\varepsilon_{ox}}(t_{oxF} + t_{oxB}) + t_s} \tag{17}$$

where the subscripts F and B refer to the front and back of the structure, respectively. Fig. 11(a) plots E_s against the semiconductor body thickness t_s for an HfO_2/Si/HfO_2 EHB structure. Fig. 11(a) shows that TCAD simulations [50] are in good agreement with (17). Semiclassically, there will be an induced electron density near the top gate electrode if $\psi_{sF} > 0$ [refer to (23)] with an electron density at the interface $n = n_i \exp(\psi_{sF}/u_T)$. Similarly, if $\psi_{sB} < 0$ [refer to (24)], there will be an induced hole density near the bottom gate electrode

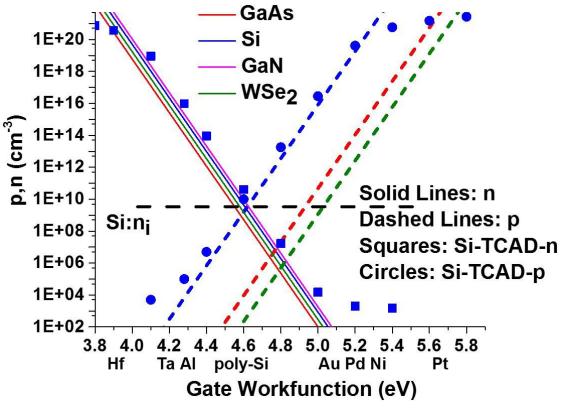

Fig. 12. Calculated induced carrier concentration (10) in "n-type" and "p-type" gated Schottky regions of the CP diode structure (refer to Fig. 6) with a varying workfunction of the gate electrode. The calculation is performed for different semiconductor channel materials (Si (E_g = 1.12 eV and χ_S = 4.07 eV), GaAs (E_g = 1.42 eV and χ_S = 4.07 eV), GaN (E_g = 3.39 eV and χ_S = 4.1 eV), WSe_2 (E_g = 1.56 eV and χ_S = 4.03 eV) [79]) in the UTB device. TCAD simulation (symbols) for Si shows good agreement with the model. In both the model and TCAD simulations, ideal interfaces have been assumed.

at the interface $p = n_i \exp(-\psi_{sB}/u_T)$. Obtaining closed-form solutions for ψ_{sF} and ψ_{sB} is, however, rather difficult. Moreover, quantum mechanical (QM) effects can change this picture [60] as qualitatively shown in Fig. 11(b) using TCAD simulation. The effect of fixed or interface charge can also be accounted for as described by (26) (see the Appendix) by assuming nonzero Q_{fF} and Q_{fB}.

Lattanzio *et al.* [35], [36] have applied the EHB concept to a DG-TFET geometry. This transistor was conventionally symmetrically biased for better electrostatic control over the channel. Under asymmetric bias, a bias-induced EHB forms in the channel. For a certain top–bottom bias difference (~0.1–0.5 V), BTBT of charge carriers in the EHB p-n junction occurs, which results in an increase in the drain current [60]. In this case, the direction of tunneling is parallel to the gate field. This results in more ON-state tunneling current compared with, e.g., the doping-less TFET [22] because of the large tunneling surface area and a stronger electrostatic control over both n-type and p-type regions in the subthreshold region. However, there has been some debate on the effectiveness of the EHB formation [37], [62]. In [37], experimentally realized EHB-TFET structures were reported and it was argued that conditions to meet efficient BTBT and the formation of the EHB cannot simultaneously be satisfied: there is a tradeoff between the induced field and quantum-confinement.

III. Electrostatic Doping Approaches: Discussion

Table I provides a summary and classification of various ED device concepts. Based on this literature, it can be established that a high carrier density of both p- and n-type (10^{18}–10^{20} cm^{-3}) can be electrostatically induced in UTB devices, particularly for narrow bandgap semiconductors. Fig. 12 shows the induced charge carrier concentration using (10) for gated Schottky regions of the UTB CP

device (refer to Fig. 6) (see also [78] where a measured effective ED density of 10^{19} cm^{-3} was reported). A high carrier density can be induced by adopting a suitable workfunction for the gate electrode. The effect of the bandgap is more pronounced for holes, while for electrons, ED is largely governed by the electron affinity of the material and the metal workfunction.

With this understanding, we next discuss the competitiveness of ED for future CMOS as compared with impurity doping. We also address the possible drawbacks of ED.

A. Potential ED Devices for Future CMOS

Among various reported ED devices discussed so far, the SB-MOSFET, the reconfigurable FET, and the TFET based on FD semiconductors and 2-D materials appear to be the most promising for future CMOS.

The SB-MOSFET is by far the most experimentally investigated device in this category and a detailed review [18] discussed the competitiveness of this technology for ultimately scaled CMOS. In addition to the technology benefits in terms of scalability to sub-30-nm gate lengths and lower temperature processing with a fewer lithography steps, SB-MOSFETs offer performance benefits in terms of improved I_{OFF} and elimination of the parasitic bipolar action. Further because of the low parasitic S/D resistance (1% of the total resistance), the SB-MOSFETs potentially offer a relatively high cutoff frequency (f_T). An SB-pMOS with an f_T of 280 GHz was reported [18]. The same article presented an SB-CMOS ring oscillator with only 30-ps gate delay. Xiong *et al.* [80] also claimed that for relatively low SB heights, metal S/D UTB devices do offer performance benefits over doped S/D devices due to improved parasitics. In addition, the SB-MOSFET concept has been experimentally demonstrated in alternative materials, such as CNTs and Si-nanowires, and in different device designs, such as FinFETs. However, further optimization of the SB height is needed for CMOS competitive SB-pMOS and nMOS devices with improved I_{ON} and I_{OFF}. The barrier height lowering techniques such as the use of a thin interfacial layer are being explored but are technologically challenging from process integration viewpoint [18].

The reconfigurable nanowire FET (RFET) [24], [78] is also a conceptually attractive new device due to its switchable functionality. The performance of different experimentally demonstrated RFETs and their maturity for logic circuit applications has been reviewed in [78]. Next to the polarity control, the symmetric transfer characteristic for n-type and p-type FET operation is important for low power CMOS. The latter must be obtained by fine tuning the SBHs, tunneling probabilities and channel mobilities of electrons and holes. The extra gate can additionally suppress the OFF-state current of the RFET [24]. This is encouraging for devices with narrow bandgap channel materials which otherwise suffer from high leakage currents.

Furthermore, a propagation delay of 35 ps at $V_{DD} = 5$ V was extracted for realized RFET CMOS inverter, which can be further optimized. The reconfigurable NAND/NOR logic operation was also demonstrated using a lower number of FETs than required for conventional CMOS for the same functionality [78]. Moreover, the RFET concept is not limited to nanowires and can be translated to any other low dimensional CMOS compatible material and geometry as required for efficient channel electrostatics. However, the management of a large number of programming gate signals could be a concern in high level circuitry.

Novel ED TFET concepts, such as the CP-TFET [22] and the EHB-TFET [81], though mostly investigated with TCAD only, have been reported to be competitive to conventionally doped counterparts and therefore could be interesting for future low power CMOS switches. Lattanzio *et al.* [81] estimated that germanium-based EHB TFETs outperform doped DG-TFETs in terms of intrinsic delay. The intrinsic delay for a single EHB device was less than 1 ns at $V_{DD} = 0.25$ V with a theoretical maximum operating frequency of 1.39 GHz.

Other recently proposed ED TFET designs [34], [72] also offer distinct advantages. Ilatikhameneh *et al.* [34] proposed to enhance the lateral field in a lateral ED tunnel junction using low-k dielectric spacers in between high-k gate dielectrics of the gated regions. Along with the advantages of the ED and enhanced electric field, such dielectric engineered TFET also offers a reduced sensitivity of the device performance to the gates spacing and gate oxide thickness compared with the previously discussed ED-TFETs [22], [79].

Pan and Chui ([72] and references therein) discussed an ED-TFET design where the gate electrodes consisting of two different workfunction metals are physically and electrically shorted. This design addresses the limitation of minimizing the tunnel width of previous ED-TFET designs, which is limited by the lithography resolution of the intergate spacing. Also this design overcomes the limitations of bias-induced quantum confinement effects, which could adversely affect the device performance as in the EHB-TFET [60]. However, the abruptness of the gate metals heterojunction to prevent metal intermixing and workfunction pinning could be technologically challenging.

Transistors based on 2-D materials, such as TMDs [33], [76], [77], [79] and graphene [29], [55], are also interesting candidates for future low-power and high-speed CMOS [14]. In this class of transistors, ED is the most applied doping technique. Other than the mostly reported n-type MoS_2 device [76], recently, a p-type MoS_2 transistor [77] was also demonstrated with an I_{ON}/I_{OFF} ratio of 10^4 employing a Schottky contact with high workfunction MoO_x for efficient hole injection. However, obtaining an MS interface with a low contact resistance presently poses the key challenge for technology development.

In summary, the performance of ED devices with well-optimized interface electrostatics could be at par with impurity-doped devices. However, more extensive experimental investigation is required to confirm whether ED could replace conventional doping in mainstream Si-CMOS technology. Nevertheless, ED could be the potential solution for alternative materials systems, such as Graphene, CNTs, TMDs, and nanowires, where conventional impurity doping is a big challenge. The ED is also interesting for innovative device concepts, such as EHB-TFETs and RFETs, which could not be realized using conventional doping.

B. ED: Limitations and Drawbacks

Although ED-based approaches look very promising, there are still some limitations and drawbacks, which need to be addressed from a technology perspective.

First, the ED concept is usually designed assuming ideal MS contacts. However, there has been much experimental evidence that the observed SBHs (ϕ_b) and, thus, "effective" workfunctions on various MS systems deviate from their bulk values and the linear relationship between ϕ_b and ϕ_m may not hold in certain cases [39]. The assumption of an ideal, abrupt, and nonreactive MS interface does not hold in practice. The chemical reactivity between a metal and a semiconductor, interdiffusion, and the presence of interface dipoles make the observed ϕ_b to deviate from the ideal Schottky–Mott relation [82], where ϕ_b has a linear relationship with ϕ_m. Recently, Tung [83] has reported a detailed review on physics and chemistry of SBHs of MS interfaces. The author reviewed various strategies of modifying ϕ_b at the MS interface by an insertion of a thin ($\approx$2 nm) interfacial layer. This avoids chemical interdiffusion and also decouples the electron states in the semiconductor from the influence of the metal [39]. ϕ_b obtained from such an MIS system with a thin interfacial layer shows a much stronger dependence on the metal workfunction than an MS interface without any intentionally grown interfacial layer [83], [84]. Such a thin interfacial layer could be a solution for the realization of workfunction-induced ED devices with a better control over ϕ_b [85]. Moreover, the presence of additional dipoles from the interfacial layer opens up the possibility to further tune ϕ_b. Since, most ED devices can be realized via low temperature processing, the metastability of the interfacial layer should also not be a big concern.

Second, metal workfunction variation could also be a concern [86], [87], particularly, for metal nitride gates, such as TiN [88] due to their polycrystalline nature. This could have serious implications on the effectiveness and uniformity of workfunction-induced doping and device variability.

Third, implementing several metals in galvanic contact may lead to corrosion during wet processing [see Fig. 7(b)]. This effect was observed for several combinations of electrode metals [20]. Rather than wet etching, other metal patterning approaches are recommended, such as dry etching, damascene, or liftoff.

Fourth, the scaling approach for ED devices may be different from chemically doped ones as reported in the recent study by Ilatikhameneh *et al.* [33]. The atomistic simulations of such ED 2-D material transistor showed a different behavior from devices with same equivalent oxide thickness (EOT) but with varied physical oxide thicknesses. The authors therefore proposed a new scaling theory and design guidelines for such ED devices where the actual physical oxide/dielectric thickness is more critical unlike conventional transistors where scaling is regulated by the EOT. The authors proposed to employ ultrathin wide bandgap oxides as gate dielectric for both optimized ED and suppressed gate leakage.

Fifth, in the case of wide bandgap semiconductors such as GaN with $E_g = 3.4$ eV and electron affinity $\chi_s = 4.1$ eV, the condition for the workfunction-induced n-type doping, i.e., $\phi_m < (\chi_s + E_g/2)$ can be satisfied with a lower workfunction metal such as Al. However, similar p-type ED in GaN would require a workfunction higher than 5.8 eV (see Fig. 12), which is not available. A possible solution to this problem in wide bandgap semiconductors could be the bias-induced doping approach with a suitable workfunction metal.

Furthermore, in general, for any material, the smallest lateral spacing between the gates is desired for optimized performance of ED devices [33], which is largely limited by the lithographic resolution. This becomes more critical in the case of wide bandgap materials as the highly resistive intrinsic gap between the two ED regions may lead to a reduced ON-current and very high turn-ON voltages. Recently, Pan and Chui ([72] and references therein) discussed to overcome this limitation in their new ED-TFET design. Such ideas can be explored for other ED devices as well.

Finally, the presence of interface traps could adversely affect the effectiveness of ED as discussed before. The use of a thin interface layer is a potential solution to minimize the effect of interface traps on induced charge [83], [85].

IV. Conclusion

Electrostatic doping (ED) offers an alternative to chemical doping in nanometer-scale devices. Recent articles have treated the applicability of ED in a host of devices based on different materials ranging from Si to CNT, graphene, and other 2-D semiconductors.

In this paper, various reported ED approaches were reviewed. Using basic 1-D electrostatic relations, we established the conditions for ED and derived simple expressions for induced charge carrier densities as applied to different ED approaches. The derived expressions highlight the role of metal and semiconductor workfunctions, energy bandgap, electron affinity, and applied electric field, and the interplay between them for the induced ED.

From various reported results and the developed analytical understanding, it can be concluded that ED techniques can be utilized to induce high charge concentrations in UTB active devices. In general, ED is more effective for narrow bandgap semiconductors.

ED can be obtained by low temperature processing with a fewer lithography steps. The performance of ED devices is also found competitive with that of conventional counterparts especially for SB-MOSFETs, RFETs, and TFETs. However, many of these device architectures, in particular TFETs, have only been studied via modeling or computer simulations. Experimental realization of such structures will assist in evaluating the true merit of these device ideas for alternative material systems and innovative device concepts for future CMOS.

The effective workfunction variation, presence of interface traps, processing with multiple metals, and applicability to wide bandgap materials are identified as the current major limitations to ED approaches. These need to be extensively addressed for developing future CMOS technology.

Appendix

We focus on the formation of the dual gate-induced EHB and derive a closed-form analytic expression-based 1-D elec-

trostatics. For doing so, we neglect quantum mechanical (QM) effects as reported before by Trivedi and Fossum [89] for dual gate silicon-on-insulator (SOI) MOSFETs and more recently, Alper *et al.* [60] for EHB-TFET systems.

From Fig. 10, we can write

$$V_{GF} = V_{oxF} + \Delta\phi_{mF} + \psi_{sF} \tag{18}$$

$$V_{GB} = V_{oxB} + \Delta\phi_{mB} + \psi_{sB} \tag{19}$$

where V_{GF} and V_{GB} are front and back gate voltages, V_{oxF} and V_{oxB} are voltage drops across front and back oxides, $\Delta\phi_{mF}$ and $\Delta\phi_{mB}$ are front and back gate-body workfunction difference, and ψ_{sF} and ψ_{sB} are front and back surface potentials. Now applying Gauss' law at both surfaces of the semiconductor body, we can write

$$V_{oxF} = \frac{1}{C_{oxF}}(\varepsilon_s E_{sF} - Q_{fF} - Q_{itF}) \tag{20}$$

$$V_{oxB} = \frac{1}{C_{oxB}}(-\varepsilon_s E_{sF} - Q_{fB} - Q_{itB}) \tag{21}$$

where C_{oxF} and C_{oxB} are the front and back areal oxide capacitances, E_{sF} is the electric field in the body at the front surface, ε_s is the semiconductor dielectric constant, Q_{fF} and Q_{fB} are fixed charge densities, and Q_{itF} and Q_{itB} are the interface trapped charge densities at front and back surfaces, respectively. Since we assume full depletion, the electric field is constant inside the body

$$\psi_{sF} - \psi_{sB} = E_{sF} t_s = -E_{sB} t_s \tag{22}$$

where t_s is the thickness of the body and E_{sB} is the electric field in the body at the bottom surface. Now, for simplicity sake, we neglect fixed charge at both surfaces and a relatively small inversion charge, we can write

$$\psi_{sF} = V_{GF} - \frac{\varepsilon_s E_{sF}}{C_{oxF}} - \Delta\phi_{mF} \tag{23}$$

$$\psi_{sB} = V_{GB} + \frac{\varepsilon_s E_{sF}}{C_{oxB}} - \Delta\phi_{mB}. \tag{24}$$

Subtracting (24) from (23) and replacing the term $\psi_{sF} - \psi_{sB}$ with $E_{sF} t_s$ and substituting $C_{oxF} = \varepsilon_{ox}/t_{oxF}$ and $C_{oxB} = \varepsilon_{ox}/t_{oxB}$, we obtain

$$E_s = \frac{(V_{GF} - V_{GB}) - (\phi_{mF} - \phi_{mB})}{\frac{\varepsilon_s}{\varepsilon_{ox}}(t_{oxF} + t_{oxB}) + t_s}. \tag{25}$$

The effect of the interface traps on the electrostatics of the EHB-TFET can also be incorporated here. Consider a device in which $t_{oxB} = t_{oxF} = t_{ox}$ with the same uniform interface trap charge density at both semiconductor surfaces, then we have a constant areal interface capacitance C_{it}, and consequently, $Q_{itF} = C_{it} \cdot \psi_{sF}$ and $Q_{itB} = C_{it} \cdot \psi_{sB}$. Then, we obtain

$$E_s = \frac{(V_{GF} - V_{GB}) - (\phi_{mF} - \phi_{mB})}{\frac{2\varepsilon_s}{\varepsilon_{ox}} \cdot t_{ox} + \left(1 + \frac{C_{it} \cdot t_{ox}}{\varepsilon_{ox}}\right) \cdot t_s}. \tag{26}$$

Hence, for the same biasing conditions, we can conclude that the higher C_{it}, i.e., the higher trap density, the lower E_s, and therefore, the effectiveness of the EHB concept.

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