1/f Noise and Switched Bias Noise Measurement in p-MOSFET with varying gate oxide thickness

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Abstract -- **MOS transistors are notorious for their low frequency noise, which increases with decreasing device size. Using a new noise measurement set up, the power spectral density of 1/f noise in MOSFETs decreases, if the transistors are switched "off" periodically (switched bias conditions)[1]. In this work, noise measurements on p-MOSFET are reported, with gate oxide thickness varying from 2 to 20 nm, keeping the electric field in the channel constant at 1.4 MV/cm. The switched bias noise and the reduction in the switched bias noise for p-MOSFET, are investigated as a function of the gate oxide thickness and the switching amplitude. Recently reported literature[2] on explanation for switched biased noise reduction is then compared with our measurement results and some explanations are proposed.**

Keywords – **1/f noise; MOSFET LF noise; switched bias; noise reduction; p-MOSFET**

I. INTRODUCTION

Charge transport in semiconductor devices is fundamentally accompanied by noise, which limits the signal processing capabilities of electronic circuits. MOS transistors are notorious for their low frequency noise. This low frequency noise contribution becomes larger with decreasing MOS device sizes, and is hence, of increasing concern. There are several theories and models, which are available in literature[3-5], which attempt to explain the 1/f noise behaviour. Although they differ in detail, they are based on the mobility fluctuation model expressed by the Hooge empirical relation, and the carrier density or number fluctuation model first introduced by Mc Whorter. The Unified model for the flicker noise proposed by Hung et.al.[6], incorporates both the number fluctuations and the surface mobility fluctuations. The physical principle behind the model is that the fluctuation in the occupancy of the oxide traps induces correlated fluctuations in the carrier number and surface mobility.

Previously, it has been shown that the noise power spectral density of the low frequency noise of MOSFETs decreases, if the transistors are switched "off" periodically[1]. A noise reduction of 6 dB is expected, with 50% duty cycle of the switching pulse [7].

This work presents the low-frequency noise and switched bias noise measurements on p-MOSFETs.

II. PMOST NOISE MEASUREMENT

The p-MOSFET on which the noise measurements are carried out have a substrate doping of 5×10^{17}. The p-MOSFET are available on wafers of different gate oxide thickness 2; 3.6; 7.5; 10 and 20 nm. The process steps are the same for all the wafers. The noise measurements are carried out on p-p-MOSFET with geometry W:L=10:1 and W:L=10:0.3 (W and L are the width and length of the p-MOSFET in µm). Fig. 1 shows the noise measurement set up. This set up is functionally similar to the one used by vander Wel et. al.[7]. The p-MOSFET on the wafer are a matched pair (identical in geometry and all electrical properties). The differential probe is used to cancel out the common mode signals. The bipolar cascode transistors ensure an almost constant drain voltage at the matched pair of p-MOSFET. The function of the resistors at the drain is to convert the differential drain current into an equivalent voltage, whose spectral density is then measured by a spectrum analyser. The noise measurement set up measures the drain current spectral density of the p-MOSFET. The switched bias voltage is applied to the gate of the p-MOSFET to periodically switch the transistors "off".

The first set of PMOST noise measurement involves changing the "off" voltage of the switching gate signal.

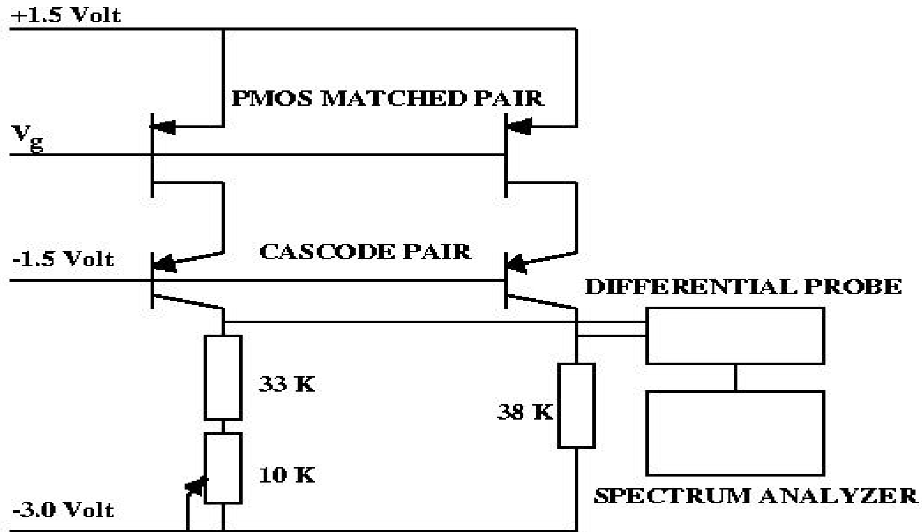

Fig.1. p-MOSFET noise and switched bias noise measurement set up

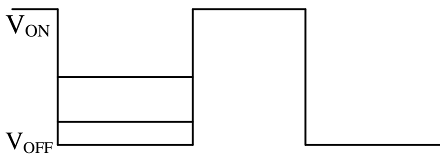

Fig. 2. The switching voltage applied to the gate of the p-MOSFET matched pair

The "off" voltage is systematically varied, and the corresponding switched bias noise is measured. See Fig. 2.

The second set of p-MOSFET noise measurements are carried out on wafers with different gate oxide thickness, 2; 3.6; 7.5; 10 and 20 nm. A constant drain current of 17 µA is forced through the p-MOSFET during each of the measurements. This ensures that the electric field in the channel is kept constant (1.4 MV/cm) in each case. The V_{GS}-V_T value is around 0.4 volts, which ensures that the p-MOSFET are indeed in saturation and also in strong inversion. The switching amplitude is kept constant at 1.2 V for each measurement. The noise measurements are averaged over 20 times. Also the noise measurements are done on 5-10 different devices with identical geometry on different locations on the wafer for a given gate oxide thickness.

III. RESULTS AND DISCUSSIONS

The results obtained for the first set of noise measurements (changing the off voltage) are shown in Fig. 3.

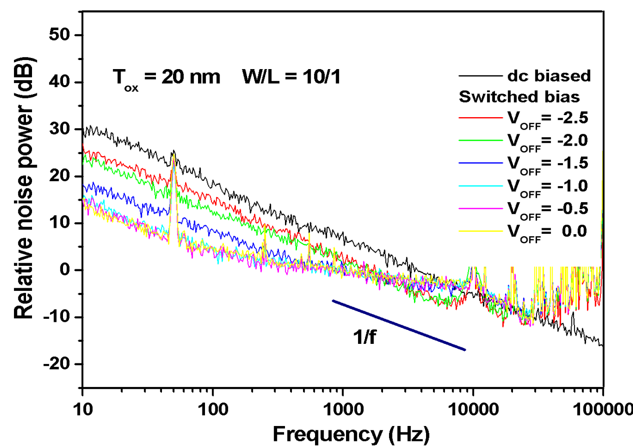

Fig. 3. Noise spectral density as a function of the "off" voltage for W:L=10:1

The low-frequency noise is measured on the linear portion of the noise spectrum at around 100 Hz. The noise reduction is the difference between the low-frequency noise and the noise measured when the gates of the p-MOSFET are periodically switched on and off. The measurements show that the low frequency noise decreases as the "off" voltage of the gate pulse decreases or when the switching amplitude is decreased (Fig. 3).

Fig. 4 shows the relation between the relative noise reduction and the "off" voltage of the switching gate pulse. Also shown, is the expected noise reduction, which is 6 db below the DC biased value, because of the 50% duty cycle of the switching pulse[7]. The noise reduction increases with increasing switching amplitude and then saturates.

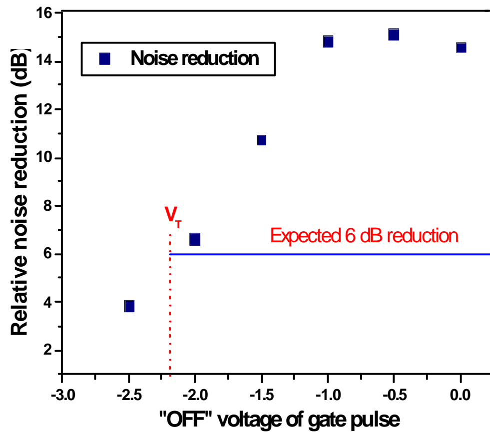

Fig. 4. Noise reduction as a function of the "off" voltage

The results of the p-MOSFET noise measurements as a function of varying t_{ox} is given in Fig. 5. The measurement results on transistors with W:L=10:1, show a distinct trend. The low-frequency noise decreases as the gate oxide thickness decreases. The results of measurements over different locations on the wafer show spread as indicated in Fig. 5.

The noise reduction (averaged over 5 devices on wafer) as a function of the changing t_{ox} is shown in Fig. 6. The switching amplitude of the gate pulse is kept constant (1.2 V) during each measurement. Also shown is the expected 6 dB noise reduction value.

The switched bias noise reduction for p-MOSFET with W:L=10:0.3 for different values of t_{ox} is shown in Fig. 7. The spread in the values of the low-frequency noise and the corresponding noise reduction, over 10 different locations on the wafer, is evident from Fig. 7.

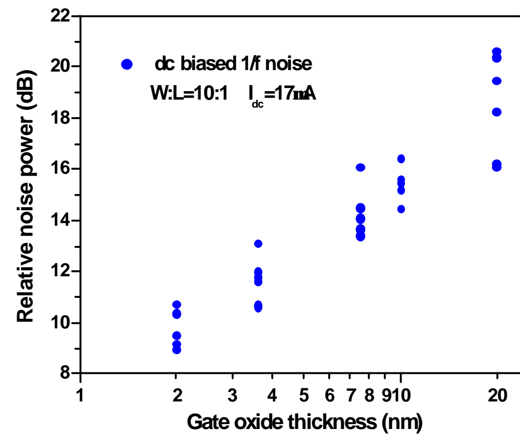

Fig. 5. Noise as a function of the gate oxide thickness W:L=10:1

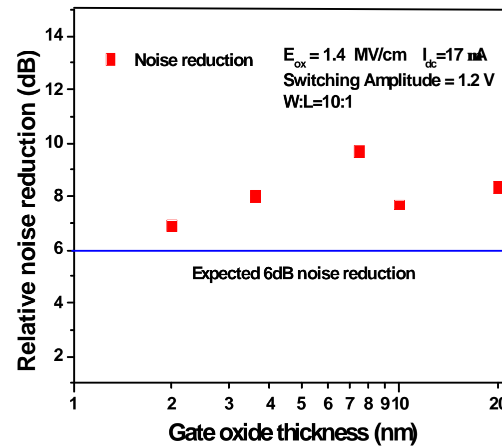

Fig. 6. Noise reduction as a function of gate oxide thickness W:L=10:1

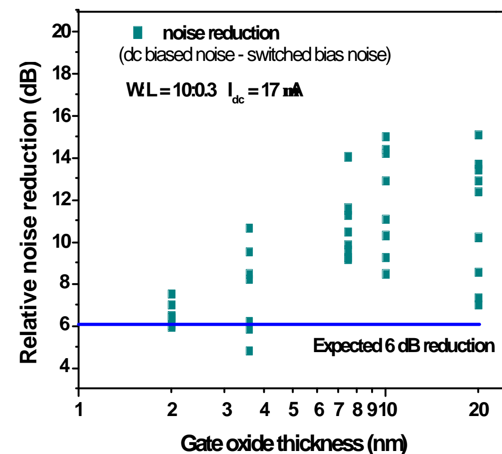

Fig. 7. Noise reduction as a function of gate oxide thickness W:L=10:0.3

Fig. 8 is a plot of the all the measured low-frequency noise values (spread over all the wafers with different t_{ox}) and their corresponding noise reduction. Also shown is the expected 6 dB noise reduction. From Fig. 8 it can be concluded that larger the low-frequency noise in a particular device, larger is the noise reduction observed under switched bias conditions.

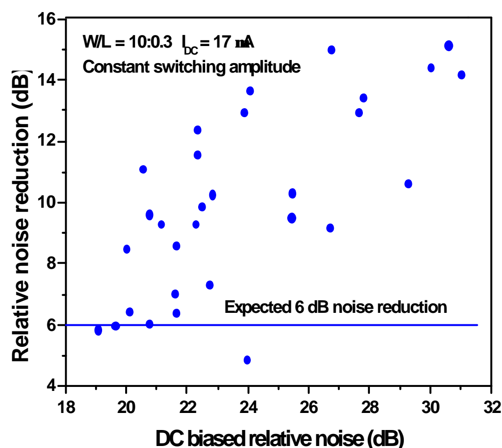

Fig. 8. Noise reduction and low frequency noise for all t_{ox} values

The measurement results can be explained qualitatively as follows. The low frequency or 1/f noise in p-MOSFET can be explained by the mobility fluctuation theory or by the number fluctuation theory. The latter, is based on theory of trapping and detrapping of mobile charge carriers in traps located at the silicon interface and in the oxide. When a transistor is periodically switched "off", there is a high probability that the traps with energies located close to the Fermi level, are emptied. Thus, the average values of capture time constant (τ_c) and emission time constant (τ_e) of the trap are now changed, which in turn leads to a reduced noise spectrum. As the "off" voltage of the switching amplitude is increased, more traps are emptied in the "off" state. Thus, the noise reduction increases with increasing amplitude of the switching gate pulse. The limit to the extent of noise reduction is reached, when all the traps, involved in the trapping-detrapping process, are emptied during the "off" state of the transistor. Increasing the "off" voltage now has no effect on the noise spectrum.

The decrease in the low-frequency noise as a function of decreasing gate oxide thickness, can be explained from the inverse relationship of the low-frequency noise with the oxide capacitance (C_{ox}). However, the dependence of noise reduction on t_{ox} is not yet clear. It is difficult to obtain a trend, for the noise reduction as a function of t_{ox}, for constant switching amplitude, as seen from Fig. 6 and 7.

IV. CONCLUSION

The p-MOSFET noise measurements and switched bias noise measurements do not differ from the n-MOSFET noise measurements[7]. In almost all the cases, the noise reduction was more than 6 dB. The noise reduction increased with increase in switching amplitude of the gate pulse. The gate oxide dependence of the low-frequency noise was verified and was observed to be the same as given in literature[6]. No specific trend in the noise reduction as a function of t_{ox} was observed. Larger the low-frequency noise in a p-MOSFET, larger was the noise reduction under switched bias conditions.

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