

INTERFACE STUDIES OF THE MOS-STRUCTURE BY TRANSFER-ADMITTANCE MEASUREMENTS

JAN KOOMEN

Twente University of Technology, Enschede, The Netherlands

(Received 20 November 1972; in revised form 17 August 1973)

Abstract—The transfer-admittance of *n*- and *p*-channel MOS transistors has been measured under the condition of a uniform channel. These MOS transistors all showed a measurable “slow interface state drift” $< 0.1-0.2$ V. The transfer-susceptance has been found to show a significant peak value in moderate inversion. Over the entire moderate and strong inversion region the transfer-susceptance remains constant as a function of the measurement frequency ω between 1.6 Hz and 2×10^4 Hz, while the transfer-conductance varies almost like $\ln \omega$. Furthermore the transfer-susceptance shows a linear relationship with the variation of the transfer-conductance per frequency decade. The paper shows that these phenomena can be well explained by assuming a tunneling of channel charge carriers into electron states in the oxide. Also the temperature behaviour of the transfer-admittance does not seem to be in conflict with this tunnel model. More than the *CV* measuring method the measurement of the transfer-admittance allows an investigation of the interaction between mobile inversion layer charge carriers, and interface states in the condition of moderate inversion ($5 \times 10^{10}-5 \times 10^{11}$ electrons cm^{-2}). The measuring method might therefore find application in the investigation of charge trapping in CCD devices. As a pertinent result the density of oxide states having time constants between 6×10^{-1} sec and 1.6×10^{-3} sec appears to increase to values of about 10^{11} per cm^2V as the interface state energy approaches the conduction and valence band edges within a distance of ≈ 70 meV.

1. INTRODUCTION

Generally the transfer-conductance of MOS transistors has been found to increase in magnitude with frequency [1, 2]. The larger the frequency, the smaller the number of interface states which are able to follow the small signal variations and relatively more charge carriers in the MOST channel become available to participate in the transfer-conductance. In this paper both transfer-conductance and -susceptance measurements have been performed on a number of *n*- and *p*-channel MOS transistors as a function of gate voltage for frequencies between 1.6 and 10^4 Hz and uniform channel. The aim of these measurements is an investigation into the capture of mobile channel charge by oxide states located close to the Si-SiO₂ boundary.

In the next section we shall first consider the complex small signal MOST-transfer-admittance for small voltage differences between the source and the drain, in the presence of charge capturing oxide states.

The real and imaginary parts of the transfer-admittance will be found to be dependent on the real and imaginary part of an assumed proportionality factor *A* between trapped and mobile channel charge.

In the second part of this section we shall deal

with the actual nature of this factor *A* if trapping occurs by tunneling interaction with states in the oxide.

2. THEORY OF THE INFLUENCE OF INTERFACE STATES ON THE TRANSFER ADMITTANCE

The transfer-admittance of an *n*-channel MOST under the condition of a uniform channel and neglecting capacitive currents may be written like,

$$\left. \frac{dI_d}{dV_g} \right|_{V_b, V_d=0, V_s>0} = q \frac{W}{L} V_s \left(\mu_n \frac{d\Delta n}{dV_g} + \Delta n \frac{d\mu_n}{dV_g} \right) \quad (1)$$

where $dV_g \exp(j\omega t)$ is the small signal gate voltage with a rotational frequency ω ,

- dI_d the small signal source-drain current;
- W/L the MOST aspect ratio;
- V_s the source-substrate reverse bias ($\ll kT/q$); $kT/q = 25.5 \cdot 10^{-3}$ V at 300°K;
- q the electron charge;
- Δn the inversion layer electron excess density (cm^{-2}); $\Delta n(\psi_s = 0) = 0$;
- μ_n the mobility of the electrons in the inversion layer ($\text{cm}^2 \text{V}^{-1} \text{sec}^{-1}$);
- $\left. \begin{matrix} d\Delta n \\ d\mu_n \end{matrix} \right\}$ the small signal variations of the inversion layer electron density and mobility, respectively.

The surface potential ψ_s is defined with respect to the silicon substrate as indicated in the energy diagram of the MOS structure in Fig. 1. Taking ψ_s as the variable, rather than V_g , we obtain:

$$\frac{dI_d}{dV_g} = q \frac{W}{L} V_s \left(\mu_n \frac{d\Delta n}{d\psi_s} + \Delta n \frac{d\mu_n}{d\psi_s} \right) \frac{d\psi_s}{dV_g}. \quad (2)$$

Before we proceed with the development of the small signal transfer-admittance theory the following assumptions will be made:

(a) the surface electron concentration follows the gate signal and is in quasi-thermodynamic equilibrium. This implies that the period of the gate-signal should be much larger than the distributed channel RC time constant and moreover that the source-drain voltage V_s is much less than kT/q . Consequently the ratio $d\Delta n/d\psi_s$ may be considered to be real.

(b) The electron mobility variation follows the gate signal as well, and $d\mu_n/d\psi_s$ is real.

Now the transfer-conductance and -susceptance can, respectively, be written as:

$$\text{Re} \frac{dI_d}{dV_g} = q \frac{W}{L} V_s \left(\mu_n \frac{d\Delta n}{d\psi_s} + \Delta n \frac{d\mu_n}{d\psi_s} \right) \text{Re} \frac{d\psi_s}{dV_g} \quad (3)$$

$$\text{Im} \frac{dI_d}{dV_g} = q \frac{W}{L} V_s \left(\mu_n \frac{d\Delta n}{d\psi_s} + \Delta n \frac{d\mu_n}{d\psi_s} \right) \text{Im} \frac{d\psi_s}{dV_g}. \quad (4)$$

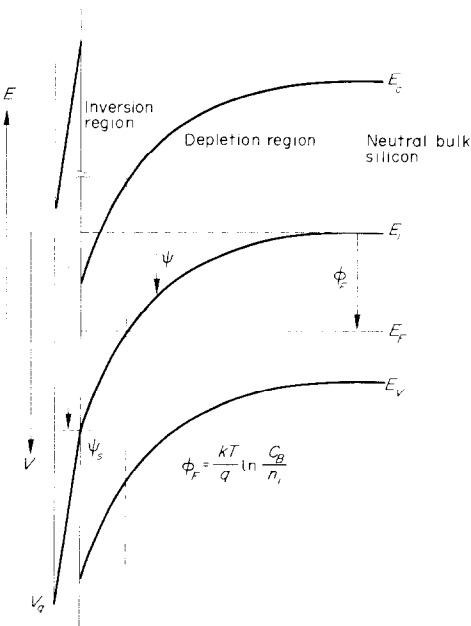


Fig. 1. Energy and potential diagram of the MOS system. The bulk fermi-potential is denoted by ϕ_F . C_B is the bulk dope density and n_i the intrinsic silicon electron concentration.

Equations (2), (3) and (4) express that the transfer-admittance is proportional to the ratio $d\psi_s/dV_g$. This ratio can be solved from the small signal MOST charge neutrality equation. The complex behaviour of $d\psi_s/dV_g$ arises from the interaction of inversion layer electrons with energy states in the silicon-dioxide.

We shall continue with the presentation of a tunneling model[19] that describes the capture of inversion layer electrons by so called slow states in the oxide. Here after we form the small signal MOS charge neutrality equation. First of all we shall start with a description of the spatial and energy distribution of the electron states in the MOS system.

The oxide states, responsible for electron capture are assumed to be located in the silicon dioxide within a thin layer of thickness z_0 , adjacent to the Si-SiO₂ interface. We estimate that z_0 has actually a value between 20 and 50 Å. The oxide state concentration N'_{T0} per cm³ eV is supposed to be continuously distributed over the location depth $-z$ and the electron energy E . Furthermore fast states are assumed also to be present at the Si-SiO₂ interface and even as the oxide states continuously distributed over the electron energy E , as has been visualized in Fig. 2.

In the inversion condition of the silicon surface, the interaction of the interface and oxide states with the inversion layer electrons dominates [12, 18] over the corresponding interaction with the holes in the valence band. Hence we may confine ourselves to the electron capture of the interface and oxide states.

Fu and Sah[19] proposed an electron transition from the conduction band to an oxide state to occur by the following steps:

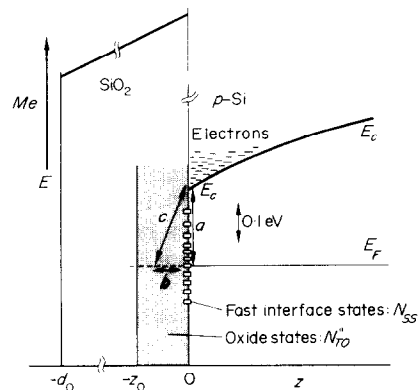


Fig. 2. Spatial and energy distribution of oxide- and interface states in the MOS system. The p -type silicon is in the inverted condition.

(a) a transition from the conduction band to a fast interface state (transition a in Fig. 2) and; (b) subsequently, an elastic tunneling transition from the interface state to oxide states (transition b in Fig. 2).

Provided that the transition time constant of the electrons from the conduction band to the fast interface states and *vice versa* is assumed to be much smaller than the period of the measurement signal and moreover if the small signal charge variations in the oxide states are considered as to occur at the interface, the MOST small signal charge neutrality equation may be expressed like:

$$C_0(dV_g - d\psi_s) = \{C_D + C_{inv} + C_{ss}\} d\psi_s + q dn_{TO} \quad (5)$$

where

- C_{inv} the inversion layer capacitance; $q d\Delta n/d\psi_s$ ($F\text{ cm}^{-2}$);
- C_D the silicon depletion layer capacitance; $q d\Delta p/d\psi_s$ ($F\text{ cm}^{-2}$);
- $\left. \begin{array}{l} \Delta n \\ \Delta p \end{array} \right\}$ the excess electron and hole densities in the silicon and $d\Delta n$ and $d\Delta p$, respectively their small signal variables; $\Delta p(\psi_s = 0) = 0$;
- n_{ss} the electron density trapped in interface states;
- dn_{ss} the small signal interface state electron occupation per cm^2 ;
- C_{ss} the interface state capacitance; $q dn_{ss}/d\psi_s$ ($F\text{ cm}^{-2}$);
- dn_{TO} the small signal oxide state electron occupation per cm^2 .

Now the total small signal charge density trapped in oxide states and the inversion layer charge density are related by a complex variable A :

$$q dn_{TO} = Aq d\Delta n = AC_{inv} d\psi_s \quad (6)$$

Further on this relationship shall be considered in more detail. The substitution of (6) into the charge neutrality equation yields:

$$C_0(dV_g - d\psi_s) = \{C_D + C_{ss} + (1 + A)C_{inv}\} d\psi_s \quad (7)$$

The following variables will be introduced;

(a) the argument of the transfer-admittance, defined as:

$$\arg \frac{dI_d}{dV_g} = \arctan \frac{\text{Im}(dI_d/dV_g)}{\text{Re}(dI_d/dV_g)} \quad (8)$$

(b) the normalized transfer-conductance, defined as:

$$\text{Re}_n \frac{dI_d}{dV_g} = \frac{\text{Re}(dI_d/dV_g)}{\text{Re}(dI_d/dV_g)_{\max}}, \quad (9)$$

where $\text{Re}(dI_d/dV_g)_{\max}$ is given by:

$$\text{Re} \frac{dI_d}{dV_g} \Big|_{\max} = \frac{C_0}{C_0 + C_D + C_{inv} + C_{ss}} \quad (10)$$

The combination of equations (3), (4) and (7) leads to the following results for $\arg(dI_d/dV_g)$ and $\text{Re}_n(dI_d/dV_g)$:

$$\arg \frac{dI_d}{dV_g} = \frac{\omega^{-1} G_{TO}}{C_0 + C_D + C_{ss} + C_{TO} + C_{inv}} \quad (11)$$

and

$$1 - \text{Re}_n \frac{dI_d}{dV_g} = \frac{C_{TO}}{C_0 + C_D + C_{ss} + C_{TO} + C_{inv}} \quad (12)$$

where $C_{TO} = \text{Re}(A)C_{inv} = \text{Re} dq n_{TO}/d\psi_s$, the oxide state capacitance and $G_{TO} = -\omega \text{Im}(A)C_{inv} = -\omega \text{Im} dq n_{TO}/d\psi_s$, the oxide state conductance.

In the derivation of equations (10) and (11) $\omega^{-1} G_{TO}$ has been assumed to be small with respect to $C_0 + C_D + C_{ss} + C_{TO} + C_{inv}$. Subsequently the term $C_0 + C_D + C_{ss} + C_{TO} + C_{inv}$ can be related to the measured total gate capacitance C by the following expression:

$$\frac{C_0 - C}{C_0^2} \approx \frac{1}{C_0 + C_D + C_{ss} + C_{TO} + C_{inv}} = \frac{1}{C_m} \quad (13)$$

For weak inversion, $1/C_m$ can be obtained from a measurement of $(C_0 - C)/C_0^2$, for strong inversion $1/C_m$ reduces to $1/C_{inv}$.

The substitution of expression (13) into (11) and (12) yields:

$$\arg \frac{dI_d}{dV_g} = \frac{G_{TO}}{\omega C_m} \quad (14)$$

and

$$1 - \text{Re}_n \frac{dI_d}{dV_g} = \frac{C_{TO}}{C_m} \quad (15)$$

Now we shall derive the oxide state capacitance C_{TO} and conductance G_{TO} as a function of the frequency ω .

Because the interface states are supposed to be "fast" with respect to the measurement frequency ω , the frequency behaviour of the transfer-admittance for low frequencies will mainly be determined by the elastic tunnel transitions between the fast interface states and the oxide states (transition b in Fig. 2).

The rate of electron trapping at energy E and location $-z$ is described by the equation:

$$\frac{\partial}{\partial t} \{n''_{\tau_0}\} = T[n'_{ss}(N''_{\tau_0} - n''_{\tau_0}) - (N'_{ss} - n'_{ss})n''_{\tau_0}], \quad (16)$$

where T is the probability for an electron to tunnel from the fast interface states towards the oxide states and *vice versa*;

- n''_{τ_0} the oxide state electron occupation at energy E and depth $-z$ ($\text{cm}^{-3}\text{e}^{-1}\text{V}^{-1}$);
- dn''_{τ_0} its small signal variable;
- N'_{ss} the interface state density per cm^2eV ;
- n'_{ss} the electron density trapped in interface states per cm^2eV ;
- dn'_{ss} its small signal variable.

The tunneling probability T is proportional to $\exp \alpha z$, where the decay constant α depends mainly on the height of the energy barrier between the conduction bands of the oxide and the silicon[4]. A typical value for $\alpha = 1 \text{ \AA}^{-1}$.

We now rewrite equation (16) in a simpler form:

$$\frac{\partial}{\partial t} \{n''_{\tau_0}\} = T[n'_{ss}N''_{\tau_0} - N'_{ss}n''_{\tau_0}]. \quad (17)$$

The product $(TN'_{ss})^{-1}$ in equation (17) is the electron capture time constant τ of the oxide states, and hence increases exponentially by $\exp(-\alpha z)$ with the penetration depth z : $\tau = \tau_0 \exp -\alpha z$, where τ_0 is the capture time constant of the oxide states located just at the Si-SiO₂ boundary. The maximum capture time constant is $\tau_0 \exp \alpha z_0$ (for $z = -z_0$).

The small signal representation of equation (17) is given by:

$$dn''_{\tau_0} = \frac{N''_{\tau_0}}{N'_{ss}(1 + j\omega\tau)} dn'_{ss}. \quad (18)$$

Hereby it is assumed that N'_{ss} and N''_{τ_0} do not vary too much over an energy interval $2kT$ and N''_{τ_0} over a distance $(2\alpha)^{-1}$ as well. The total small signal electron capture dn''_{τ_0} can be found from a double integration over the energy and the location depth $-z$ of equation (18):

$$dn''_{\tau_0} = \int_{-z_0}^0 \int_{-\infty}^{+\infty} dn''_{\tau_0}(E, z) dE dz. \quad (19)$$

Execution of the integration yields:

$$\omega^{-1}G_{\tau_0} = \frac{q^2 N''_{\tau_0}}{\alpha} [\arctan(\omega\tau_0 \exp \alpha z_0) - \arctan \omega\tau_0] \quad (20)$$

and

$$C_{\tau_0} = \frac{q^2 N''_{\tau_0}}{2\alpha} [\ln(1 + \omega^2 \tau_0^2) - 2 \ln \omega\tau_0 - \ln(1 + \omega^{-2} \tau_0^{-2} \exp - 2\alpha z_0)]. \quad (21)$$

For the conditions $\omega\tau_0 \exp 2\alpha z_0 \gg 1$ and $\omega\tau_0 \ll 1$ equations (20) and (21) reduce to:

$$\omega^{-1}G_{\tau_0} = \frac{q^2 N''_{\tau_0}}{\alpha} \frac{\pi}{2} \quad (22)$$

and

$$C_{\tau_0} = \frac{q^2 N''_{\tau_0}}{\alpha} \ln \omega\tau_0. \quad (23)$$

The substitution of $\omega^{-1}G_{\tau_0}$ and C_{τ_0} into equations (14) and (15) yields the frequency dependence of the variables $\arg(dI_d/dV_g)$ and $1 - \text{Re}_n(dI_d/dV_g)$:

$$\arg \frac{dI_d}{dV_g} = \frac{1}{C_m} \frac{\pi q N'_{\tau_0}}{2\alpha} \quad (24)$$

and

$$1 - \text{Re}_n \frac{dI_d}{dV_g} = -\frac{1}{C_m} \frac{q N'_{\tau_0}}{\alpha} \ln \omega\tau_0, \quad (25)$$

where $N'_{\tau_0} = qN''_{\tau_0}$, the oxide state concentration per V cm^3 .

The relative variation per frequency decade of the transfer-conductance for $\omega\tau_0 \ll 1$ is given by:

$$\Delta_\omega \text{Re}_n \frac{dI_d}{dV_g} = \frac{1}{C_m} \frac{2 \cdot 3 q N'_{\tau_0}}{\alpha}. \quad (26)$$

From equations (24) and (26) it may be concluded that at low frequencies $\arg(dI_d/dV_g)$ and $\Delta_\omega(dI_d/dV_g)$ are linearly related with a proportionality factor $4 \cdot 6/\pi$. Furthermore, both parameters are a measure for the oxide state concentration N'_{τ_0} .

There are indications[7-10] that the mobility is dependent on the amount of charge in the oxide and on the gate voltage. This chapter shows, irrespective of the unknown mobility behaviour, the feasibility of an investigation into the capture of mobile electrons by means of transfer-admittance measurements.

In the next section we shall proceed with a presentation of the transfer-admittance measurements followed by an analysis on the basis of the theory described in this section.

3. MEASUREMENTS

MOST transfer-admittance measurements have been performed on various types of n -channel as

well as *p*-channel MOS transistors. The transistors all had a 500 Å phosphosilicate glass film on top of the gate oxide, thermally grown at 1200°C. A wet nitrogen heat treatment at 500°C was given before the deposition of the Al gate metal. The scheme of the measurement principle is shown in Fig. 3. As current detectors both the bridges Wayne-Kerr B221 and General Radio A1615 have been used. The PAR HR-8 lock-in amplifier has always been applied as a bridge detector. For frequencies smaller than 20 Hz, the use of the PAR HR-8 alone was sufficient. The gate drain resistor served to avoid large real transfer currents ($\text{Re } dI_d$) in the bridge. In Fig. 4 the measured transfer-capacitance $\omega^{-1} \text{Im}(dI_d/dV_g)$ of a typical *n*-channel MOST is shown as a function of V_g for different frequencies. The transfer-capacitance in Fig. 4, which is either positive or negative depending on the polarity of V_s , is superimposed on the gate-drain capacitance C_d , which would also be present when $V_s = 0$. A plot of the simultaneously measured transfer-conductance $\text{Re}(dI_d/dV_g)$ has been given in Fig. 5 vs gate voltage and for one frequency.

Figure 6 represents the behaviour of the transfer-conductance as a function of the measurement frequency of the same *n*-channel MOS transistor. The measurement points are plotted vs time in order to eliminate the drift. The straight lines represent the different measurement frequencies. In this case the gate voltage was kept at a value of 1.8 V. Essentially the same frequency dependence of $\text{Re}(dI_d/dV_g)$ was obtained at other gate voltages.

The MOS transistors all showed a measurable drift of the source-drain current vs time, like the drift due to the presence of so called "slow oxide states" [14]. The tendency "the larger this drift, the larger $\arg dI_d/dV_g$ and $\Delta_\omega \text{Re}_n dI_d/dV_g$ " has been observed.

The slope of the lines connecting the measurement points in Fig. 6 is a measure of the drift, just mentioned before. We always found identical and reproducible vertical distances between the straight

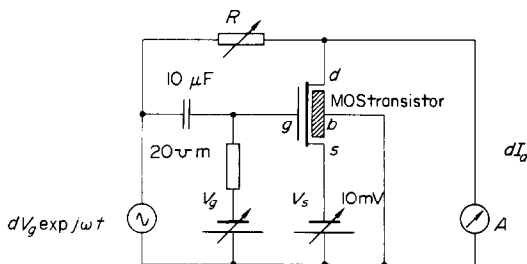


Fig. 3. Schematic diagram of the measurement principle.

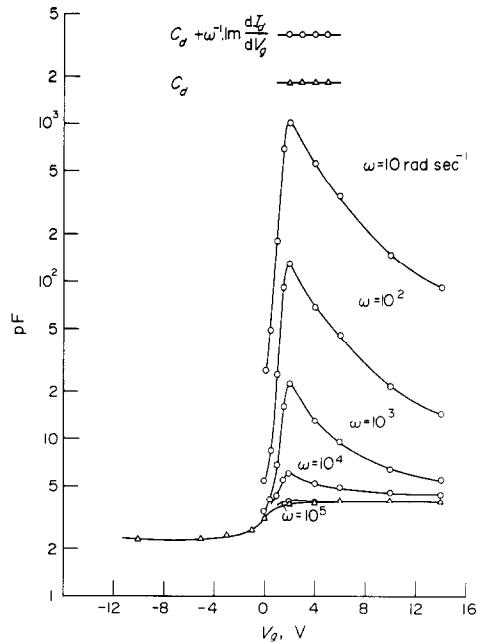


Fig. 4. Transfer-capacitance of an *n*-channel 1-1-1 oriented MOS-transistor. The bottom curve represents the gate-drain capacitance. The thickness of the gate oxide including the phosphosilicate glass layer is 2180 Å; aspect ratio (W/L): 85; channel-length L : 16 μm; mobility: $600 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ and bulk dope density $3 \times 10^{15} \text{ cm}^{-3}$.

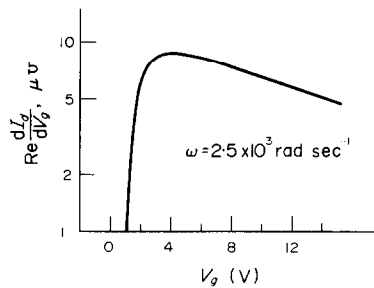


Fig. 5. Transfer-conductance vs the gate voltage of the MOS transistor in Fig. 4.

lines in Fig. 6, independent of the momentary drift or the slope of these lines.

4. INTERPRETATION OF THE MEASUREMENTS

In the previous section, transfer-admittance measurements on only one type of *n*-channel MOS transistor have been shown in detail, because measurements on similar 1-1-1 oriented *n*- as well as 1-1-1 oriented *p*-channel MOS transistors led essentially to the same results.

First we shall try to explain the variation vs gate voltage of the transfer-capacitance curves in Fig. 4.

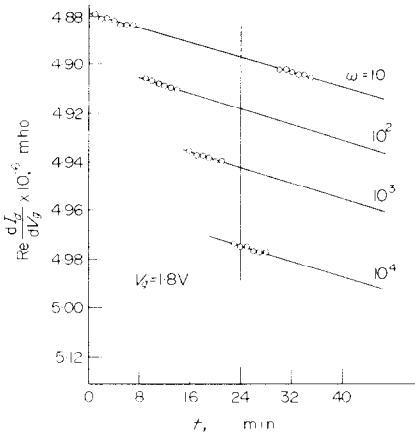


Fig. 6. The behaviour of the transfer-conductance as a function of the frequency. The measurement points are plotted vs time in order to eliminate the drift of the MOS transistor. (The same *n*-channel MOST as in Fig. 4 has been used.)

If the ratio $d\mu_n/d\psi_s$ is neglected in the right hand side of equation (4), then following a combination of equations (4), (6) and (7) $\text{Im } dI_d/dV_g$ turns out to be:

$$\text{Im } \frac{dI_d}{dV_g} = q \frac{W}{L} V_g \mu_n \frac{C_0 C_{\text{inv}} \omega^{-1} G_{T0}}{\{C_0 + C_D + C_{\text{ss}} + C_{T0} + C_{\text{inv}}\}^2} \quad (27)$$

Aside from the behaviour of G_{T0} the transfer-susceptance should have a maximum value at $C_{\text{inv}} = C_0 + C_D + C_{\text{ss}} + C_{T0}$, and decrease to zero towards weak as well as strong inversion. The gate voltage pertaining to $C_{\text{inv}} = C_0 + C_D + C_{\text{ss}} + C_{T0}$ was calculated to be ≈ 2 V. Actually we found the maximum value of $\text{Im}(dI_d/dV_g)$ also to occur at $V_g = 2$ V.

The frequency dependence of the transfer-capacitance and -conductance can be explained by the aid of the tunneling model, described in section 2, as will be shown in the following.

From Figs. 4 and 6 the variables $\arg(dI_d/dV_g)$ and $1 - \text{Re}_n(dI_d/dV_g)$ have been graphically determined as a function of ω . Figures 7 and 8 show a plot of these variables vs ω for $V_g = 1.8$ V.

At first glance $\arg(dI_d/dV_g)$ appears to be independent of ω over the measured frequency within a factor 2, while $1 - \text{Re}_n(dI_d/dV_g)$ varies almost like $-\ln \omega$.

For a homogeneous oxide state concentration we would, according to equations (24) and (25), expect a horizontal straight line in Fig. 7 and also a straight

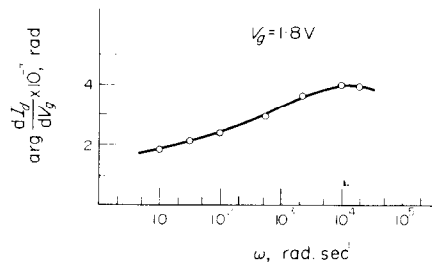


Fig. 7. $\arg(dI_d/dV_g)$ vs ω for the *n*-channel MOS transistor in Fig. 4 ($V_g = 1.8$ V).

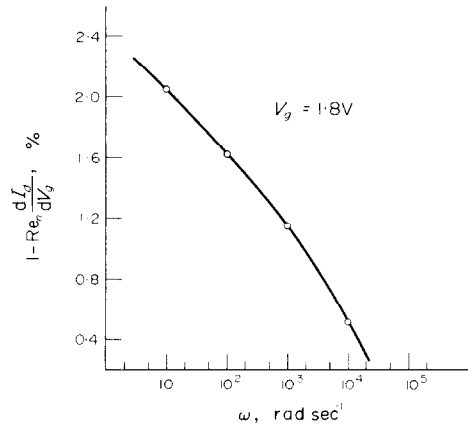


Fig. 8. $1 - \text{Re}_n(dI_d/dV_g)$ for the same *n*-channel MOS transistor in Fig. 4 ($V_g = 1.8$ V). The transfer-conductance has been normalized with respect to $\text{Re}(dI_d/dV_g)_{\text{max}} = 5 \times 10^{-6} \text{ U}$.

line $-\ln \omega$ in Fig. 8. The deviations are supposed to be due to a slight variation in N'_{T0} vs the location depth $-z$ or which is equivalent, vs frequency[4]. The variable $\alpha^{-1} N'_{T0}$ has been determined vs frequency from Figs. 7 and 8 by means of equations (24) and (26), as illustrated by Fig. 9 by the solid and broken lines, respectively. The capacitance C_{inv} occurring in equations (24) and (26) has been obtained from the relation $C_{\text{inv}} = r(q/kT)q\Delta n$. The constant r is a known function of ψ_s and lies in between 1 for weak and $\frac{1}{2}$ for strong inversion. The excess electron density Δn has been derived from the source-drain conductance $\mu(W/L)q\Delta n$. The agreement between the curves in Fig. 9 is striking, their small difference to one another might be due to experimental error.

Two conclusions can be inferred from Fig. 9:

- (1) the transfer-susceptance is proportional with the variation of the transfer-conductance per frequency decade;
- (2) the interface state concentration N'_{T0} is more or less constant in the measured frequency range.

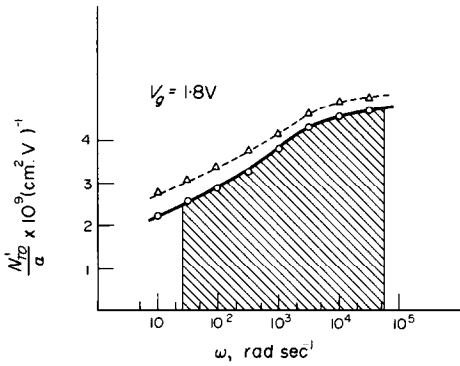


Fig. 9. The variable $\alpha^{-1}N_{T0}$ as a function of ω . The solid line represents $\alpha^{-1}N_{T0}$ as determined from $\arg(dI_d/dV_g)$, whereas the broken line represents $\alpha^{-1}N_{T0}$ as determined from the slope of $1 - \text{Re}_n(dI_d/dV_g)$.

The oxide state density having time constants between τ_1 and τ_2 $N_{T0}(\tau_1; \tau_2)$ are contained within an oxide layer of thickness $z_1 - z_2 = \alpha^{-1} \ln(\tau_1/\tau_2)$, because of the relation $\tau = 2\pi\omega^{-1} = \tau_0 \exp(-\alpha z)$. This means that $N_{T0}(\tau_1; \tau_2)$ may be determined from an integration of $\alpha^{-1}N_{T0}$ over $\ln \omega$, as shown by the shaded area in Fig. 9:

$$N_{T0}(\tau_1; \tau_2) = \int_{\ln\omega_1}^{\ln\omega_2} \alpha^{-1} N_{T0} d \ln \omega. \quad (28)$$

Figure 10 shows $N_{T0}(\tau_1; \tau_2)$ as a function of the gate voltage for τ_1 and τ_2 being 3×10^{-2} sec and 1.6×10^{-5} sec, respectively, (broken line).

Also the fast interface state density N_{ss} and the oxide state density with time constants smaller than 3×10^{-2} sec, $N_{T0}(3.2 \times 10^{-2}; \tau_0)$ has been deter-

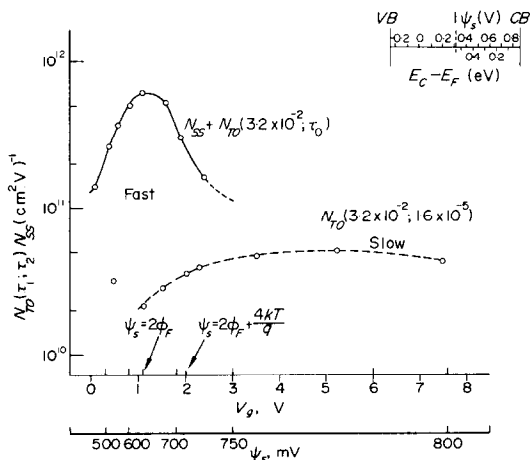


Fig. 10. Interface state and oxide state densities as a function of ψ_s and V_g . The scales at the upper right hand corner relates the position of the Fermi energy level with the various surface potentials.

mined from the low frequency CV curve (4.6 Hz) [11], and from a split CV measurement [17]. The curve $N_{ss} + N_{T0}(3.2 \times 10^{-2}; \tau_0)$ thus obtained has been depicted in Fig. 10 (solid line). Figure 10 shows that a large fast interface state density is present in the weak and moderate inversion regions. Towards strong inversion the slow oxide states tend to constitute a larger part of the total amount of electron (oxide and interface) states. The value of the minimum oxide state capture time constant τ_0 could not be obtained from the measurements, however from the frequency behaviour of the transfer-admittance we expect τ_0 to be smaller than 1.6×10^{-5} sec for all the gate voltages that have been considered.

5. DISCUSSION

A transfer-admittance measurement method, resembling to our method, with the intention of investigating the trapping and mobility of mobile charge carriers, however applied to CdS thin film transistors, has been used already by Haering *et al.* [3].

For the explanation of the low frequency MOST transfer-admittance measurements (between 1.6 and $2 \cdot 10^4$ Hz) a model describing the interaction between interface states and inversion layer including a large range of interaction time constants was necessary. Such a model is the tunneling model of Fu and Sah [19], that they have used for the explanation of noise experiments. It should therefore be meaningful to compare transfer-admittance measurements with the so-called low frequency noise [15, 19] occurring in a MOS transistor.

The tunnel probability T has been shown by Kane [20] to be the largest for so called "elastic" tunnel transitions (transition b in Fig. 2) and decreases rapidly if the states between which the tunneling occurs have an energy difference (inelastic tunneling; transition c in Fig. 2). We now consider the weak and moderate inversion condition, where $E_C - E_F \approx 200$ meV (see Fig. 10). The interaction between the conduction band and oxide states right opposite to interface states will probably occur by elastic tunneling as proposed by Fu and Sah [19]. The interaction between the conduction band and oxide states not located close and opposite to interface states will occur rather by direct inelastic tunnel transitions (described by Heimans [4] tunnel model). For strong inversion, where $E_C - E_F$ reduces to a few units of kT (see Fig. 10) the interaction between the oxide states and the conduction band may occur mainly by direct inelastic tunnel transitions. In the latter case a similar low frequency behaviour of the transfer-admittance

can be derived as in the case of the tunneling model of Fu and Sah (section 2). So in conclusion we believe that both the Heiman and Fu and Sah models may be applicable. Another model which could come into consideration for the explanation of our measurements is the statistical model of Goetzberger *et al.*[12]. In this model fluctuations in the oxide charge influence opposite fluctuations in the silicon charge and hence cause fluctuations in the silicon surface potential and the interface state electron capture time constant τ_{ss} [6, 12]. The variances of the oxide charge fluctuations, found in the literature are of the order 0.1×10^{-8} – 0.4×10^{-8} Ccm⁻²[12, 21]. Now these fluctuations hardly affect ψ_s and τ_{ss} in moderate and strong inversion, because of the large value of C_{ox} . According to the model of Goetzberger $\arg dI_d/dV_g$ should be frequency independent at frequencies corresponding to $\approx \tau_{ss}^{-1}$. Because τ_{ss} is small (10^{-7} sec) in moderate and strong inversion [6, 12], and also its fluctuations are small, $\arg dI_d/dV_g$ should following the statistical model of Goetzberger be frequency independent at large frequencies (10^6 – 10^7 Hz) rather than in the low frequency range (1.6– 10^4 Hz) of our measurements. For this reason we believe that the tunneling models [4, 19] are in our case more plausible than the statistical model of Goetzberger.

Polarization effects in the oxide and phosphosilicate layer interface [16] may also be discarded as a source for time constants. This can be concluded from the fact that both the transfer-conductance and -susceptance measurements, as represented in Fig. 9, lead to equal values of the interface state variable N_{ro}/α .

We have done an exploring measurement of the transfer-capacitance ($\omega^{-1} \text{Im } dI_d/dV_g$) vs V_g at two other temperatures: 263° and 323°K. The frequency behaviour of these curves at 263° and 323°K was found to be similar to the room temperature (293°K) curve of Fig. 4. Also quantitatively the transfer-capacitance curves at 263° and 323°K appeared to be consistent with the oxide state density N_{ro} (3×10^{-2} ; 1.6×10^{-5}) as derived from the room temperature measurements, thus providing additional support for the validity of the tunnel models of Heiman [4] and Fu and Sah [19].

6. CONCLUSION

The transfer-admittance measurements (for $V_s \approx 0$) on MOS transistors with a small measurable drift provided verification of a tunneling interaction mechanism between oxide states and inversion layer carriers in the lower frequency range between 1.6 and $2 \cdot 10^4$ Hz. Both the tunneling mod-

els of Heiman [4] and of Fu and Sah [19] could be applied for an explanation of the frequency behaviour of the transfer-admittance. For weak and moderate inversion we believe that Fu and Sah's tunneling model is more plausible, in strong inversion also direct inelastic tunneling interactions between oxide states and the inversion layer electrons may occur. (We did not look into the possibility of indirect tunneling transitions between interface and oxide states). Furthermore transfer-admittance measurements lead to an adequate impression of the "quality" of the MOS transistor fabrication process, because interface state densities downwards to 10^{10} per cm²V can be detected well from moderate towards strong inversion. The latter is of value for people, interested in the charge-loss mechanism in CCD's.

Acknowledgements—It is a great pleasure to thank H. de Haas and H. Alink, who carefully performed many of the transfer-admittance measurements, O. W. Memelink for his guidance, Mrs. J. Koomen-Wortelboer for typing the manuscript, and E. Holl who drew the figures.

REFERENCES

1. F. Fang and G. Triebwasser, *IBM J.* **8**, 410 (1964).
2. F. Fang and A. B. Fowler, *Phys. Rev.* **169**, 619 (1968).
3. M. G. Miksic, E. S. Schlig and R. R. Hearing, *Solid-St. Electron.* **7**, 39 (1964).
4. F. P. Heiman and G. Warfield, *IEEE Trans. Electron. Devices* **EC-12**, 167 (1965).
5. H. Preier, *Appl. Phys. Letts.* **10**, 361 (1967).
6. K. Lehovc and A. Slobodskoy, *Solid-St. Electron.* **7**, 59 (1964).
7. O. Leistikko Jr., A. S. Grove and C. T. Sah, *IEEE Trans. Electron. Devices* **EC-12**, 248 (1965).
8. E. Arnold and G. Abowitz, *Appl. Phys. Letts.* **9**, 344 (1966).
9. R. E. Oakley and M. Pepper, *Phys. Letts.* **4A**, 87 (1972).
10. C. T. Sah, T. H. Ning and L. L. Tschopp, *Surface Sci.* **32**, 561 (1972).
11. C. N. Berglund, *IEEE Trans. Electron. Devices*, **ED-13**, 701 (1966).
12. E. H. Nicollian and A. Goetzberger, *Bell Syst. Tech. J.* **46**, 1035 (1967).
13. K. H. Zaininger and G. Warfield, *IEEE Trans. Electron. Devices* **EC-12**, 179 (1965).
14. I. Lundström, S. Christensson and C. Svensson, *Phys. Status Solids (a)* **1**, 395 (1970).
15. E. H. Nicollian and H. Melchior, *Bell Syst. Tech. J.* **46**, 2019 (1967).
16. E. H. Snow and B. E. Deal, *J. Electrochem. Soc.* **113**, 263 (1966).
17. J. Koomen, *Solid-St. Electron.* **16**, 801 (1973).
18. W. Shockley and W. T. Read, *Phys. Rev.* **87**, 835 (1952).
19. H. S. Fu and C. T. Sah, *IEEE Trans. Electron. Devices* **ED-19**, 273 (1972).
20. E. Burstein and S. Lundqvist, *Tunneling Phenomena in Solids*, Plenum, New York (1969).
21. G. Declerck, Ph.D. Thesis, Louvain, Belgium (1972).