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NARROW CHANNEL Si-MOSFETs FOR ELECTRON TRANSPORT STUDIES

J.R. Gao*, J. Caro*, A.H. Verbruggen*, S. Radelaar* and J. Middelhoek**

* Centre for Submicrontechnology and Delft Institute for Microelectronics and Submicron-technology, Delft University of Technology, Delft, The Netherlands
** Vakgroep IC-technology and Electronics, Twente University, Enschede, The Netherlands

We have fabricated narrow channel Si-MOSFETs for electron transport studies at low temperature. The fabrication process combines optical lithography for large structures and high resolution e-beam lithography for narrow gates. The smallest working devices have a 0.14 µm wide gate. This paper reports the fabrication process and gives some examples of the quantum transport phenomena observed in these devices.

1. INTRODUCTION

Recently new quantum interference phenomena in the low temperature electrical transport of structures with one or more dimensions in the submicron regime have been discovered [1]. Among the phenomena studied so far are weak localization, the Aharonov-Bohm effect and universal conductance fluctuations. The relevant length scale for these effects is the inelastic mean free path L_{in}, along which electron waves retain their phase coherence. At liquid helium temperature or lower in metallic or semiconducting structures L_{in} is usually in the submicron range. Therefore, electron beam lithography has become the most important technique for the fabrication of samples with one or more dimensions comparable to L_{in}. For the fabrication of narrow channel MOSFETs for the study of quantum transport at reduced dimensionality, we developed a fabrication process that combines 'standard' MOS-processing and e-beam lithography. Care was taken to avoid mobility degrading steps in the process in order to obtain a long L_{in}.

2. FABRICATION PROCESS

On the basis of a MOSFET process running in the Twente IC-laboratory we defined a simple n-channel metal gate process for a high helium temperature mobility. The large structures of the devices (source, drain etc.) are defined by optical lithography, while the narrow gates and their contact pads are patterned by electron beam lithography. In the very beginning of the process alignment markers for the electron beam pattern generator are etched anisotropically along the crystal planes of the <100> substrates [2]. The second mask is aligned to the e-beam markers and defines the optical markers. Then source and drain regions are formed by the implantation of phosphorus. A channel implantation to adjust the threshold voltage is not applied, since it will degrade the mobility. Thereafter, in the channel region the oxide is removed and a high quality 25 nm thick gate oxide is grown. In this stage the gate pattern is written in positive e-beam resist and NiCr gates are produced by evaporation and lift-off (details are discussed in section 3). In a similar e-beam fabrication step NiCr intermediate contact pads to the narrow gates are formed. The CVD-oxide deposited next protects the narrow lines during the damage annealing and enables the simultaneous contact hole etching to the NiCr pads and to the source and drain areas. Then a heat treatment removes the damage due to e-beam writing. Finally the aluminium metallization is deposited and patterned, followed by a post metallization annealing. The substrates used are 2" p-type silicon wafers with a resistivity of 15-20 Ωcm. We fabricated several types of devices with different W/L (gate width/gate length) ratios, the smallest gate width realized being 90 nm. Fig. 1 shows a narrow channel MOSFET fabricated according to the process described above.

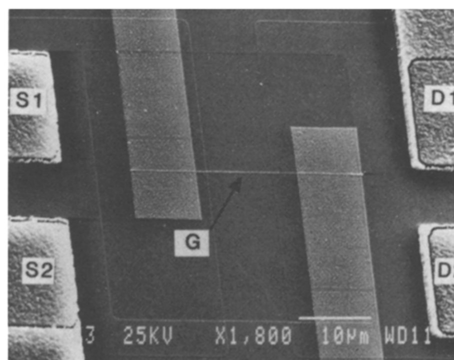

Fig. 1. SEM-micrograph of narrow channel MOSFET. The gate width is 0.16 µm.

The figure shows the source and drain regions, each with two aluminium contacts to allow for four terminal measurements, and in the centre the rectangular area of the gate oxide with the narrow gate and contact pads. The drain characteristics at 4.2 K of one of our devices, with

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channel width 0.16 μm, are given in fig. 2. The family of curves shown in the figure characterizes a properly operating device, as for instance reflected by a quadratic dependence of the saturation current on the gate voltage above threshold. Typically the threshold voltage at 4.2 K is about 1.5 V, the maximum deviation from this value among the devices being 0.5 V. The maximum mobility of our narrowest devices amounts to 8000 $cm^2/Vsec$.

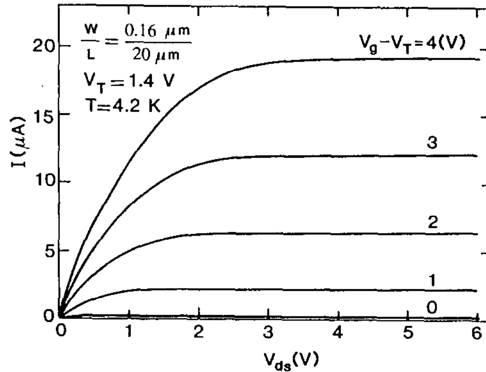

Fig. 2. Drain characteristics of a MOSFET with a 0.16 μm wide gate. The curves are labeled according to their gate voltage (in Volts) above threshold.

3. LITHOGRAPHY OF NARROW GATES

The narrow gates were made out of NiCr. Long, narrow lines between source and drain were defined by electron beam lithography using an upgraded Philips EBPG/03 operating at 50 keV. As resist we used a double layer of PMMA resists with different molecular weight. The bottom layer was 65 nm thick (molecular weight 180 K) and was baked at 180 °C for 1 h. The top layer was 130 nm thick (molecular weight 300 K) and dissolved in xylene in order to prevent intermixing of the two PMMA's. After spin coating of the upper layer, the double layer was baked at 180° C for 15 h. After exposure and development this double layer forms an undercut profile [3]. Development was done in a 1: 3 solution of cellosolve and methanol for 10 seconds at a temperature of 22 °C. Fig. 3 shows a typical undercut profile obtained with our procedure. Although the undercut is not as pronounced as reported by for instance Rooks et al. [4], excellent lift-off was obtained. After development an oxygen plasma was shortly applied to remove residual resist in the developed line. Then 25 nm NiCr was evaporated followed by lift-off in hot acetone (50 °C). NiCr was selected as gate material for its small granularity. In a similar fabrication sequence, using a new double layer, two NiCr contact pads to the gate were formed. These pads are 40 nm thick and extend to the areas outside the device. In fig.4 we show the narrowest NiCr line that was produced in our experiments. The width is about 90 nm. The above procedure for fabrication of narrow gates was implemented in the MOS-process described in section 2. We produced a variety of MOSFETs with a gate width ranging between 0.09 μm and 0.50 μm and gate lengths of 5, 10 and 20 μm. The smallest gate width of the working devices, however, was 0.14 μm. Presumably the failure of smaller devices was caused by the process steps following the lithography of the narrow line.

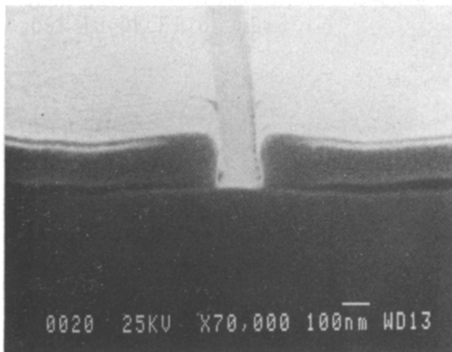

Fig. 3. SEM-micrograph of developed double layer, demonstrating the undercut profile. The bar in the micrograph is 100 nm.

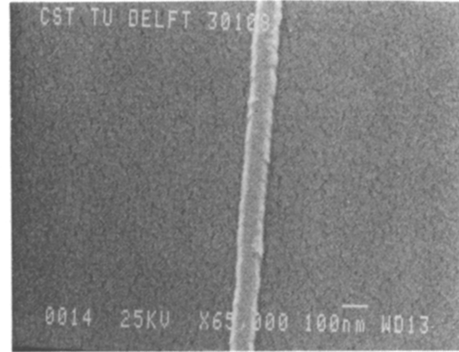

Fig. 4. SEM micrograph of narrow gate line. The bar in the micrograph is 100 nm.

4. QUANTUM TRANSPORT STUDIES

At present experiments are carried out to study the quantum interference phenomena in the electrical transport of the devices described above. More specifically, we study weak localization and the universal conductance fluctuations from the temperature, magnetic field and gate voltage dependence of the conductance of our devices. The conductance was measured by a standard lock-in technique. The excitation voltage across source and drain was small in order to avoid electron heating. Below, we present a few examples of the experiments carried out so far.

4.1. Weak localization

In fig. 5 the turn-on characteristic of a narrow channel device with W/L = 0.14 μm/5μm is shown at 4.2 K and 1.6 K. The conductance at constant gate voltage decreases with decreasing temperature. Also, the 1.6 K curve has reproducible aperiodic oscillations. In order to explain the

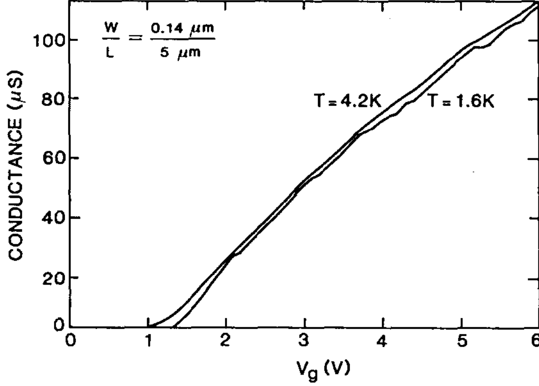

Fig. 5. Turn-on characteristic of narrow channel device at 4.2 K and 1.6 K.

conductance decrease, we considered the correction ΔG_1 to the Boltzmann conductivity due to 1-dimensional weak localization and interaction effects [5]:

$$\Delta G_1 = -\frac{e^2}{\pi \hbar L}\left(L_{in} + \frac{2-F}{\sqrt{2\pi}} L_T\right) \quad (1)$$

Here L_{in} is given by $(D\tau_{in})^{1/2}$, $D = v_f \tau_e / 2$ being the 2-dimensional diffusion constant and τ_{in} and τ_e the inelastic and elastic time, respectively. The parameter $F \approx 1$ is the Hartree term representing the screening and $L_T = (hD/kT)^{1/2}$ is the thermal diffusion length. To establish the validity of eq. (1) for our situation we calculated L_{in} from our magnetoconductance data (section 4.2.) and L_T using $D = G_{\square}/(e^2 N_2)$, N_2 being the 2-dimensional density of states. It was found that at 4.2 K the system is marginally 1-dimensional, while at 1.6 K it is really in this limit. Nevertheless, using eq. (1) to calculate ΔG_1 (4.2 K)– ΔG_1 (1.6 K), we find a value of 2.7 μS. Comparing this with 1.8 μS, the experimental value at 3.6 V (the gate voltage for the magnetoconductance experiments) and taking into account the uncertainties in this calculation (e.g. the value of F and the effect of the oscillations), we conclude that the order of magnitude of the effect is correct. Also, a conductance decrease was not found in less narrow ($W>L_{in}$) devices, confirming that it originates from the 1-dimensional character of the channel. Concerning the oscillations in the 1.6 K curve we mention that from later experiments we already have indications that these are universal conductance fluctuations.

4.2. Magnetoconductance

In order to determine the inelastic length in our samples the magnetoconductance was measured at low fields. As an example in fig. 6 we show the magnetoconductance at 4.1 K and 1.8 K of the same device as characterized in fig. 5. The curves in fig. 6 are a fit of the theoretical 1-

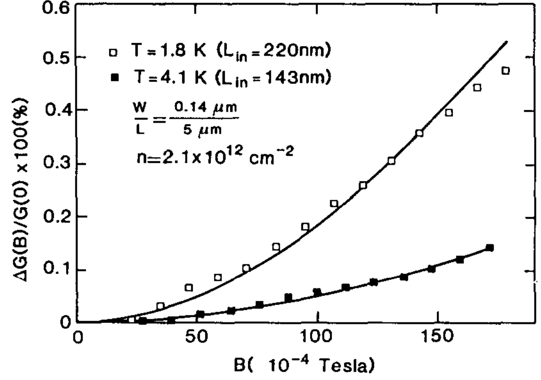

Fig. 6. Magnetoconductance as a function of magnetic field at an electron density of 2.1×10^{12} cm^{-2}. At 4.1 K and 1.8 K G(0) is 65.90 μS and 63.95 μS, respectively.

dimensional expression of Al'tshuler and Aronov [6] to the experimental data. This expression is given by :

$$\Delta G_1 (B) = -\frac{e^2}{\pi \hbar L}\left(\frac{1}{L_{in}^2} + \frac{W^2}{12\, l_B^4}\right)^{-1/2} \quad (2)$$

where $l_B = (\hbar/2eB)^{1/2}$ is the magnetic length. In eq. (2) only L_{in} was used as a fitting parameter. For W we used the gate width. As seen from the figure the fitted curves describe the experimental data very well. From the fits we derived L_{in} (4.1 K) = 0.14 μm and L_{in} (1.8 K) = 0.22 μm. So the MOSFET is 1-dimensional with respect to weak localization, although marginally at 4.1 K.

4.3. Universal conductance fluctuations

Recently, experimental and theoretical investigations [1] have shown that in disordered metals sample-specific random quantum interference of electron waves gives rise to the "universal conductance fluctuations" (UCFs). We have found, as illustrated in fig. 7, that the conductance of our devices as function of magnetic field shows aperiodic oscillations that can be interpreted as UCFs. From analysis of the data shown in fig. 7 we derived the rms deviation from the mean of the conductance, $\langle \delta g^2 \rangle^{1/2}$ and the correlation function in the magnetic field $F(\Delta B) = \langle \delta g(B).\delta g(B+\Delta B) \rangle$, from which the correlation length B_c was obtained. The angular brackets denote averaging over

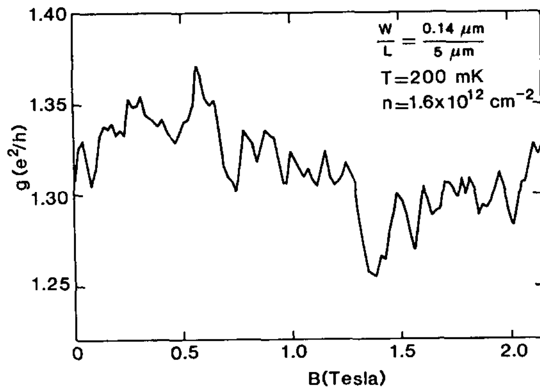

Fig. 7. Reduced conductance g of a narrow channel MOSFET as function of the perpendicular magnetic field at 200 mK. As argued in the text the oscillations are UCFs.

the magnetic field. The values obtained are $<\delta g^2>^{1/2}$(exp) = 0.023 and B_c(exp) = 0.087 T. The theoretical expressions [7,8] appropriate for our situation (L_T=1.3 μm and L_{in}=0.52 μm, L_{in} obtained from the magnetoconductance at 1.8 K assuming $L_{in} \propto <g> T^{-1/2}$) are $<\delta g^2>^{1/2} = 0.729 (L_{in} / L)^{3/2}$ and $B_c = (2.4\, h / e) / L_{in}^2$. From this we find $<\delta g^2>^{1/2}$ (theory) = 0.024 and B_c (theory) = 0.037 T. Comparing the experimental and theoretical values, we conclude there is good agreement.

5. CONCLUSIONS

In conclusion, we have developed a process for the fabrication of MOSFETs with 0.1 μm gate width. The process combines optical and electron beam lithography and produces devices very well suited for quantum transport studies at low temperatures. The smallest working devices have a 0.14 μm wide gate. On our devices we performed weak localization, magnetoconductance and universal conductance fluctuation experiments. The experiments done so far to a large extent confirm present-day theory. However, in later experiments that are not reported here (gate voltage dependence of the conductance near the strong localization regime) we have found interesting deviations that do not fit the theoretical framework mentioned above.

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