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Dynamics of metastable defects in a-Si:H/SiN TFTs

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Abstract

This paper has aimed at creating a more complete picture about the instability mechanism responsible for a-Si:H/SiN TFTs degradation. Additional insight about the degradation kinetics in a-Si:H/SiN TFTs is obtained by the in-situ monitoring of the source to drain current during alternative periods of stress and relaxation. The results presented in this paper come to the conclusion that the physical mechanism responsible for instability of the device operating at low bias stress, short stress time and different temperatures is a combination of defect creation and the trapping/detrapping of the carriers.

Keywords: Instability; Degradation; Interface state creation

1. Introduction

Because of inexpensive and common deposition technology, but mostly because of ease in integration, the a-Si:H TFTs are gaining in popularity. However, their areas of application are restricted to those applications where the TFT is used as a switch. Working as a switch, the TFT is subjected to repeated stress periods that degrade the electrical characteristics.

The two models acknowledged for physical interpretation of the degradation are the charge trapping in the gate insulator and the creation of states at the interface of a-Si:H/a-SiN:H and a-Si:H [1]. The threshold voltage shift is mainly due to state creation below a critical value of the gate voltage and due to charge trapping above this value. The value of critical voltage depends on the nitride band gap and it is reported to be 55 V [2]. When the state creation dominates, the threshold voltage shift shows a power law time dependence, but a logarithmic time dependence for charge trapping. Moreover, the threshold shift is thermally activated for state creation and temperature independent for charge trapping.

We have presented a method to study progressive degradation under various operating conditions, and that will add insight into the mechanism responsible for instability in a-Si:H/SiN TFTs.

The stretched exponential equation $|\Delta V_t| = |\Delta V_0|\{1 - \exp[-\left(\frac{t_{st}}{\tau}\right)_\beta]\}$ describes the defect creation mechanism and it has been explained by the stabilisation of a Si–Si broken bond by hydrogen (dispersive-hydrogen diffusion). In this model, the defect formation rate is governed by the hydrogen diffusion $\frac{d\Delta N_{db}}{dt} = -D_h \Delta N_{db}$, where the hydrogen diffusion coefficient is given by $D_h = D_0(\omega t)^{-\alpha}$; D_0 is a microscopic diffusion; ω is attempt-to-escape frequency and $\alpha = 1 - \beta$ [3]. For short stress time, the stretched exponential equation reduces to power law time dependence $|\Delta V_t| = |\Delta V_0|\left(\frac{t_{st}}{\tau}\right)_\beta$.

The threshold voltage shift under BTS measurements is usually obtained by extrapolating to the gate voltage axis for a small V_{ds} or by plotting $\sqrt[n]{I_{sd}}$ and varying the root to get the best fit. The disadvantage of this method is that the gate bias stress is interrupted and charge relaxation could occur. We monitored the source-to-drain current without any interruption of the procedure, moreover we described a complete mea-

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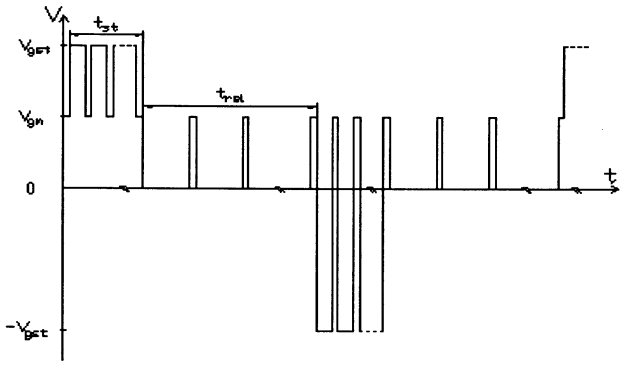

Fig. 1. Measurement sequence.

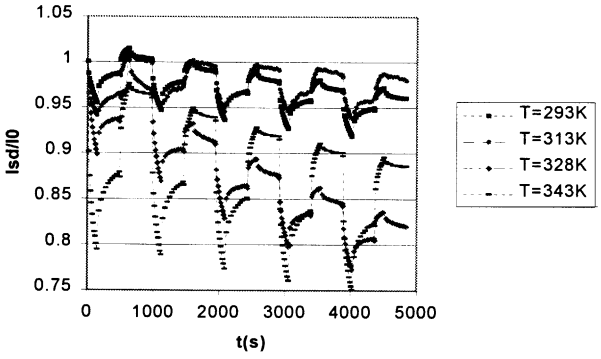

Fig. 2. Normalised time dependence of source-to-drain current.

surement procedure that adds insight on the degradation kinetics and the mechanism responsible for a-Si:H TFTs degradation.

2. Experiments and results

The devices under test (DUT) were top gate a-Si:H/SiN ($W/L = 18/9$) TFTs on a glass substrate. Each experiment was performed on a 'fresh' device. The measurement of the source to drain current I_{sd} is a consequence of a continuous alternation of pre-defined positive stress ($+V_{gst} = 20$ V, $V_{dst} = 0.5$ V, $V_{sst} = 0$ V), relaxation (0 V), negative stress ($-V_{gst} = 20$ V, $V_{ds} = 0.5$ V, $V_{sst} = 0$ V), and relaxation again. The sequence also occurs at pre-defined time intervals $t_{st} =$ 100 s (total stress time) and $t_{\mathrm{rel}} = 300$ s (relaxation time). A measurement is performed at every $t_{\mathrm{pollst}} = 10$ s (stress polling interval) and $t_{\mathrm{pollrel}} = 30$ s (relaxation polling interval) when the stress voltages switch to measurement voltages $V_{gm} = 10$ V, $V_{dm} = 0.5$ V, $V_{sm} = 0$ V. The very first data point I_0 is a pure measurement before any stress is applied to the device (Fig. 1).

Choosing $V_{gst} = 20$ V assigns the degradation mechanism as a defect creation. By lowering V_{gm} with respect to V_{gst}, we aimed to minimise the influence of measurement in the state of the system and assume that the measurement itself does not induce stress effects. Since the defect creation mechanism is temperature dependent, we introduce temperature as a variable in our experiment. The chuck temperature T_{st} modifies from DUT to DUT in the range 273–343 K. By monitoring the I_{sd} in time while applying a gate voltage stress and a low drain bias at a given temperature, we obtain a repeated pattern with a descendent trend (Fig. 2).

When a positive bias is applied to the gate electrode, the negative charge stored in the channel region of a-Si:H and, residing in the gap states, gets trapped in the empty localised states present in the transitional regions and located at lower energies. The phenomenon does not seem to saturate even at $t_{st} \sim 1500$ s. It is a very fast process, moreover, the difference between the initial I_0 and the very next I_{sd} value is considerably larger than the difference between any subsequent stresses, and this could be related to the interface state creation.

After the period of gate bias stress, when the electrodes are grounded in the first relaxation period, an amount of trapped charge is released from the traps and I_{sd} recovers partially; therefore, relaxation plays a role in annealing. We allowed the device to relax for a longer time in order to study the current recovery. However, the relaxation process seems to saturate in approximately 70 s at room temperature and it tends to

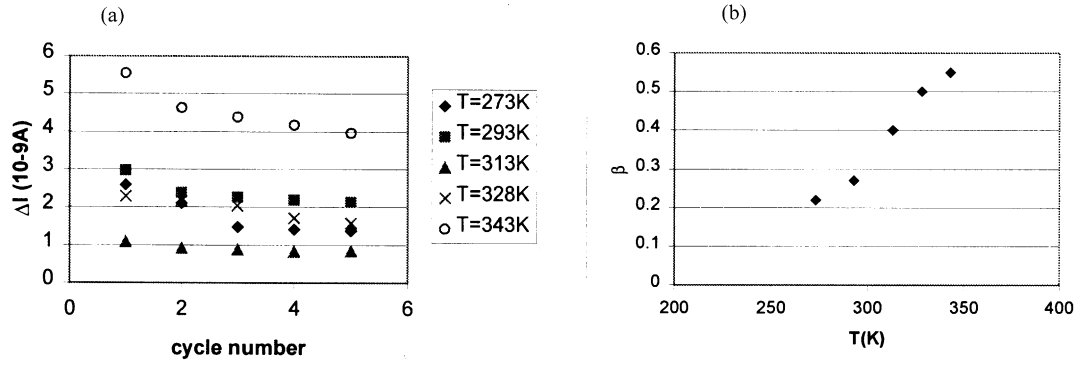

Fig. 3. The drop in the source-to-drain current in the first cycle vs. temperature (a) and the temperature dependence of the exponential coefficient calculated for the positive stress period in the first cycle (b).

saturate at longer stress times as the temperature increases, suggesting that the relaxation process could occur via hopping through localised states. This dispersive process has been reported previously in the literature [4].

During the negative stress period the removal of charge from the traps continues and almost a full recovery is noticed. The reverse bias offers an extra-recovery of the current values.

During the second relaxation period, trapping of the carriers is noticed again. In the subsequent stress/relaxation periods, further trapped charges accumulate and are released.

By this time, the device is irreversibly damaged and the application of a reverse bias could not recover the I_{sd} values registered at the beginning of each cycle. The decrease in the current values as stress temperature increases is noticed in the first cycle, but in the subsequent cycles a transient trend overlaps this effect (Figs. 2 and 3).

The exponential coefficient β of 0.2–0.5 and the characteristic time τ of 10^3–10^5 were calculated from the slope and the intercept of the curve $\ln\left(1-\frac{I_{ds}}{I_0}\right) = f(\ln t)$. The β values calculated in the positive stress period of the first cycle represent linear temperature dependence. Close values were obtained for the first relaxation period, suggesting that the relaxation annealing of the defects was created by the applied stress. The transient trend does not show temperature dependence but power law dependence in time with the β value calculated in the first cycle, suggesting that defect creation is a fast process mainly related to the interface states.

3. Conclusion

Working as a switch, the TFT is subjected to repeated stress periods. The method we describe in this paper emphasises the influence of repeated duty cycles on the degradation of TFTs. This paper studies the process of degradation by introducing a new approach to interpret the degradation of a-Si:H/SiN TFTs. Through this study, we aimed to get a closer view of the origin and kinetics of the degradation phenomenon in a-Si:H/SiN TFTs.

The measured values of I_{sd} show a progressive degradation of DUT and a repeated sequence, as in the case of trapping/detrapping on existent states of a finite number of carriers. Seemingly, the number of states is changing as a consequence of the repeated applied bias stress.

The results came to the conclusion that two mechanisms are involved at $V_{gst} = 20$ V: defect creation of the states and trapping/detrapping of the carriers on the interface states induced by stress.

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