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A buried-channel charge-coupled device with non-overlapping gate structure for a CMOS/BCCD process

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Abstract. A buried-channel CCD is presented, suitable for integration in a high-energy ion-implanted CMOS process. The BCCD channel is high-energy ion-implanted and the gate structure is non-overlapping. The required submicron spacings between adjacent gates are created by a sequence of processing steps. No demands are imposed on the lithography used. SEM photographs show a well-defined gate structure with straight spacings exhibiting minor width variation. The parasitic potential well, associated with the presence of spacing between the gates, has little influence on charge transport performance. Delay lines have been operated with transfer inefficiency of 10^{-5} and less.

1. Introduction

During the past two decades, the charge-coupled device (CCD) has shown a tremendous development in both sensor-based and electronic systems. Despite the focus on imaging applications during the last decade, significant results have been achieved in the field of signal processing [1–4]. CCD-based signal processing has to compete with other monolithic technologies like switched-capacitor (SC) and digital and active analogue filtering. It is expected that only the applications giving increased performance at equal or reduced costs will survive in the near future. A promising field of applications is video signal processing. Exploiting the serial data stream of video signals, CCDs are excellently suited for these applications [4–7].

This paper describes a low-voltage buried-channel CCD (BCCD) and its incorporation in a CMOS process [8]. The primary field of application of circuits fabricated with this process is signal processing in the range of video frequencies (signal frequencies up to a minimum of 5 MHz). Demands for a small transfer inefficiency (of the order of 10^{-5}) at high speed indicate the implementation of a BCCD. Practically all published CMOS/CCD processes were developed for signal processing applications [9–11]. Recently several advanced applications in video signal processing demonstrated the possibilities obtainable with a CMOS/CCD process [5,7,12]. CMOS offers both great freedom for design and a low power consumption. Power consumption is further reduced by the implementation of a non-overlapping polysilicon gate technology, which minimizes the interelectrode capacitance, contributing to the capacitive load of the clock drivers.

In section 2 the merging of CMOS and BCCD is discussed in general. The gate definition process, described in section 3, has been based on a proposal by Hosack and Dyck [13], implemented in its rudimentary form by Kapoor [14]. In this paper we present significant progress in the quality of definition, obtained by the implementation of anisotropic plasma etching. Scanning electron microscope (SEM) photographs demonstrate the results. Section 4 discusses the influence of interelectrode spacings on BCCD performance. Both simulation and experimental results are presented. A nearly perfect BCCD operation has been obtained on fabricated devices with interelectrode spacings of 0.3 μm. Finally in section 5, the conclusions are summarized.

2. General processing considerations

The high degree of compatability in CMOS and BCCD processing permits a straightforward combination of both in a single process [9–11]. In order to provide continuity in both circuit design and processing environment, a newly designed BCCD has been integrated in the existing CMOS process. A schematic cross section of the CMOS devices and BCCD is presented in figure 1.

The CMOS process is a retrograde twin-well process, employing high-energy ion implantation [8]. A shallow 3–5 μm, 5–10 Ω cm, p-type epitaxial layer on a low-resistivity substrate is used to enhance latch-up hardness.

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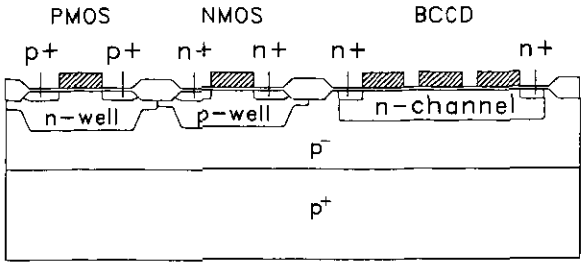


Figure 1. Cross section of the CMOS transistors and BCCD.

The gate oxide thickness is 25 nm. The CMOS process has been designed for 5 V applications. In order to preclude excessive biasing conditions of transistors in the periphery of the BCCD, its supply voltage has been determined to be 9 V.

The CMOS process uses nine masks. Addition of the BCCD requires a minimum of two extra masks. Incorporation of the BCCD influences processing with regard to the definition of the BCCD channel and the gate structure. For correct BCCD operation, a so-called 'closed'-gate structure is required with zero or deep submicron spacing between adjacent phases.

Analogous to the CMOS wells is the BCCD channel implanted with high-energy ions. As far as we are aware, this is the first fully high-energy ion-implanted CMOS/BCCD process with deep channel BCCD described in the literature. The use of high-energy ion implantation avoids prolonged diffusion steps and therefore facilitates the incorporation of the BCCD in the CMOS process. The BCCD channel consists of two high-energy phosphorus implantations with a total dose of 1.5×10^{12} cm^{-2} and a maximum implantation energy of 560 keV. The implanted layer shows a homogeneous doping profile with junction depth of 0.8 μm, the charge transfer depth being 0.5 μm. The BCCD channel is defined by a masking step prior to the channel implantation. Damage annealing is performed at 800°C.

3. Gate definition process

At present the double and triple layer polysilicon technologies are the mainstream gate definition processes used in CCD processing. Since the polysilicon layers overlap, a closed-gate structure is readily obtained. A source of concern is the isolation between the phases in the overlap region, especially when scaling down the gate oxide thickness. In order to ensure sufficient isolation, present CCD processes with thin gate oxides use spacers to encapsulate the lower polysilicon gates [15]. An important drawback remains the interelectrode capacitance, related to the overlap of the phases. This capacitance contributes significantly to the total capacitive load of the clock-phase drivers. Non-overlapping gate structures with submicron spacings may offer a reduction by a factor of 2.5 in interelectrode capacitance, thus relaxing the demands on the clock driver circuits [16].

Spacings between adjacent gates should not exceed 0.5 μm for good BCCD operation. For larger spacings, parasitic potential maxima will occur in the channel and may trap signal charge, as discussed in section 4. Because direct optical definition may take several years to achieve, previous direct dimensioning has been performed with e-beam lithography [17, 18]. If e-beam lithography is not considered a viable alternative, a technological solution may be considered.

All known processes for the technological definition of submicron spacings or 'gaps' are based on the creation of a feature with desired submicron dimension at the edge of a particular assisting layer. The assisting layer is patterned by means of standard lithography. This step defines not the dimensions but merely the location of the spacing. It is also a fact that an image reversal as shown in figure 2, from submicron feature to submicron spacing, is always needed. This image reversal is obtained by the application of a local surface treatment. A straightforward implementation is a thermal oxidation of the polysilicon layer to be etched. During oxidation, the growth is inhibited in the gap region by the submicron feature. This feature is therefore created from a silicon nitride layer.

Several alternatives have been described, based on the above-mentioned principle. In [19] a nitride spacer is used to create submicron trenches in a silicon substrate. Another implementation exploits the lateral oxidation of a second polysilicon layer, also known as the PABLO technique [20] (PABLO stands for perfect alignment by lateral oxidation; its feasibility is demonstrated by the fabrication of an experimental 100 K CCD memory [21]). The prolonged oxidation of the polysilicon layer and the corresponding thermal budget are disadvantages of this implementation. The edge-etch technique, proposed by Hosack and Dyck [13] and implemented by Kapoor [14] does not suffer from this. Therefore, their concept has been applied in this work. We present an application using anisotropic plasma etching instead of wet and isotropic plasma etching, which gives poor linewidth control. Thus a considerable improvement in the accuracy of definition of submicron features is obtained.

The gate definition process [16,22] starts after the well formation and gate oxide growth. Topography on the wafer is caused by the LOCOS isolation. The bird's beak length is 0.75 μm and the step height from active area to isolation region is about 0.25 μm. The gate definition process is illustrated in figure 3. SEM analysis

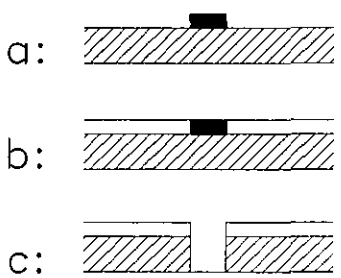
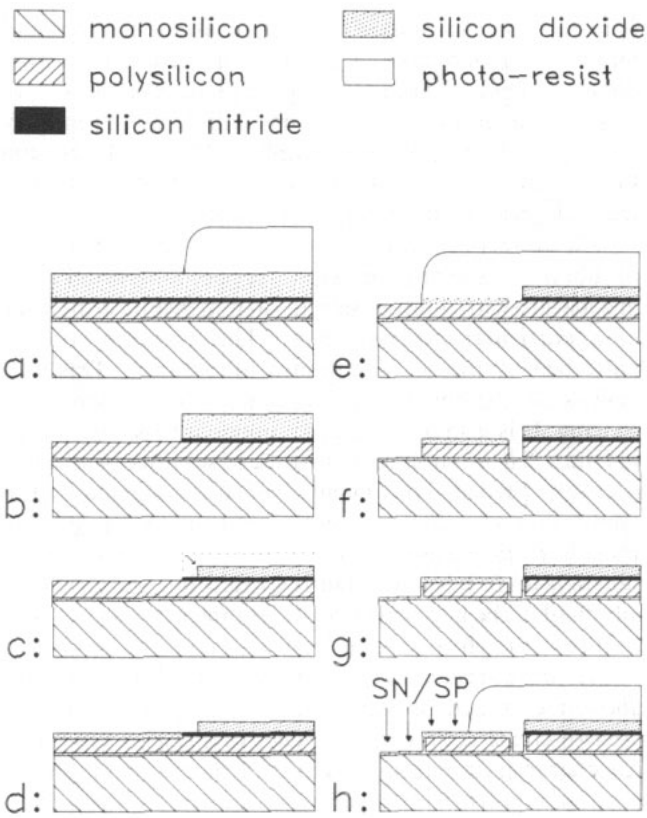
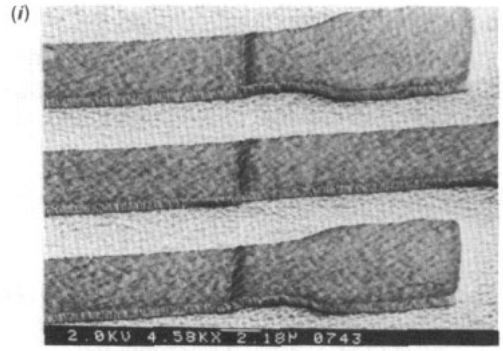
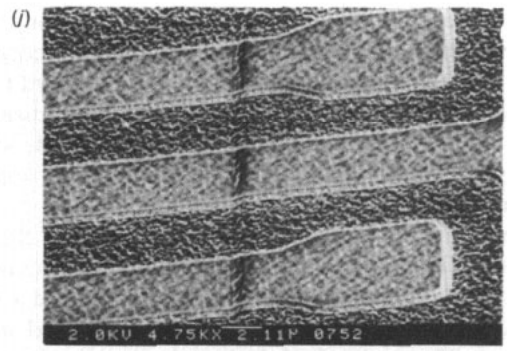
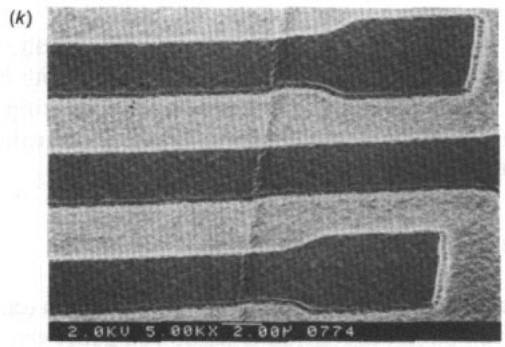


Figure 2. Image reversal, required for the technological definition of a submicron spacing. First a submicron feature is created (*a*). This feature is used to create an etch mask (*b*). Finally the original feature and the submicron spacing are etched (*c*).









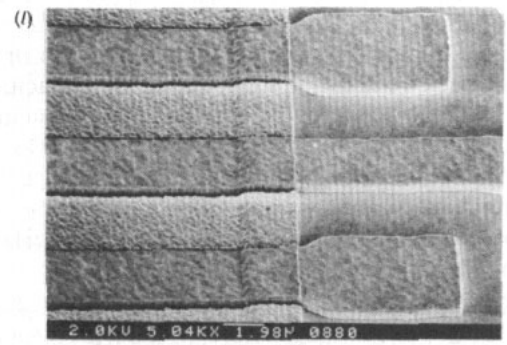


Figure 3. Flow of the gate definition process.

1. Starting point: stack of gate oxide, polysilicon, silicon nitride and silicon oxide.
2. Application of photoresist pattern (GD mask) (*a*).
3. Definition of the oxide–nitride stack.
4. Resist strip (*b*, SEM photo *i*).
5. Isotropic back-etch of oxide (*c*, SEM photo *j*).
6. Growth of oxide on exposed polysilicon (*d*).
7. Etch of exposed silicon nitride (SEM photo *k*).
8. Application of photoresist pattern (PS mask).
9. Definition of masking oxide (*e*).
10. Resist strip.
11. Etch of polysilicon (*f*).
12. Growth of passivating oxide (*g*, SEM photo *l*).
13. Application of photoresist and shallow n^+ and p^+ SN/SP implantations (*h*).

was used to tune the processing through the entire gate definition process. A selection of the photographs, obtained at several stages during the gate definition process, are shown in this figure as well. The starting point is the stack of gate oxide (25 nm), polysilicon (500 nm), silicon nitride (50 nm) and silicon oxide (700 nm).

The first step of the gate definition process is the exposure of the GD mask in resist (figure 3(*a*)) (GD stands for 'gap location definition'). Gaps may result at the edges of the patterns defined with this mask. With the GD pattern in resist as a mask, the silicon oxide–silicon nitride stack is etched anisotropically in a CHF_3–O_2 plasma (figure 3(*b*)). After removal of the resist, the key step of the gap definition follows, namely the lateral back-etch (figure 3(*c*)). The silicon oxide layer is isotropically etched back, the amount of lateral etching defining the gap width. The back-etch is performed in a thermostatted bath with a buffered high-purity NH_4F–HF mixture. The etch rate is low (70 nm min^{-1}) and reproducible. Both the anisotropic definition of the silicon oxide–silicon nitride stack and the controllability of the back-etch contribute greatly to the quality of the gap definition.

After the lateral back-etch the exposed polysilicon is oxidized in a wet ambient at 900°C for 40 min (figure 3(*d*)). Thus the image reversal has been completed and next the superfluous silicon nitride rims are etched. The previously grown oxide layer is patterned with the PS (polysilicon') resist pattern as the mask (figure 3(*e*)). After removal of the resist and cleaning of the wafer, the polysilicon is etched anisotropically in a Cl_2–$SiCl_4$ RIE plasma (figure 3(*f*)). The GD- and PS-defined silicon oxide patterns function as etch masks during this step. Finally, the polysilicon sidewalls are passivated during oxidation (figure 3(*g*)). Simultaneously, the integrity of the oxide in the gap region and source/drain areas is restored. During the source and drain implantations, the gaps are protected by a layer of photoresist (figure 3(*h*)). The process finishes with a conventional single-metal back-end process.

4. Results and discussion

All polysilicon features are etched in a single step (step 11 in figure 3). During this etch silicon oxide acts as an etchmask. In order to define arrays of isolated gates and areas free of polysilicon, a pattern is etched in the masking oxide (Step 9 in figure 3). This pattern intersects the previously defined etch mask of the gaps. A sharp transition from gap to open area results without any edge effect, as may be seen in figure 3(*l*).

The signal charge in the BCCD channel under the gap is less influenced by the gate potential, due to the increased distance to the gate. The reduced coupling manifests itself as a local maximum in the channel potential and is thus a possible trap for signal charge. The potential well Ψ_w is defined as the difference between the maximum potential in the gap region and the minimal

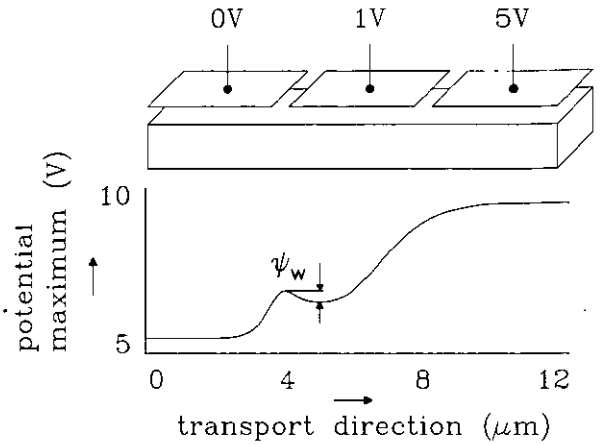


Figure 4. Definition of the potential well Ψ_w. The maximum potential is determined over the depth of the CCD channel.

potential maximum in the transport direction below the adjacent gate, as illustrated in figure 4. The potential well Ψ_w depends strongly on gap width. The potential well was determined experimentally by a conductivity measurement [16]. Test devices with gap widths of 0.2 and 0.5 μm were fabricated and analysed. In figure 5 the results are compared with simulated values. The difference between experimentally determined and simulated values for the potential well Ψ_w is attributed to the actual geometry in the gap region. In figure 6 a SEM photograph of a cross section of a 0.5 μm gap test device is shown. The wedge of oxide at the edge of the gates is clearly visible. It is a result of the final passivating oxidation. This oxide wedge reduces the coupling between gates and channel through the lower dielectric constant of silicon oxide compared with silicon. The size and form of the wedge are determined by the oxidation step rather than the gap width. Therefore the relative influence of the wedge increases for small gap widths, as can be seen in figure 5.

Potential wells may limit charge-transfer efficiency when present at the trailing side of a charge packet. A fraction of the mobile charge, present under the hindmost storage gate is trapped in the potential well and separated from its charge packet. Two-dimensional transient simulations with TRENDY [23] have shown that gaps

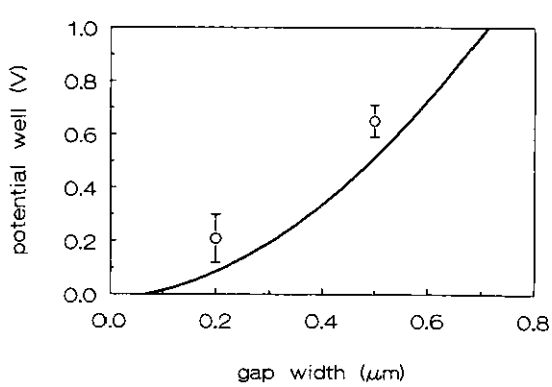


Figure 5. Comparison of the simulated values for the potential well (drawn curve) with experimental results (circles).

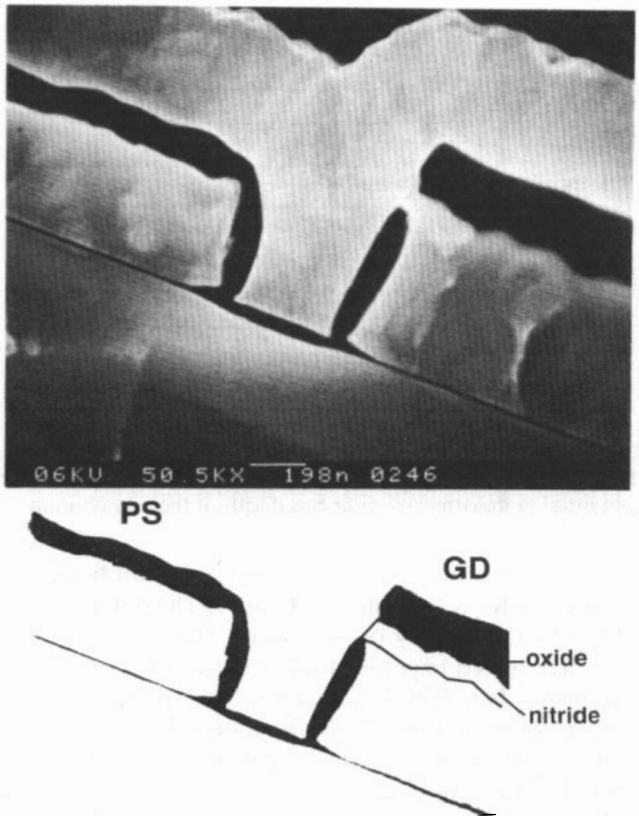


Figure 6. Cross-section SEM photograph of a 0.5 μm gap test device (*a*). The diffeent layers (*a*) are distinguished in the stylized drawing (*b*).

smaller than 0.5 μm enable an almost perfect charge-transport behaviour. For a device with 0.4 μm gaps and 4 μm gate length a fraction of the order of 10^{-5} per transfer is trapped in the gap region. This was for a maximum size charge packet of 22 pC cm^{-1}. Smaller charge packets are transported under ideal conditions since charge transport ceases before the potential well Ψ_w builds up.

Actual transfer inefficiency (ε) measurements support the simulations. Measurements have been performed on processed delay lines with fill-and-spill input and reset floating diffusion output [24]. The number of delay sections was 50 and 200 respectively, with four phases per delay section. The gate length is 4 μm for all phases and the gap width is 0.3 μm. The transfer inefficiency ε was determined from the transfer function $|H(f)|$ of the delay line [25]. The measured transfer function was fitted to a model describing the influence of ε. Only marginal deviations from theory in the frequency range from 0 Hz to clock frequencies f_c of 2 MHz were found. Higher operating frequencies were excluded due to the limited current-drive capability of the output. The high accuracy of the measurement technique allowed us to determine the upper limit of the confidence interval of ε to 10^{-5}, which is considered a worst-case value.

5. Conclusion

In this paper we have presented a buried-channel CCD, as part of a high-energy ion-implanted combined CMOS/BCCD process. Also the BCCD channel is high-energy ion-implanted, which enhances the compatibility with the CMOS processing. Integration of the BCCD requires two additional masking steps for the definition of the BCCD channel and the realization of the closed-gate structure.

The non-overlapping BCCD gate structure reduces the interelectrode capacitances. The definition of deep submicron spacings is performed by a sequence of processing steps, based on an edge-etch technique [13]. This work presents significant improvements in the definition technique by the implementation of anisotropic plasma etching. No demands are imposed on the lithography used. Extensive SEM analysis demonstrated a well-defined gate structure with straight spacings showing minor width variations. The deep submicron spacings between adjacent gates make good charge-transfer performance possible.

The spacings between adjacent gates induce parasitic potential wells that may trap signal charge and degrade charge-transport performance. Experimental verification of the potential wells supports theory. It is shown that for spacings below 0.5 μm only a marginal influence on charge transport remains. Operated delay lines showed transfer functions with hardly any deviation from theory. Charge-transfer inefficiency has been determined to be less than 10^{-5}.

Acknowledgments

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References

[1] Wallinga H and Pelgrom M J M 1980 An electrically programmable split-electrode charge-coupled transversal filter (EPSEF) *IEEE J. Solid-State Circuits* **15** 899-907

[2] Schreiber R *et al* 1981 Passive CCD resonator filters *IEEE J. Solid-State Circuits* **16** 125-9

[3] Vogelsong T L, Tieman J J and Steckl A J 1985 Charge-domain integrated circuits for signal processing *IEEE J. Solid-State Circuits* **20** 562-70

[4] Narabu T *et al* 1986 CCD delay line for video TBC *IEEE Trans. Consumer Electron.* **32** 666-72

[5] Miura H, Masuda I and Sato M 1987 A CMOS-CCD signal processor for skew compensation *ISSCC Digest Tech. Papers* 112-3

[6] Pelgrom M J M, Jochijms A and Heijns H 1987 A CCD delay line for video applications *IEEE Trans. Consumer Electron.* **33** 603-9

[7] Maki Y *et al* 1988 A CMOS-CCD comb filter with dropout compensation for a VCR *ISSCC Digest Tech. Papers* 46-7

[8] Stolmeijer A 1986 A twin-well CMOS process employing high-energy ion implantation *IEEE Trans. Electron Devices* **33** 450-7

[9] Dawson R *et al* 1979 A CMOS/buried-n-channel CCD compatible process for analog signal processing applications *RCA Rev* **38** 406–35
[10] Ong D 1981 An all-implanted CCD/CMOS process *IEEE Trans. Electron Devices* **28** 6–12
[11] Tower J R *et al* 1982 A CMOS/CCD 256-stage programmable transversal filter *IEEE J. Solid-State Circuits* **17** 1062–9
[12] Veendrick H J M *et al* 1988 An 835 Kb video serial memory *ISSCC Digest Tech. Papers* 44–5
[13] Hosack H H and Dyck R H 1977 Submicron patterning of surfaces *IEEE J. Solid-State Circuits* **12** 363–7
[14] Kapoor V J 1981 Charge-coupled devices with submicron gaps *IEEE Electron Device Lett.* **2** 92–4
[15] Davids G J T *et al* 1988 CMOS technology for CCD video memories *Proc. ESSDERC '88, J. Physique* **49** C4 41–4
[16] Warmerdam L F P 1990 Development of a combined CMOS/BCCD process with self-aligned gate structure *PhD Thesis* University of Twente, The Netherlands
[17] Hashimoto N and Saito N 1975 N-channel narrow gap charge-coupled devices using electron-beam lithography *Thin Solid Films* **27** 89–93
[18] Slotboom J W *et al* 1984 Submicron CCD memory structures fabricated by electron-beam lithography *IEDM Tech. Digest* 308–11
[19] 1986 Submicron isolation trenches in silicon *IBM Tech. Disclosure Bulletin* **28** 3419–22
[20] Maas H G R and Appels J A 1984 PABLO a versatile VLSI technology *Philips J. Res.* **39** 103–8
[21] Slotboom J W *et al* 1986 High-density CCD video-memories: physics and technology *Proc. ISSDM Tokyo* (Japan. Soc. Appl. Phys.) pp 315–8
[22] Warmerdam L F P *et al* 1989 A self-aligned gate definition process with submicron gaps *Proc. ESSDERC '89* (Berlin: Springer) pp 37–40
[23] van Schie E, Wolbert Ph B M and Middelhoek J 1989 TRENDY: a 2D process and device modeling and simulation environment *Proc. NASECODE VI* (Dublin: Boole) pp 155–61
[24] Howes M J and Morgan D V (ed) 1979 *Charge-Coupled Devices and Systems* (New York: Wiley)
[25] Wallinga H 1979 A general model for the frequency response of multiphase charge transfer delay lines *IEEE J. Solid-State Circuits* **14** 653–5