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Test structures and their application in structural testing of digital RSFQ circuits ☆

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Abstract

As the niobium (Nb) LTS RSFQ processes advance being the technology for future ultrahigh-speed systems in the digital domain, the quality of the process should be maintained high for a successful realization of these complex circuits. A defect-oriented testing (DOT) approach is essential so as to increase the yield of the process. Little information is available in this area and the recent increase of Josephson junctions to around 90,000 per chip requires a detailed study on this topic. In this paper we present how DOT can be applied to RSFQ circuits. As a result of a study conducted on an RSFQ process, a list of possible defects has been identified and described in detail. We have also developed test-structures for detection of the top-ranking defects, which will be used for the probability distribution of faults in the process. One of the highly probable defects will be used to elaborate the DOT technique for fault modeling and simulation purposes.

Keywords: Structural testing; Defect-oriented testing; Superconductor devices; RSFQ circuit testing; Fault modeling

1. Introduction

The requirements for efficient high-speed electronic devices in telecommunication and computing are increasing rapidly. Current semiconductor technologies will not be able to handle these requirements in speed and accuracy in the near future. Even at immature stage, superconductor electronics is capable of handling these tasks. Examples of such complex devices are a Superconductor ADC [1] and the Flux microprocessor chip [2].

As the complexity of the superconductor circuits is increasing to almost a 100,000 Josephson junctions (JJ) per chip [2], realization of the design becomes a difficult task. Although extended research is going on in making complex circuits and scaling down the minimum sizes, very little or no information is available in literature on the

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methodology for achieving high yield for superconductor electronics. The yield levels are much lower than in the semiconductor industry [3]. This is due to the fact that little information is available on superconductor processes while much research has been carried out with respect to the defects in semiconductor manufacturing processes [4]. Special test structures have been developed and realized along with the integrated circuits (ICs). The information gathered using these test structures is used for yield analysis and defect-oriented testing (DOT) [5]. Fault models have been developed after studying the behavior of the test structures. These fault models are then used for fault simulation of the circuit. In this way, the semiconductor industry has developed methodologies and techniques to achieve high yields.

In this paper, test structures that can be used to detect the top-ranking defects that can occur in a niobium tri-layer based technology and their application to DOT of RSFQ circuits are discussed. The organization of the paper is as follows. The next section briefly explains general defects and their testing strategies. In Section 3, the JeSEF Nb tri-layer process is described followed by the defect analysis in Section 4. Associated test structures are presented in Section 5. The influence of these defects on circuits, by the usage of defect modeling and fault simulation, is tackled in the last section.

2. Defects and defect-oriented testing

The type of defects that can occur in an IC manufacturing process flow can be divided into two categories: design failures and manufacturing defects. They are named after the cause of the failure. We will only consider manufacturing effects, which can be classified into two subclasses:

1. Local (random) defects;
2. Gross manufacturing defects.

Defects that affect a large area, even a complete wafer, are called gross manufacturing errors. Random defects are named to illustrate their random occurrence in nature. This type of defects is important because they contribute to the majority of their kind in a mature process.

The most common defects that occur are shorts between the same metal layer resulting from extra material and bridges between different metal layers due to bad isolation layers. In addition there are opens in layers or in vias resulting from the absence of material. Cracking of metal layers due to step-coverage problems is another issue, which, in the worst case, can become an open in the layer.

The effective detection and avoidance of these defects in a manufacturing process are essential for the quality of the devices. Information about the defects in a process is gathered by using specially designed test modules also called Process Control Monitors (PCM). According to the information that can be acquired from PCMs, four types of test structures can be identified:

(a) Evaluation of the functional properties of IC building blocks (test circuits);
(b) Extractions of IC geometric parameters;
(c) Determination of the structural defect distribution and their influence on the yield (short, breaks etc.);
(d) Determination of electrical parameters like critical current (I_c of JJs or vias).

In this paper we will discuss the third type of test structures. Inductive fault analysis (IFA) is a widely used technique for DOT. It is based on the fact that the probability of a defect is a function of the local layout geometry and the distribution of failure mechanisms in a manufacturing process. A defect ranking is used to create a realistic fault list. Faults are the defects that can cause malfunctioning of the realized circuit in the technology under study. In IFA, the faults are sprinkled virtually on a fault-free layout according to the probability distribution of defects. Then, a detailed simulation of the circuit is carried out to evaluate faulty circuit behavior.

Until now, most research has been done on type a, b, and d errors, i.e. parametric defects in superconductor processes [6] and the functional verification of devices. As the processes become more mature, the importance of detecting the structural defects increases. This is due to the fact

that the occurrence of gross manufacturing errors and deviation of parametric values are decreasing due to the maturity of the process. However, random defects can still occur due to various reasons like the presence of impurities, local wafer defects and human errors.

3. The JeSEF tri-layer process

The process that we have been investigating is the JeSEF (Jena Superconductor Electronics Foundry) Nb tri-layer process [7] for realising RSFQ circuits. It has three metal layers including the ground plane (M0, M1 and M2) and a Mo-resistor layer R1. To reduce the probability of pinholes in the isolation layers between the conducting layers, the isolation is carried out in two separate steps one by niobium oxide and the other by silicon oxide. M0 and M1 are separated by I0A (Nb_2O_5) and I0B (SiO_2), while M1 and R1 by I1A (Nb_2O_5) and I1B (SiO_2). The T1 layer defines a JJ. A cross-section of the process is shown in Fig. 1. The minimum dimensions for interconnection width and spacing are 5 μm. The critical current density J_c for the process is 1 kA/cm^2 and the sheet resistance of the Mo-resistor layer (R1) is 1 Ω/square. The junction capacitance for the process is 0.05 pF/μm^2. Further details on the process are given in Ref. [8].

4. Defects in the JeSEF tri-layer process

We have conducted an investigation to get information about the types of defects that can occur in the JeSEF (RSFQ) process [9]. Looking at processed circuits, along with the design rules, 27 possible defects have been theoretically predicted for this process. At the time of investigation, only two types of test chips were available from JeSEF—Test Chip A and Test Chip B. These chips were designed to test the parametric variation of the process. The structures include fiske-step measurement, sheet resistance measurement and junction chains. Parts of these structures were used to study the occurrences of defects. Details of the measurements carried out are given in Ref. [10].

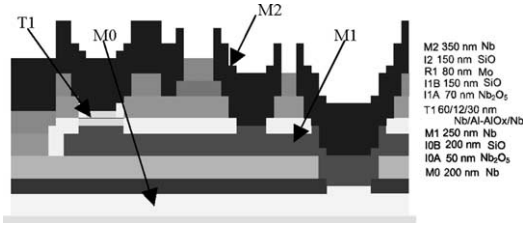

Fig. 1. Cross-section of the JeSEF RSFQ process.

These defects have been grouped and ranked into a list of probable defect locations. The primary defects are related to the thin oxide-barrier of a JJ. Shorts, opens and pinholes (in the thin barrier) are believed to cause junctions to malfunction. At a current stage of a process, the chance of a failure of a JJ is one in a thousand. Opens and near opens in the top metal layer (M2) form the second ranking defect, resulting from the step coverage profile of the underlying SiO_2 isolation layer. SEM photographs (Fig. 2) of this situation from the test samples support these arguments. Different other possibilities of opens or shorts in the different layers follow. A comprehensive list of the most probable defects is given in Table 1.

The fault list has been prepared by considering the following facts: the frequency of occurrence of the weak-spots and the topography of the defects. An actual rank list has to be made after verification by measurements on the designed test chips.

5. Test structures

A test chip (Fig. 3) has been designed for the JeSEF RSFQ process, that allows detection and localization of the defects listed in Table 1. Development of simple and easily-testable structures was crucial during the design phase. We came up with basically two types of structures. One set for low temperature (LT), 4 K, measurements and the other set for room temperature (RT), 294 K measurements [11]. This reduces the unnecessary complexity in the testing phase and test running costs. If necessary, the LT structures can be tested at RT and vice versa. The 4 K

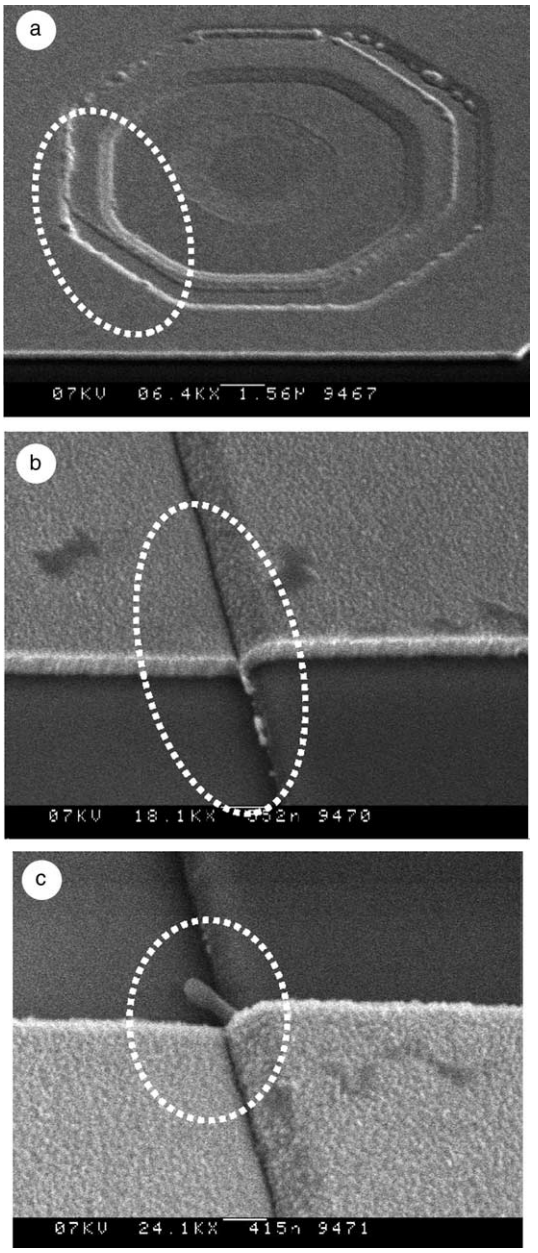

Fig. 2. SEM photographs of defective samples: (a) JJ, (b) M2-M1 cracked edge, (c) same as (b), but extra material that can cause potential shorts to nearby lines.

structures are placed at the four edges of the chip for easy bonding access. The RT structures are positioned at the centre of the chip, which can be accessed by the probes of an automatic tester.

Table 1
List of most probable defects in the JeSEF Nb tri-layer process

No.	Defect type	Nature of the defect
1.	Junction defects	Shorts and opens in metal electrodes, excessive size and number of pinholes in the thin barrier
2.	M2 defects	Opens or near opens as a result of underlying steps in M1
3.	Resistor defects	Opens or near opens in the M2 to resistor contact, opens and near opens in the Mo resistor, shorts in the Mo layer
4.	M2 via defects	Opens or near opens as a result of underlying via

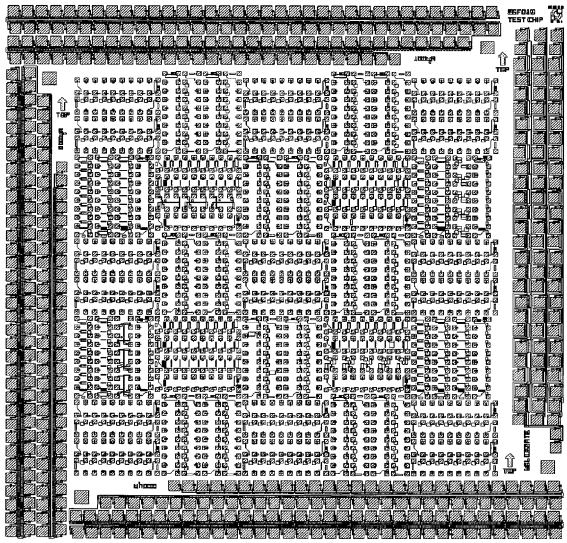

Fig. 3. Overview of the layout of the test chip; location of the RT are in the center and LT structures at the periphery for easy access for testing.

Test for structural defects is performed by measuring an electrical parameter of the test structure under consideration. Certain deviations from a nominal parameter value are then indicative for the presence of a defect. But, the test parameter will have a certain natural variation inherent in the process. This is generally assumed to be a normal distribution. The amount of natural variation is a function of the amount of test objects in a segment.

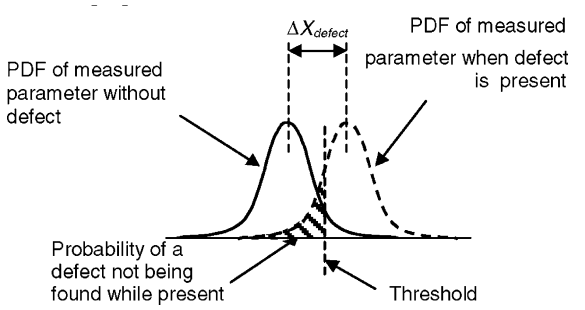

Fig. 4. Realistic probability distribution function (PDF) of measured parameters, when a defect is absent and present, showing possible overlap.

The presence of defects will cause parameter changes that result in a different distribution for the parameter values. In ideal case, the distributions of the parameter for the defect and defect free are separate. But, in a real case, there is a possibility of an overlap of the distribution by which the presence of a defect will be obscured by the natural parameter variations (in case of marginal parameter changes). A defect causing a change ΔX_{defect} will result in a shifted distribution depicted in Fig. 4, but can be handled by careful design of the structures [10].

5.1. Junction defects

Detection of the most probable JJ defect is going to be achieved at 4.2 K using a structure designed to reveal the most important junction quality parameters such as V_m [12,13] (a measure for the junction leakage) and the critical current of the unshunted junction. It has been suggested in literature [14] that the switching properties of the JJs can be used to find a single defect in a long chain of series connected JJs. Based on this suggestion, a model has been developed that has helped to create a method for detecting and pinpointing possible junction defects. The detection method has been developed to reduce the number of thermal cycles needed, thus reducing test cost and test time.

The method consists of an *IV*-curve measurement of several long series of JJs. From the *IV*-curves it can be determined whether one of the long series possibly contains a defective JJ. Detection of the defect by one of the suggested method in a JJ array is as shown in Fig. 5. Dynamic resistance is plotted versus forced current for a series of JJs. Here the result is for a series of 320 JJs with two of them being defective [10]. A long series that is thought to contain a defect can be further investigated in detail by performing *IV*-curve measurements on segments of the long series. The procedure can be repeated down to segments containing 20 JJs in series (Fig. 6).

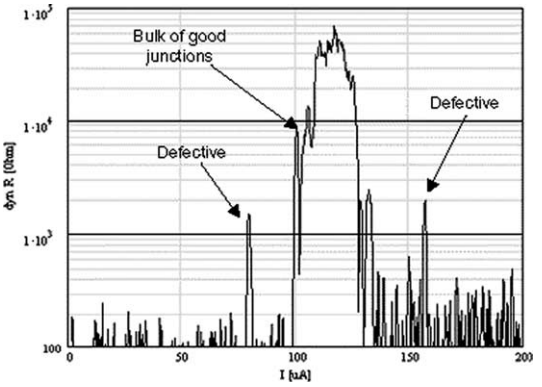

Fig. 5. Detection of defective JJs in a series: dynamic resistance versus forced current for a series of 320 junctions with two defective junctions.

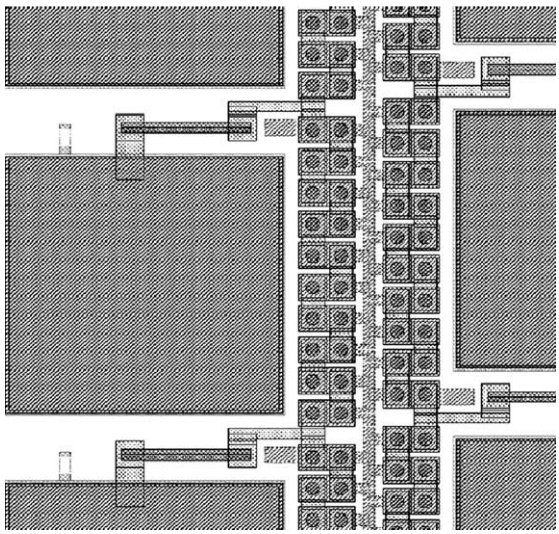

Fig. 6. Part of the layout of the JJ chains designed to test for junction defects. This structure can localise a defect down to 20 JJs.

The test chip contains three structures at the top, left and bottom edges of the chip, which each contain 2560 JJs in series. The JJ area has been varied among the three structures to determine possible area dependencies. The critical currents of the JJs in the structures are 100, 200 and 300 μA, respectively.

The disadvantage with this method is that bonding has to be done for the JJ access pads to the circuit board for measurements for each thermal cycle (time-consuming). This limits the number of measurements that can be done per cycle, again depending on number of the signal lines in the used cryo-probe. An alternative LT access technique like fingerboard design for the JJ structures restricts the number of structures that could be placed with reasonable localization of the defect.

A separate test structure has been designed in which deliberate defects, shorts and opens have been introduced into the JJs (Fig. 7). Shorts have been introduced by removing rectangular portions of different areas from the tri-layer definition (T1) (Fig. 8(a)). Opens have been created by removing rectangular portions from both tri-layer and anodisation definitions (I1A) (Fig. 8(b)). The purpose of this structure is to compare measurements of good and defective JJs, to compare measurement and theory and to develop a realistic fault model for the JJ.

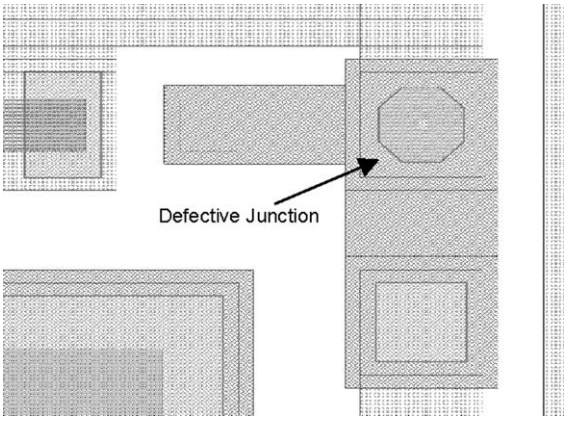

Fig. 7. Part of the layout showing the induced defective JJ to study the detailed faulty behavior.

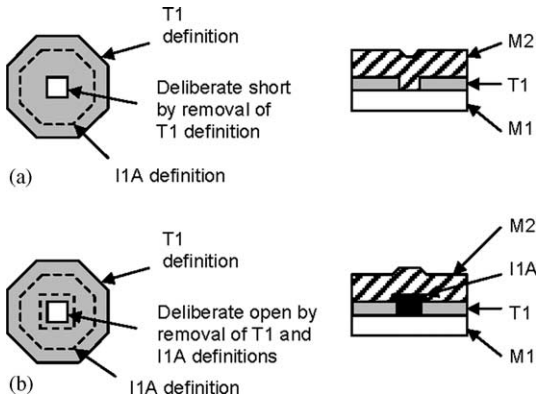

Fig. 8. Insertion of defects into the JJ and its cross-sectional view: (a) short in the tri-layer and (b) open in the tri-layer.

5.2. Other defects

Metal layer defects can be detected using a structure in which the metal structures runs over repeated steps of the underlying layer [15]. In our case, M2 strip running over repeated steps in underlying M1 strip (Fig. 9). At room temperature, the resistance of this path is going to be measured and compared with the resistance of a reference path, called "v/d Pol structure" [16], with the same layout, though without the steps in M1. Deviations in the average measured resistance will

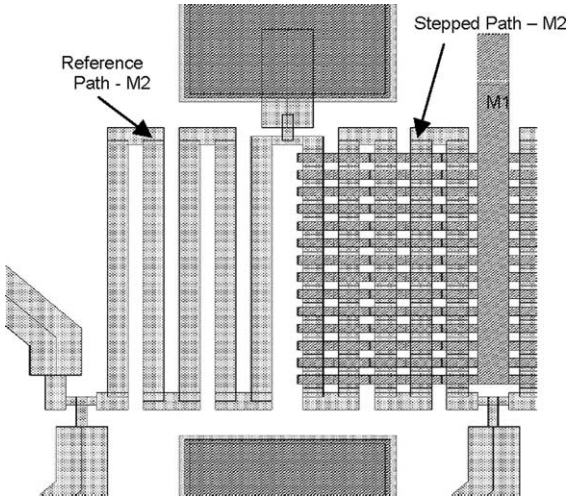

Fig. 9. Part of the layout of the test structure to detect opens and near opens in M2 layer.

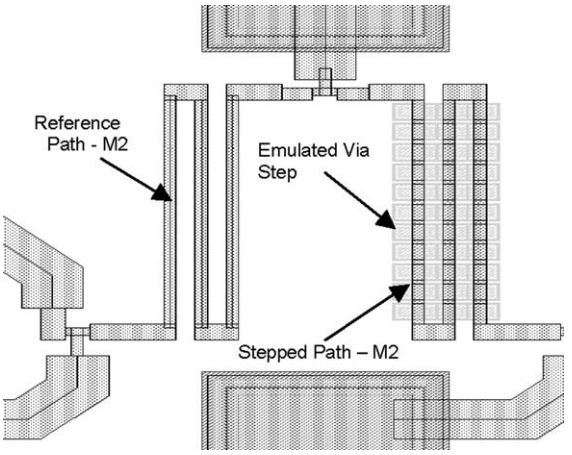

Fig. 10. Part of the layout of the structure for the detection of defects in M2 layer for step-coverage problem over a via.

reveal opens or near opens in the test structure. A structure similar to the above has been designed to test M2-via defects (Fig. 10). The via step was emulated by removing the corresponding isolation layers to form the test structure. Here in the case of a M2-M1 via, I1A and I1B are removed to form the required via step. M1 is removed so as to prevent a second conducting path. This prevents detecting multiple defects in the structure. The basis for the measurements is forcing a current and measuring the voltage at fixed power dissipation.

Resistors occur in two forms in superconductor electronics: as shunts for the JJs and as bias resistors. Test structures have been designed for both types. It consists of a series chain of resistors in which defects can be detected by determining the total resistance of such a chain at room temperature. The drawback of this structure is that it can only detect complete opens or near opens in the chain due to the relatively large natural parametric variations inherent in the process. There is no local reference except for the sheet resistance structure for the R1 layer.

6. The influence of defects on RSFQ circuits

The present method to achieve robust design is carrying out margin calculations for RSFQ circuits to fabricate them with optimum values. To a certain extent, this ensures that the allowed gross process variations and the allowed random local variations will not affect the accepted performance of the circuit. During the test phase, the common practice for digital circuits is to load the data into a shift-register (SR) at low-speed. Run the system "at-speed" and store the processed data in the output SR. Finally, the read out is carried out at a low-speed and the response is subsequently verified. This (functional) test will show whether or not the processed circuit will work. Further information about faults/ defects occurred is not available by this approach. Structural testing overcomes this problem because the faults are mapped to the physical defects in the process.

The defect statistics obtained from the above test structures will be used for IFA. Depending upon the type of defect occurring in the processed circuit, it can be classified as semiconductor-like defects and special defects that apply to superconductor circuits. Resistive bridges and shorts are examples of semiconductor-like defects that can occur in the circuit. Shorts in a JJ are an example of the second kind. Our early study on this subject was published in Ref. [17]. The induced faults in the developed test structures will be used to validate the results of our earlier studies.

As an example, in this paper, we will be considering the step—coverage problem of M2 over a M2-M1 via. The possible result of the step-coverage problem is cracking of the metal layer above the location and in the worst case it can form an open in the layer (Fig. 11). Detailed modeling approach is given in [9]. The severity of the situation depends on the ratio of the thickness of conducting layer to the thickness of insulating layer. Here a confluence buffer, commonly known

Fig. 11. Modeling of the step-coverage problem of metal layer as resistor.

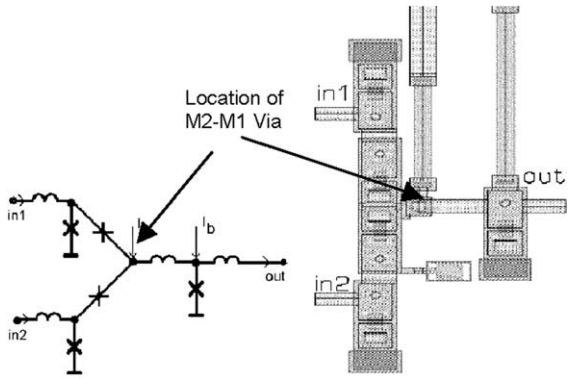

Fig. 12. Circuit and layout of the confluence buffer used for the fault-simulation of step-coverage problem of the M2 layer over a via.

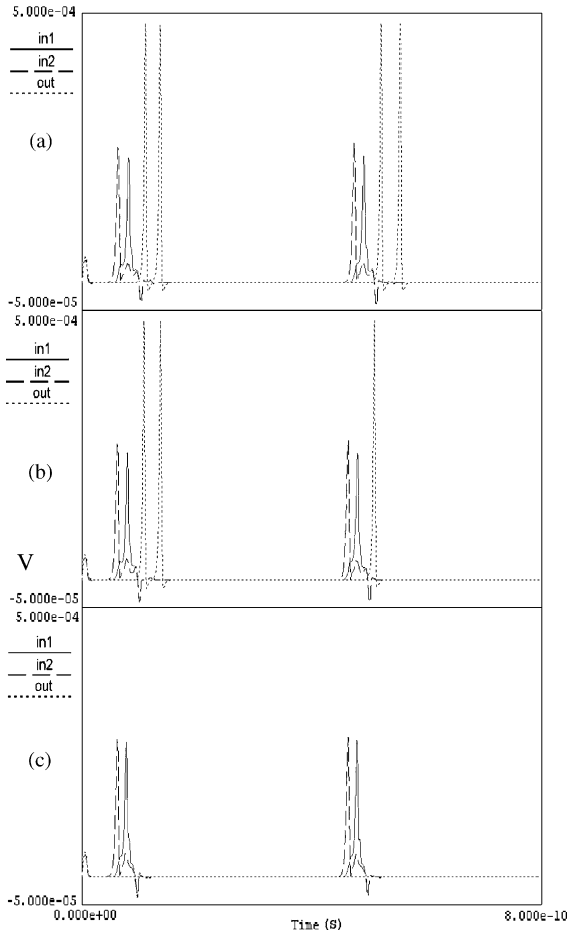

Fig. 13. Fault-free (a) and faulty simulation (b, c) of the confluence buffer for the step-coverage problem of the M2 layer over a via (see text).

as merger, is used to show the effects of the problem.

Fig. 12 shows the circuit and the layout of the confluence buffer, with marked location of the predicted defect. Here the effect of the defect is considered to be resistive. This is due to the fact that there will be an effective thinning of the conductive layer at the point of crack as seen in Fig. 11. The fault-free and fault-induced simulations of the circuit are shown in Fig. 13. The fault has been modeled as a resistor and introduced into the netlist of the confluence buffer. The correct operation is shown in Fig. 13(a). As the value of the resistor goes above 60 mΩ, the circuit starts misbehaving (Fig 13(b)) and as the resistance increase to 0.6 Ω, the circuit ceases to work (Fig. 13(c)). This shows that such a crack, even of a small depth, introducing 60 mΩ, in the chip can cause a fault to occur. Variation of the faulty response with the severity of the defect shows that the fault-model is realistic. A more detailed study of DOT at system-level for superconductor electronics was published in Ref. [18].

7. Conclusion

This paper discussed the defect-oriented methodology for the development of an Nb tri-layer process to achieve higher yield. This forms the basis towards a systematic DOT scheme for RSFQ circuits. The most probable defects that can occur in such a process were enumerated and test structures described in detail for each. These structures can be used to gather statistical information, i.e. the probability of the occurrence of defects in the process. Modeling and the influence of a defect that can create a fault in an RSFQ circuit are subsequently described using circuit simulations. This forms the first step for IFA, a commonly used DOT methodology for yield analysis.

Test results from measurements on these structures will be used to create a database for defects. This statistical information will be used as input for performing IFA. ''Defect-sprinkling'' over a fault-free circuit will be carried out according to the measured defect densities over various layers. The resulting information will indicate realistic faults. It

should be noted that this information is different from that obtained by Monte Carlo yield analysis on circuit margins. Comparing the results from both approaches, information on how yield is influenced by random defects can be inferred. Then adequate measures can be taken, depending on the nature of defect, so as to increase the yield. The details of the test results from the test structures and further study on the actual defect behavior are subject of a future paper.

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