Electrical properties of low pressure chemical vapor deposited silicon nitride thin films for temperatures up to 650 °C

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The results of a study on electrical conduction in low pressure chemical vapor deposited silicon nitride thin films for temperatures up to 650 °C are described. Current density versus electrical field characteristics are measured as a function of temperature for 100 and 200 nm thick stoichiometric (Si_3N_4) and low stress silicon-rich (SiRN) films. For high *E*-fields and temperatures up to 500 °C conduction through Si_3N_4 can be described well by Frenkel–Poole transport with a barrier height of ~1.10 eV, whereas for SiRN films Frenkel–Poole conduction prevails up to 350 °C with a barrier height of ~0.92 eV. For higher temperatures, dielectric breakdown of the Si_3N_4 and SiRN films occurred before the *E*-field was reached above which Frenkel–Poole conduction dominates. A design graph is given that describes the maximum *E*-field that can be applied over silicon nitride films at high temperatures before electrical breakdown occurs. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3078027]

I. INTRODUCTION

Previously we have reported on silicon flat-membrane microreactors for the study of catalytic partial oxidation of methane into synthesis gas.[1–3] These microreactors comprise a flow channel etched in silicon, capped with a thin composite membrane of 850 nm heavily boron-doped silicon (p^+-Si) covered with 150 nm low stress silicon-rich silicon nitride (SiRN), on which thin metal film heaters and sensors are located. It was observed that at temperatures above 300 °C dielectric breakdown of the SiRN layer occurred at unexpectedly low voltages on the heaters. This breakdown resulted in a short circuit between the p^+-Si layer and the heater pattern, causing a large current through the short-circuit link, which led to a hot spot that damaged the membrane (Fig. 1).[3]

In order to gain more insight into the dielectric breakdown behavior and to be able to optimize the microreactor configuration, we have performed a study on the dielectric behavior of different types of silicon nitride films at temperatures up to 650 °C, which is approximately 400 °C higher than previously reported.[4,5] Our findings are relevant for high-temperature devices, such as silicon-based microreactors[6] or catalytic gas sensors,[7] and high-temperature electronic circuits[8] in which thin films of silicon nitride are or may be used as insulating material.

II. THEORY

Electrical conduction through amorphous dielectrics is dominated by charge traps in the material. Traps are able to bind electrons, and the existence of traps is attributed to material imperfections, such as impurities and crystal defects (bulk traps), or to interfaces between different materials (interface traps). The origins of traps in bulk silicon nitride are dangling bonds, either connected to silicon or to nitrogen.[9–12] The amount of charge traps and their density determine to a large extent the electrical properties of dielectrics: A higher trap density results in a higher electrical conduction through the films.[5,13–15] The amount of traps in stoichiometric silicon nitride highly depends on the deposition method and conditions: Low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or hot wire chemical vapor deposition (HWCVD) each give films with different amounts of traps. Moreover, when the composition of silicon nitride deviates from its stoichiometric composition, the trap density in the film increases.[16] The inclusion of oxygen and/or hydrogen in silicon nitride, either due to impurities in the feed gases or the deposition process itself, also leads to an increase in trap density.[16–18] In general, LPCVD silicon nitride has a significantly lower hydrogen content than HWCVD and PECVD films. Typically, the hydrogen content in LPCVD and HWCVD silicon nitrides is 2–7 at. %, whereas PECVD films contain up to 30 at. % hydrogen.[19–21] The incorporated hydrogen concentration can be decreased by annealing the films at temperatures above the deposition temperature in vacuum or inert-gas ambients.[22]

It has been pointed out by Sze[23] that for sufficiently thick dielectric layers (thickness > 3 nm) on silicon, the current through the dielectric is controlled by the bulk instead of by the electrode interface. For high electrical fields (*E*), conduction through silicon nitride is dominated by the Frenkel–Poole mechanism. Frenkel–Poole conduction indicates that the current density (*J*) is due to field enhanced thermal exci-

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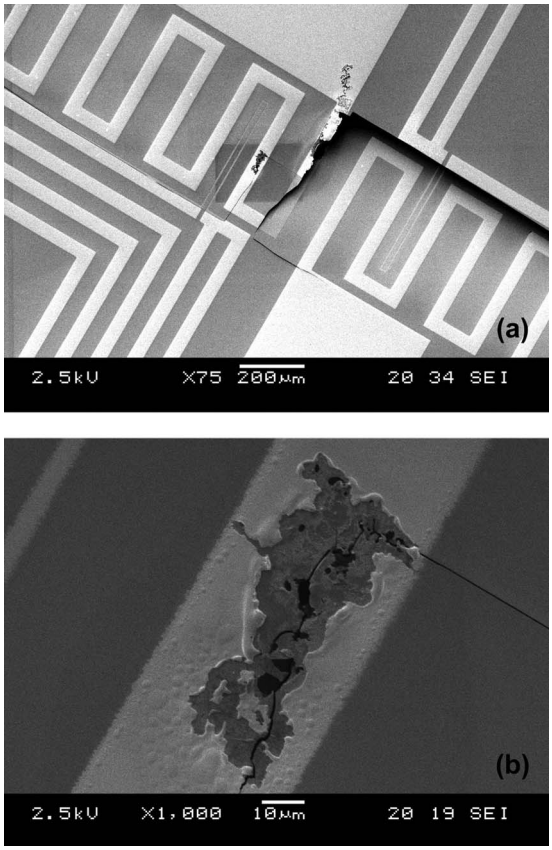

FIG. 1. Pictures of the microreactor membrane after dielectric breakdown of the silicon nitride layer (a) cracks in the membrane; (b) zoom-in on the location where dielectric breakdown and subsequent hot spot formation occurred.

tation of trapped electrons into the conduction band.[23] The relation between J and E for Frenkel–Poole conduction is

$$J = C_1 \times E \exp\frac{-q\left[\phi - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}}\right]}{kT}, \quad (1)$$

in which J is the current density (A/cm^2), C_1 is a pre-exponential factor (among other things a function of the density of trapping centers and the effective carrier mobility), E is the electrical field (V/cm), q is the electric charge ($1.602\,177\,3\times10^{-19}$ C), ϕ is the barrier height of traps (V), ε_0 is the permittivity in vacuum ($8.854\,19\times10^{-14}$ F/cm), ε_r is the relative dielectric constant, k is Boltzmann's constant ($1.380\,66\times10^{-23}$ J/K), and T is the absolute temperature (K). From Eq. (1) it follows that if the current density through silicon nitride is dominated by Frenkel–Poole conduction, a linear relation between $^{10}\log(J/E)$ and $\sqrt{E}$ should be observed.[23,24]

Although Frenkel–Poole transport [Eq. (1)] is generally accepted as the dominant mechanism for enhanced conduction in silicon nitride, there is no consensus on the type of charge carrier responsible for conduction: Where several groups[23,25–27] interpreted their results as electron conduction, other groups reported dominant hole conduction.[28–30] It might be even more complex, since it is also reported that the type of charge carrier depends on the polarity of the electrodes.[31]

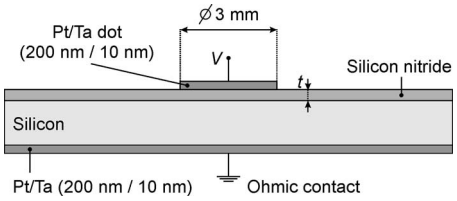

FIG. 2. Cross-sectional view of Pt/Ta–silicon nitride–silicon structure for study on electrical behavior of silicon nitride at elevated temperatures.

III. SAMPLE PREPARATION AND MEASUREMENT SETUPS

On double-side polished p-type silicon (100)-wafers with a resistivity of 5–10 Ω cm (boron concentration $N_A \approx 5\times10^{15}$ cm^{-3}) and on single-side polished n-type silicon (100)-wafers with a resistivity of 12–18 mΩ cm (arsenic concentration $N_D \approx 1\times10^{18}$ cm^{-3}) (diameter of both substrate types 100 mm), two different types of silicon nitride were deposited by a LPCVD process using dichlorosilane (SiH_2Cl_2) and ammonia (NH_3). Stoichiometric silicon nitride (Si_3N_4) was deposited with a SiH_2Cl_2:NH_3 ratio of 1:3 at a pressure of 200 mTorr and a temperature of 800 °C in an Amtech-Tempress Omega Junior reactor, whereas for low stress SiRN a SiH_2Cl_2:NH_3 ratio of 70:18 at 200 mTorr and 850 °C was used in an Amtech-Tempress diffusion system. Prior to silicon nitride deposition, the silicon wafers were immersed in 1% hydrofluoric acid to remove the native oxide. Separate silicon nitride LPCVD runs were performed on eight different substrates, on which the silicon nitride layer thickness was determined by ellipsometry (Plasmos SD 2002, wavelength of 632.8 nm). The thicknesses were 105 and 200 nm for Si_3N_4 and 105 and 215 nm for SiRN on p-Si substrates, and 111 and 221 nm for Si_3N_4 and 108 and 217 nm for SiRN on n^+-Si substrates, respectively.

After removing the silicon nitride from the backside of the wafers, using plasma etching with sulfur hexafluoride (SF_6), metal was deposited by dc magnetron sputtering in an argon ambient. For adhesion purposes, a layer of 10 nm tantalum (Ta) was used underneath a 200 nm platinum (Pt) layer. Deposition was done without breaking the vacuum between the sputter runs. Following the deposition on the backside, Pt/Ta circular dots of 3 mm in diameter were deposited on the silicon nitride using a stainless steel shadow mask. In Fig. 2 a cross-sectional view of the realized metal-insulator-semiconductor structures is given.

Current-voltage characteristics (I,V-characteristics) were measured with three different setups to study the electrical behavior of silicon nitride as a function of temperature. A HP/Agilent 4156C Precision semiconductor parameter analyzer was used together with a Cascade Microtech probe station to verify the conduction mechanisms through silicon nitride at room temperature. For experiments above room temperature two setups were used. One setup involved a home-built hotplate, on which test samples were heated to temperatures up to 400 °C in air. The temperature of the hotplate was measured with a thermocouple, and verified by infrared measurements. In the second setup, a furnace (Toma TSD12) was used for measurements at temperatures in the range 400–650 °C in air. The temperature ramp was

10 °C/min, and prior to each electrical measurement the temperature of the sample was stabilized for 15 min. In both setups, the applied voltage, the current through the silicon nitride, and the temperature of the hotplate or furnace were measured and controlled by a PC using a GPIB connection to a sourcemeter (Keithley 2410) and software in Agilent Vee Pro. Probe needles (Micro-manipulator Inc., type B205189–7B) were used to obtain electrical contacts with the Pt/Ta dots on the front side of the wafer, whereas the backside of the wafer was contacted by probing a needle onto the front side of a second wafer (with a blanket 200/10 nm Pt/Ta film) that was positioned underneath the substrate with the Pt/Ta dots with an overlapping area of ~95%. During experiments with the hotplate, the wafer was illuminated with a halogen lamp prior to each measurement in order to avoid current saturation due to limited carrier generation in the depletion layer in the silicon underneath the dot. Without the photogenerated carriers, current saturation effects in I,V-curves, due to lack of minority-charge carriers, influenced the measurements at temperatures below 50 °C.

First, I,V-measurements were performed on 105 nm SiRN and Si_3N_4 (on p-Si) with the HP/Agilent system. The voltage was swept from 0 to +100 V, followed by a sweep from 0 to −100 V. In a second set of experiments the voltages at which electrical breakdown occurs were determined for the silicon nitride layers (on p-Si and n^+-Si) for a wide range of temperatures, using the hotplate setup and the furnace setup. The breakdown voltage (V_{BD}) is defined as the voltage where the dielectric material becomes conductive, i.e., at this voltage silicon nitride loses its electrical insulating property and a large current flows through the dielectric. The voltage was increased stepwise (steps of 0.1 V) from 0 V until the voltage where dielectric breakdown was measured (a positive voltage was applied to a dot on the front side of the wafer, while the backside was grounded, Fig. 2). At each temperature these measurements were done three to five times (p-Si substrates) or two to three times (n^+-Si substrates) for each silicon nitride layer, and all measurements were performed on unused (virgin) Pt/Ta dots. In case of the hotplate setup no substrate cooling-down was necessary before relocating the probe needle onto a new Pt/Ta dot, whereas in case of the furnace setup cooling-down of the substrate to 50 °C was required prior to probe needle relocation.

Subsequently, for a series of temperatures, I,V-characteristics were recorded on silicon nitride films on p-Si wafers: The voltage was increased from 0 V to V_{final} and back to 0 V, where the maximum voltage V_{final} was set just below the breakdown voltage V_{BD}. After recording the I,V-curves, these Pt/Ta dots were used again to determine the breakdown voltage at various temperatures; however, no differences in V_{BD} were found with respect to the first series of breakdown experiments.

IV. EXPERIMENTAL RESULTS

Figure 3(a) shows typical $^{10}\log J,E$-characteristics (J is the current I divided by the dot area and E is the applied voltage V divided by the thickness of the silicon nitride layer) for 105 nm SiRN and 105 nm Si_3N_4 on p-Si substrates: These curves are reproducible on other Pt/Ta dots on these silicon nitride layers. Similar J,E-characteristics were observed for 200 nm Si_3N_4 and 215 nm SiRN layers. In case of Si_3N_4 for low E-fields (absolute values below ~2.0 MV/cm) a linear relation can be observed between J and E. Furthermore, for high E-fields (absolute values above ~4.7 MV/cm), the relation between $^{10}\log J$ and E is linear. This is in accordance with the observation of Sze and co-worker[23,24] that at room temperature two conduction regions can be distinguished for Si_3N_4: Ohmic conduction at low voltages (also known as hopping; $J\sim E$), and Frenkel–Poole conduction at high voltages [$J\sim\exp(E)$]. The observed E-field values below/above which the dominating

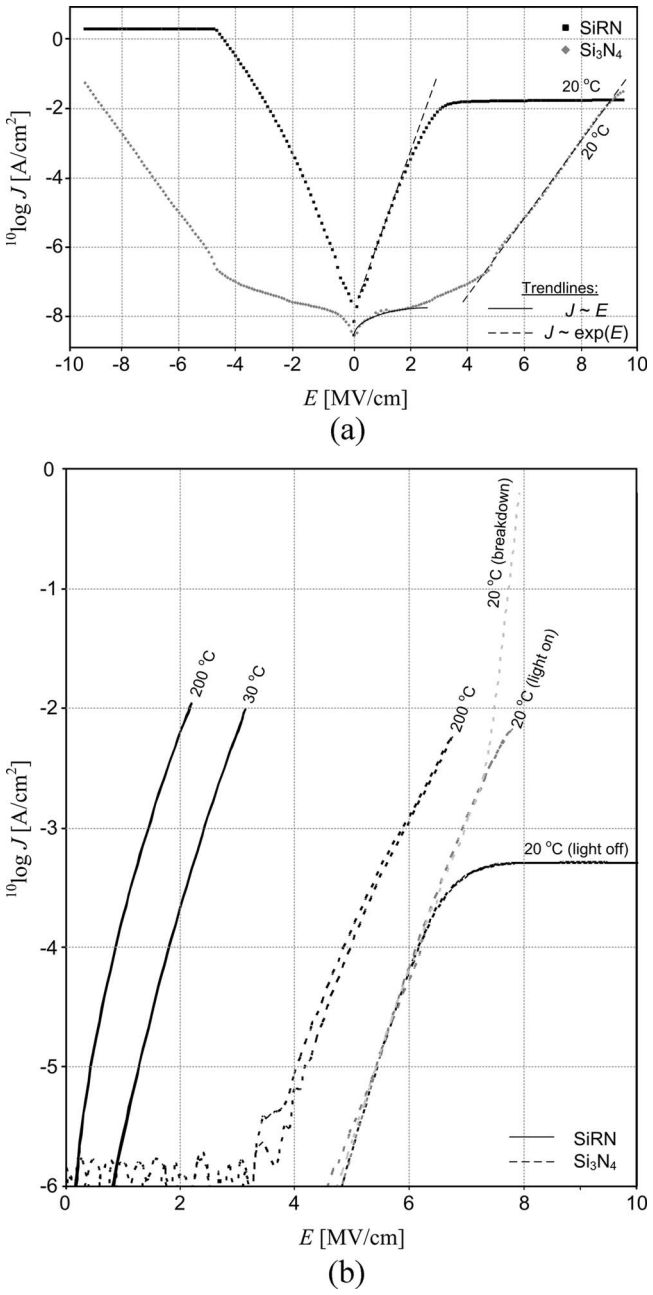

FIG. 3. $^{10}\log J,E$-characteristics measured on 105 nm Si_3N_4 and 105 nm SiRN on p-type silicon at room temperature (a) and for temperatures up to 200 °C (b).

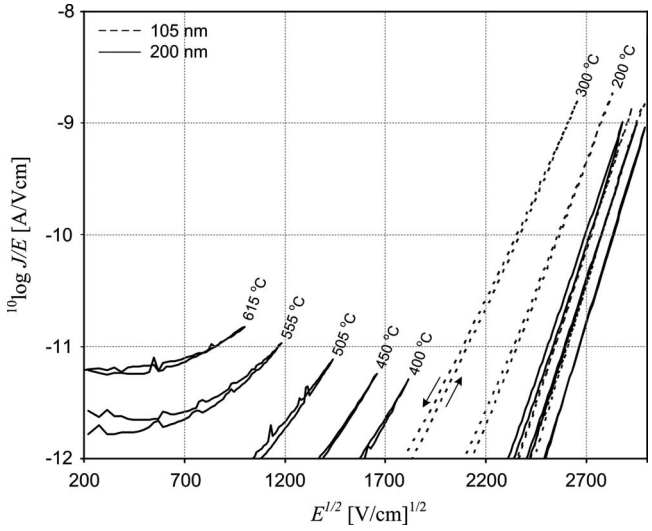

FIG. 4. $^{10}\log(J/E)$ vs $\sqrt{E}$ characteristics of 105 (up to 300 °C) and 200 nm (up to 615 °C) Si_3N_4 on *p*-type silicon. The arrows indicate the voltage sweep direction (equal for all curves). The curves without temperature labels (at the right-hand side of the graph) are measured at 50 and 100 °C (105 nm), and 20, 75, and 180 °C (200 nm), respectively.

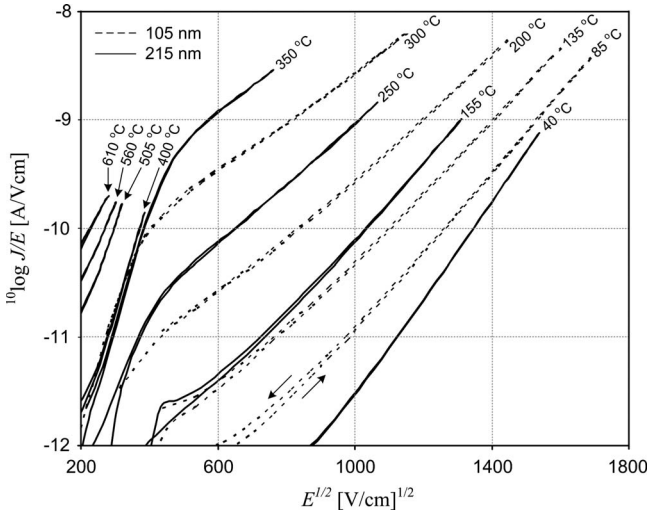

FIG. 5. $^{10}\log(J/E)$ vs $\sqrt{E}$ characteristics of 105 (up to 300 °C) and 215 nm (up to 610 °C) SiRN on *p*-type silicon. The arrows indicate the voltage sweep direction (equal for all curves).

conduction mechanism through Si_3N_4 is hopping ($E_{hopping}$) or Frenkel–Poole transport (E_{FP}) are within 7% of the values found by Sze and co-worker[23,24] (~1.9 and ~4.7 MV/cm, respectively). For SiRN the *E*-fields below/above which hopping or Frenkel–Poole conduction prevails are significantly lower: $E_{hopping}$ cannot be estimated reliably from Fig. 3(a), and E_{FP} is ~0.3 MV/cm. The saturation levels for $^{10}\log J$ for high *E*-fields are due to (i) a maximum level of the current for large *E*-fields (the compliance was set to 1 mA) and (ii) lack of minority-charge carriers (for positive *E*-fields only).

In Fig. 3(b) $^{10}\log J,E$-characteristics are shown obtained from 105 nm SiRN and 105 nm Si_3N_4 (*p*-Si substrates) with the hotplate setup. E_{FP} cannot be observed due to the lower signal-to-noise ratio of the hotplate setup. Furthermore, it can be observed that conduction through silicon nitride increases with temperature, and that for temperatures up to 50 °C current saturation at high *E*-fields due to a lack of charge carriers can be avoided by illumination of the substrate during I,V-recordings. Finally, an I,V-curve is shown for a room temperature experiment during which the *E*-field was increased until breakdown of the silicon nitride: This curve overlaps with other I,V-curves at 20 °C up to ~7,3 MV/cm, but above this *E*-field the current increased very rapidly, indicating electrical breakdown.

In order to gain a better understanding of the conduction through silicon nitride layers on *p*-Si substrates for high *E*-fields, the I,V-curves measured above room temperature are plotted as $^{10}\log(J/E)$ versus $\sqrt{E}$ in Figs. 4 and 5. Note that in these plots $^{10}\log(J/E)$-values below −12 were extremely noisy and therefore omitted.

A. Stoichiometric silicon nitride (Si_3N_4)

In Fig. 4 the $^{10}\log(J/E)$ versus $\sqrt{E}$ characteristics for 105 nm Si_3N_4 and 200 nm Si_3N_4 are shown up to 615 °C. Curves for different Si_3N_4 layer thicknesses measured at the same temperature fully overlap. For temperatures above ~150 °C a little hysteresis is observed, which may be the result of probing stress induced trap generation.[32] For temperatures up to 500 °C (nearly) straight lines can be fitted through the curves, which implies that Frenkel–Poole transport is the dominating conduction mechanism through Si_3N_4 up to 500 °C. It cannot be concluded that for temperatures above 500 °C the conduction is Frenkel–Poole transport (no straight fitting lines through data) since dielectric breakdown occurred before E_{FP} was reached.

B. Low stress silicon-rich silicon nitride (SiRN)

In Fig. 5 the $^{10}\log(J/E)$ versus $\sqrt{E}$ characteristics for 105 nm SiRN (a) and 215 nm SiRN (b) are shown up to 610 °C. For the investigated temperature range, the curves for 215 nm SiRN are consistently steeper than the curves for 105 nm SiRN. Up to 200 °C most curves are straight, which indicates that the Frenkel–Poole conduction mechanism is dominating in this temperature range. For temperatures in the range 200–350 °C two slopes occur in the $^{10}\log(J/E)$ versus $\sqrt{E}$ curves: Straight lines can be fitted through the curves for $E>0.3$ MV/cm (i.e., the part of the curves with the lowest slope); thus above this *E*-field Frenkel–Poole emission is the dominating transport mechanism. For temperatures above 350 °C the *E*-field above which Frenkel–Poole transport dominates is not reached due to (early) dielectric breakdown of the SiRN film.

C. Electrical breakdown of Si_3N_4 and SiRN

The electrical field E_{BD} at which breakdown was observed for Si_3N_4 and SiRN is shown in Fig. 6 as a function of the temperature. For Si_3N_4 and SiRN on *p*-Si substrates, E_{BD} decreases linearly with the temperature up to ~300 °C, whereas above 300 °C the relation between E_{BD} and *T* follows a quadratic decay. In contrast, for Si_3N_4 and SiRN on n^+-Si substrates, the quadratic decay of E_{BD} starts at room temperature. The quadratic decay ($E_{BD}\sim 1/T^2$) seems to be a similar trend as reported by Sze and co-worker,[23,24] who ob-

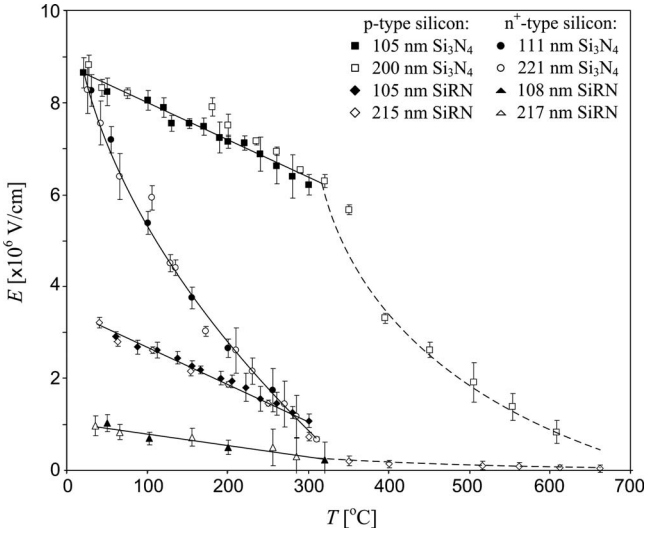

FIG. 6. Electrical breakdown field E_{BD} as a function of temperature T up to 650 °C for Si_3N_4 and SiRN films deposited on p-Si and n^+-Si substrates.

served a linear relation between the square root of the maximum dielectric strength and the temperature ($\sqrt{E_{BD}} \sim 1/T$) for Si_3N_4 deposited on p-Si substrates. However, the onset of the quadratic decay for the layers of Sze and co-worker[23,24] is ~0 °C, whereas it is ~300 °C for p-type Si substrates in this work. Based on the data of E_{BD} as a function of the temperature T, conduction through silicon nitride films appears to be limited by electrons. Figure 6 can be used as a guideline to avoid electrical breakdown of silicon nitride on different silicon substrates: From E_{BD} the maximum supply voltage and/or temperature that can be applied to thin films of silicon nitride can be estimated.

V. DISCUSSION

From the $^{10}\log(J/E) - \sqrt{E}$ characteristics in Figs. 4 and 5 it followed that, at least for temperatures up to 500 or 350 °C, conduction through Si_3N_4 and SiRN can be described well by the Frenkel–Poole relation [Eq. (1)]. Values of the pre-exponential factor C_1 can be estimated by plotting $^{10}\log J$ as a function of $1/T$ for a constant E-field at conditions where Frenkel–Poole transport dominates: From such a plot the linear region of the data can be used to determine C_1. E-fields of ~6.7 and ~1.0 MV/cm were used to extract C_1 for Si_3N_4 and SiRN films, respectively, for temperatures in the range 20–300 °C. It is noted that for all silicon nitride films I,V-characteristics were recorded at significantly more temperatures than shown in Figs. 4 and 5; see Ref. 33. The extracted values for C_1 are shown in Table I. Figures 4 and 5 in combination with the extracted values for C_1 can be used to estimate the barrier height ϕ. For both types of silicon nitride good fits were found for barrier heights given in Table I (ε_r values in Si_3N_4 and SiRN were determined with ellipsometry, and were 4.03 and 4.75, respectively).

The values for C_1 for Si_3N_4 are close to $(1.44 \pm 0.08) \times 10^{-7}$ A/V cm reported in literature,[5] and the barrier height of ~1.1 eV Si_3N_4 also agrees well with literature.[5,23] Both C_1 and ϕ appear to be independent of the layer thickness. For SiRN the C_1 values are higher than the reported value of $(1.81 \pm 0.15) \times 10^{-6}$ A/V cm for $SiN_{1.22}$, which is due to a lower silicon content in our SiRN films (Si:N=4:5 for our films). Furthermore, slightly different values for ϕ are found for both SiRN thicknesses. This is consistent with the observation in Fig. 5 of two different slopes for the E-field range where Frenkel–Poole conduction dominates. Probably the barrier height for both silicon nitride types decreases slightly with increasing temperatures (Table I). In general, nonstoichiometric silicon nitride has a higher C_1 value and a lower barrier height than stoichiometric silicon nitride due to its increased silicon content.

The values for C_1 and ϕ shown in Table I yield reasonable fittings with measurements for temperatures above 300 °C: for Si_3N_4 up to ~500 °C, and for SiRN up to ~350 °C. This confirms our statements that Frenkel–Poole transport is the dominant conduction mechanism through silicon nitride up to these temperatures. At higher temperatures, i.e., $T > \sim 500$ °C (Si_3N_4) or ~350 °C (SiRN), electrical breakdown of the silicon nitride films occurs prior to reaching the E-field above which Frenkel–Poole transport is the dominant conduction mechanism.

VI. CONCLUSIONS

In this work the conduction through LPCVD silicon nitride thin films at elevated temperatures is studied. J,E-characteristics of Si_3N_4 and SiRN are measured for temperatures up to 650 °C. Based on the obtained data, it is found that Frenkel–Poole conduction is the dominating conduction mechanism for high E-fields and temperature up to 500 °C (Si_3N_4) or 350 °C (SiRN), with barrier heights of ~1.10 and 0.92 eV, respectively. Furthermore, a design

TABLE I. Values of the parameters' pre-exponential factor C_1 and the barrier height ϕ describing Frenkel–Poole conduction through two types of silicon nitride for various layer thicknesses and temperatures.

Silicon nitride data			Barrier height ϕ (eV)					
Type	Thickness (nm)	C_1 (A/V cm)	20 °C	50 °C	100 °C	200 °C	300 °C	Error (eV)
Si_3N_4	105	$(1.37 \pm 0.04) \times 10^{-7}$	1.11	1.10	1.08	1.10	1.07	<0.02
	200	$(1.35 \pm 0.03) \times 10^{-7}$	1.10	1.10	1.08	1.09	1.06	
SiRN	105	$(5.36 \pm 0.21) \times 10^{-6}$	0.97	0.95	0.90	0.92	0.91	<0.07
	215	$(5.43 \pm 0.18) \times 10^{-6}$	0.93	0.91	0.91	0.89	0.89	

graph is given, which can be used to avoid electrical breakdown of thin films of Si_3N_4 and SiRN up to 650 °C.

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