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Fabrication of integrated porous glass for microfluidic applications†

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This paper presents a method for the fabrication of integrated porous silica layers in microfluidic channel networks by microfabrication techniques. Porous silica is obtained by anodization of silicon, followed by full conversion of the porous silicon network into porous silica by means of thermal oxidation. A series of experiments were performed with various channel layouts to determine the critical parameters, including the *I–V* characteristics and the optimal working potential for stable pore formation, during anodic etching. Typical test structures were anodized in 5% HF for 15 min at 1 V, yielding an average pore size of around 5.4 nm and porosity of 49%. Complete conversion of porous silicon into porous glass was accomplished with wet oxidation at 900 °C. The average pore size and porosity of porous glass network were around 3.8 nm and 34%, respectively. This decrease in both pore size and porosity is caused by the increase in molar volume when silicon oxidizes to silicon oxide. The transparency and the hydrophilicity of porous glass layers are evidenced by means of monitoring the diffusion of Rhodamine B fluorescent dye through the porous network. This fabrication method can be applied to (3-D) structured microfluidic channels and it is envisioned that the resulting porous silica layers can be employed for a wide range of application areas, such as membrane technology, catalyst supports, chromatography and electrokinetics.

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1 Introduction

Due to its ability to influence the absorbance/desorbance of species, porous silica and porous glass have broad areas of application since the late 1960s, for example as ion selective membranes,[1,2] electrophoretic and gas chromatographic separations,[3–5] or as a salt bridge.[6] Taking into account the modern trends of miniaturization and development of lab-on-a-chip devices, the integration of porous silica in microfluidic chips is of great interest because this opens the path to new applications and improvements in existing techniques. The ability to increase the total surface area by up to 6–7 orders of magnitude within a very small length scale (10^{-3}–10^{-6} m), or creating a confined space, or a porous network with a size ranging from nanometers to micrometers, have initiated the use of porous silicas for many other applications.

The fabrication (enabling) of porous silica inside the channels of microfluidic systems is mostly performed as a post-step after chip fabrication (a post-treatment to the inner walls of microchannels) by thermal/chemical treatments, such as forming monoliths (or layers) by sol–gel or hydrogel methods. Detobel *et al.* utilized a sol–gel method for coating the inner walls of the microchannels with porous silica and showed its potential for liquid chromatography (LC) applications.[7] As also partly reported there, obtaining a uniform distribution in pore size, porosity and layer thicknesses over the coated structures, avoidance of crack formation due to the contraction/expansion effects during thermal treatments, the realization of porous silica layers with a thickness more than a few microns (without cracking), and selective film formation (*e.g.* coating only the separation channel of a chromatography chip) are challenges that still remain for such chemical techniques. As an alternative, Kutter and co-workers published a method for the on-chip fabrication of porous glass (PG) by means of oxidizing Si needles (micrograss) obtained by a reactive ion etching method yielding so-called ''black silicon'', and used it for electrokinetic applications.[8] Although it was possible to fabricate porous channels with this method, it did not provide a regular network of pores and it was not possible to apply this technique to structured microchannels. Phase separation techniques have also been used to create porous glass.[9] However, they are limited to only the possibility of creating monoliths (not layers) and the resulting porous network is alkali borosilicate glass, which exhibits substantially different material properties than silica.

In this work we describe the realization of integrated stable porous silica (hereafter called PG) structures in microfluidic channels (3-D structures) based on the full oxidation of porous silicon (PS) layers in a well-controlled and highly reproducible

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manner. Although various methods to oxidize PS have been reported, as well as analysis methods and properties of the remaining porous silica,[10–12] until now only the integration on 2-D planar surfaces have been reported.[13,14]

The fabrication of integrated PG consists of two main steps: 1. fabrication of PS *via* anodization; 2. conversion of PS into PG *via* thermal oxidation. Although the novelty of the proposed technique is in the second step–obtaining uniform, stable and crack-free porous networks with tunable properties–the initial pore size, porosity and layer thickness were determined in the first step. Therefore, fabrication of PS and the parameters which affect the layer formation over the structured (3-D) microchannels need to be discussed first.

The possibility of its fabrication directly from Si, which is the main substrate material for microfabrication, made PS applicable into various research disciplines. It was firstly used for optical purposes in microelectronics,[15,16] later its application area became wider, such as in mechanical sensors,[17–23] thermal insulation layers,[24–27] and chemical applications.[28–32] Our group previously reported the integration of the PS layers in ordered pillar arrays for liquid chromatography[33] and a characterization study afterwards.[34]

PS is obtained by anodic etching of single crystalline silicon (Si) in hydrofluoric acid solution (HF) at room temperature. Pore formation starts at the surface, which is exposed to the HF solution and the pores penetrate commonly, with branching, into the Si substrate following the electric field lines created by the anodic polarization. A number of studies were reported on the formation of PS and the parameters affecting the pore size, porosity and layer formation rate.[35–40] It was shown that increasing the HF concentration causes a decrease in the pore size and the porosity, while resulting in a higher layer thickness formation rate. Increasing the applied current density increases the pore size, porosity and layer formation rate, but there is a certain upper limit, above which electropolishing starts. This limit was determined by voltammetry curves, which allows the possibility to determine the working range for a stable pore formation avoiding electropolishing. However, all these characterization studies, including the ones from our group, were performed on planar surfaces with non-processed wafers. Although partial masking of the wafer surface was reported,[41,42] the effect of loading, which is defined as the ratio of the total exposed (unmasked) area to the total planar surface area of the wafer, was disregarded. In our study, this effect is discussed as a critical parameter for the fabrication of PS over (3-D) structured microchannels.

PS is a semiconductor and hydrophobic material which exhibits variable optical properties depending on its process conditions.[16,43–45] By converting the PS layer into PG, which is a hydrophilic and optically transparent dielectric, it is aimed to extend the application areas of such fabrication methodology. The focus is on the fabrication and the integration of porous glass layers into microstructures: the effect of loading on the formation of PS will be addressed, as well as the conversion of PS into PG by means of thermal oxidation. Moreover, the properties of PG, *i.e.* pore size, porosity, optical transparency and wettability, were studied.

2 Experimental

2.1 Fabrication

Test structures were designed for the step-by-step optimization of the parameters of the fabrication process for conversion of PS into PG before realization of the microchips. As a first step, 150–175 nm thick silicon-rich silicon nitride (SiRN) was deposited by low pressure chemical vapor deposition (LPCVD) on 100 mm diameter and 500 μm thick, highly doped p-type silicon (p++ Si) wafers with (100) orientation and resistivity of 0.010–0.025 Ω cm. Next, the pattern of the structures was transferred into the SiRN layer *via* standard UV-photolithography and reactive ion etching (RIE). Subsequently, 10 μm deep channels were etched with RIE or deep RIE, followed by the removal of the SiRN layer from the backside of the wafers by RIE. After this, the samples were ready for anodization and oxidation, which will be discussed in the following sections. In between these two steps, a thick photoresist film (Ordyl BF410) was laminated on the back side of the wafers and patterned with UV-photolithography. The film served as a mask for through etching of the wafers to open the access holes for the fluidic connections, *via* powder blasting (with 29 μm alumina particles), using an in-house built setup. After powder blasting, the wafers were first washed with DI-water and then immersed in acetone and isopropanol, respectively, followed by thermal oxidation. Finally, the processed wafers were bonded anodically with bare glass (Borofloat) wafers and the stacks were diced into individual microchips (Fig. 1).

2.2 Anodization and oxidation

PS was formed by electrochemical etching of the p++ Si wafer in a single-cell Teflon reservoir. The front (polished) side of the wafer was exposed to aqueous hydrogen fluoride solution, while the back side was in contact with a copper electrode (anode). The counter electrode (cathode), a platinum (Pt) coated perforated silicon plate connected to a Pt wire, was immersed in the electrolyte in order to complete the circuit. A Keithley (Model 2410) high voltage source-measurement unit was used to apply a potential to the anode while the cathode was grounded. Details of the anodization set-up can be found in the ESI†. Oxidation of the obtained PS network to PG was done by means of dry and/or wet oxidation with various temperatures and times.

An important mechanism reported in literature is hydrogen gas evolution during the pore formation process.[38] This phenomenon and its detrimental impact on the uniformity of the porous layer was observed during the experiments. Hydrogen bubbles formed during the pore formation stick to the surface to be anodized and create locally isolated regions, thus preventing pore formation. Such non-uniformity was visible to the bare eye as a color change for layers even a few microns thick. In order to avoid the bubbles sticking, the wettability of the surface was enhanced by adding ethanol to

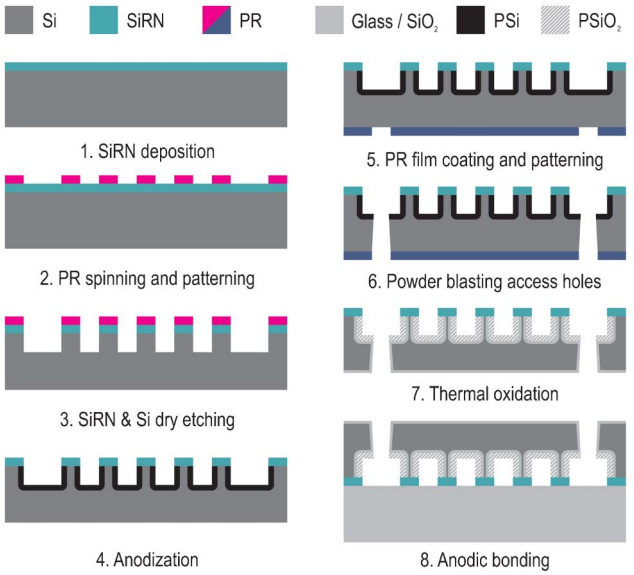

Fig. 1 Fabrication process flow for microchip fabrication with integrated porous glass layers.

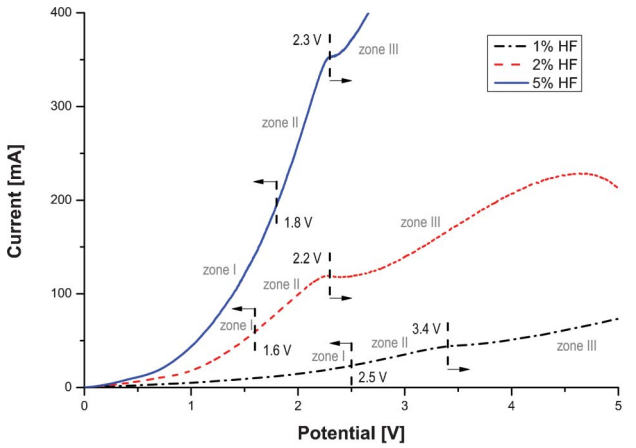

Fig. 2 *I–V* curves for micromachined structures with 30% loading on p++ Si for 1%, 2% and 5% HF solutions. The potentials were swept with 5 mV increments and 20 ms step time.

the HF solution. A volumetric ratio of 5 : 1 HF : ethanol was selected as a suitable compromise between avoiding non-uniformities and excessive dilution of the HF solution.

3 Results and discussion

3.1 Anodization

The test structures fabricated for the anodization/oxidation experiments were pillars with different geometrical shapes placed as regular arrays inside 10 μm deep, straight and open microchannels. As seen in step 4 of Fig. 1, a SiRN layer was used as a mask for the anodization process, hence only the sidewalls of the pillars and the bottom and sidewalls of the microchannels were anodized. In order to have integrated porous layers within individual microchips, masking is needed in order to selectively anodize the targeted areas, which are only the inner surfaces of the microchannels. Fig. ESI-2† explains how a porous bridge can be formed between individual microchannels without a masking layer during anodization. Since the goal was to find the optimal process parameters for stable pore formation on (3-D) structured microchannels, various test structures were designed for different loading conditions. Loading was defined as the ratio of the total surface area of the selected design to the total planar surface area of non-processed wafer, which were exposed to anodization.

For the first alternative, the total surface area exposed to the HF solution was around 10 cm^2, which resulted in a 30% loading with respect to the total planar surface area of a non-processed 100 mm wafer (34 cm^2). Fig. 2 represents the current *vs.* potential characteristics (voltammograms) of 30% loading test structures for different concentrations of HF. The obtained plots can be divided into three regions. First, they start with an exponential growth (zone I) of the current as a function of the applied potential, which represents uniformly distributed and stable pore formation. Then the voltammogram shows a linear trend in the transition phase (zone II), where pores are still created but the process becomes unstable and non-uniformities in the PS structure are observed. After passing the current peak, electropolishing starts (zone III). As seen in Fig. 2, increasing the HF concentration yields higher anodic currents. As the *I–V* curve characteristics and the effect of the HF concentration were already investigated and experimentally verified in the literature,[35] it is not discussed further in this work.

To study the effect of loading on the current *vs.* potential relationship, in addition to the 30% loading case, open microchannels with the same depth but containing pillars with smaller dimensions were fabricated for having 5% loading. As a planar alternative without etched channels, 2% loading was obtained by only masking the surface of the Si wafer with etched windows in a SiRN layer (*i.e.* no DRIE of Si). A non-processed Si wafer was also included in the study as a reference for 100% loading.

Fig. 3 shows the anodic current density (current per unit exposed area) *vs.* potential plots for different levels of loading for both planar surfaces and etched microchannels. Increasing the loading causes a decrease in the current density obtained and polishing occurs at lower potentials. However, the span of the potential in the safe zone for stable pore formation (zone I; the logarithmic region) gets larger. Therefore, designs with low loadings should be avoided as it would be difficult to determine the applicable potential for the desired pore size and porosity because of the limited working range. Moreover, applying higher anodic currents increases the rate of evolution of the hydrogen bubbles, which would cause stability and uniformity issues as discussed earlier.

Based on the data presented in Fig. 2, 1 V was selected as the anodization potential for the test structures with 30% loading. A 2 μm thick PS layer was obtained after 15 min anodization in 50 : 10 ml 5% HF : ethanol solution. In Fig. 4(a), the microscope image shows the distribution of the PS layer

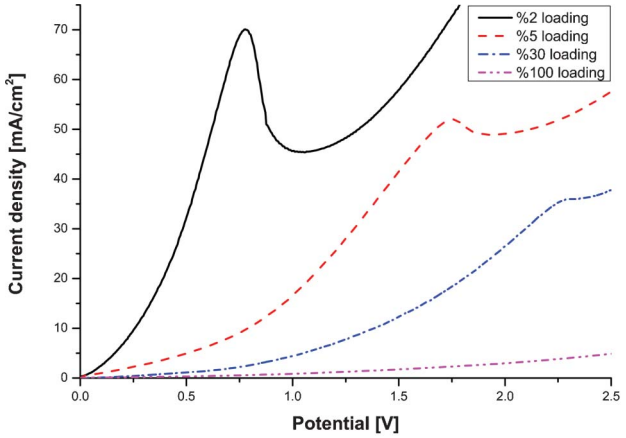

Fig. 3 *J–V* curves for micromachined structures for different loadings for 5% HF solution. The potentials were swept with 5 mV increments and 20 ms step time.

around the pillars, which are 100 μm long and 20 μm wide with a depth of 10 μm. By selecting the applied potential within the safe range (the transition regime started around 1.8 V after the first logarithmic growth region), the obtained layer thickness distribution was uniform. Fig. 4(b) shows the high resolution SEM (HR-SEM) image of the cross section of a pillar in the (cleaved) center of the wafer. The uniformity was also preserved across the height of the structures.

Since the PS layer formation rate is constant during anodization, the resulting layer thickness is linearly proportional to the anodization time. Therefore, it is possible to fabricate thicker layers and even fully porous pillars. However, the growth direction of the pores is coincident with the electric field lines through the Si wafer. After the initial pore formation on the surface, propagation with branching proceeds in a direction perpendicular to the surface. As a result, the faces parallel to the bottom electrode plate (*i.e.* the bottom of microchannels) are exposed to straight, hence stronger field lines compared to the side faces (*i.e.* sidewalls of pillars and microchannels). To investigate the possibility of having fully porous pillars and the differences in formation rates between the side and bottom surfaces, a 5% loading design was anodized in 5% HF solution without an etch mask (the SiRN layer was removed before anodization), yielding a total surface area of around 35 cm^2. The anodization current was set to 200 mA for 15 min, which was enough to convert the 10 μm thick pillars into fully porous structures. Indeed, for these settings fully porous pillars were found (see Fig. ESI-3†). Moreover, slight differences between PS formation rates between parallel and perpendicular surfaces were confirmed. The resulting thickness of the PS layer was 5.7 μm on the sidewalls, whilst it was 6.7 μm at the bottom of the channel and 6.9 μm in the bulk region as flat surfaces (Fig. ESI-3†). Pore size and the porosity were determined by processing a series of HR-SEM images of surfaces and cross-sections using ImageJ software. The average pore size and the porosity were calculated to be 5.2 nm and 53%, respectively. This data is in good agreement with PS data obtained by means of BET-adsorption/desorption experiments (for similar anodization conditions on planar, non-processed p++ Si wafer).[34] Therefore it was decided to use HR-SEM for determining the pore size and porosity as a quick and easy method for further experiments.

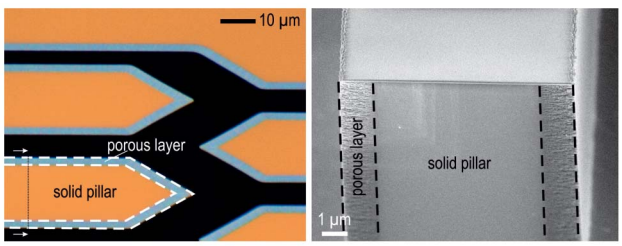

Fig. 4 PS layer formed after 15 min. at 1 V in 5% HF. Microscope image of the hexagonal shape pillar (a). HR-SEM image of the cross section at the center of the wafer (b). The layer thickness is 2 μm.

3.2 Oxidation

Porous glass (PG) was obtained by fully oxidizing the PS skeleton *via* thermal oxidation. This is a diffusion driven process for bulk Si and yields a 2.27 unit thickness of oxide layer per unit thickness of Si consumed. However, it was shown previously that the oxidation of the PS network is driven by surface reactions instead of diffusion,[46] because freshly fabricated PS is highly reactive. In order to compare the mechanisms of the conversion processes, both dry and wet oxidation were investigated.

The most critical parameter for oxidation is the process temperature. For bulk Si processing, usually temperatures of at least 1050 °C and above are preferred in order to increase the purity of produced silica.[47] Therefore the samples (shown in Fig. ESI-3†) were oxidized for full conversion of PS to PG at 1050 °C both in dry and wet environments for 80 and 15 min, respectively for the aimed oxide thickness of 150 nm (note that this value is estimated from known data for oxidation of solid, non-porous silicon), which was assumed to be larger than the thickest structure formed in the PS skeleton. Fig. 5 shows the HR-SEM pictures of cross-sections of cleaved structures after oxidation. The porous structure was preserved after dry

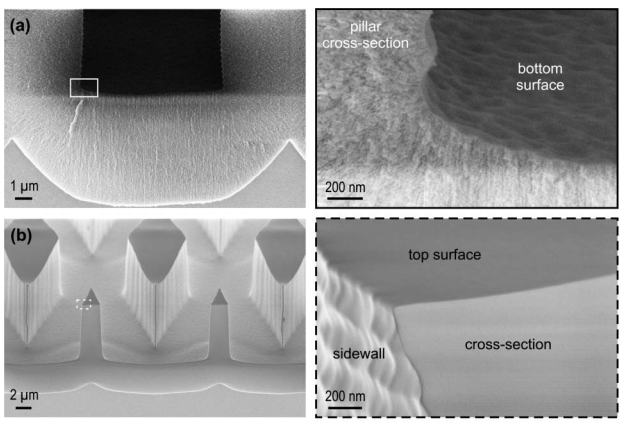

Fig. 5 Dry (a) and wet (b) oxidation of PS (the sample shown in Fig. ESI-3†) at 1050 °C.

oxidation. Charging was observed at the interface of the PG/Si during the SEM imaging, which proves the existence of a dielectric layer. The measured thickness of this layer was 80–100 nm. This finding supports the assumption of a surface reaction driven oxidation of the PS network followed by a diffusion driven oxidation reaction through the bulk Si layer underneath.

In contrast, wet oxidation of PS resulted in complete closure of the pores, but a similar dielectric layer was observed at the PG/Si interface (which can only be a silica layer in this case). Closure of the pores can be considered as an indication to an increase in wall thickness of the PS skeleton, which indicates the occurrence of the diffusion driven oxidation, in contrast to the surface reaction driven process which is found for dry oxidation. The smoothness of the surface of the cross section of the structures in Fig. 5(b), which were porous prior to the oxidation, reflects another important mechanism during high temperature heat treatments: the viscous flow of silica, which takes place at the temperatures higher than 950–1000 °C.[48] Therefore, oxidation within the viscous flow range, which may cause complete closure of the pores, should be avoided.

Preserving the porous structure with dry oxidation, whilst having complete closure of pores with wet oxidation at the same temperature, is interpreted as that the oxidation process starts with surface reactions because of the highly reactive nature of the porous silicon structure, but then continues as a diffusion driven process for longer oxidation times. This proposition is in agreement with the fact that the oxidation continues at bulk Si underneath the PG layer after complete conversion of PS.

Evaluating the use of dry oxidation for obtaining PG, the focus was given to wet oxidation for expanding the possibilities regarding electrokinetic applications, which require fluidic channels with an electrical isolation layer thick enough to withstand high potentials. Please note that PS formation and subsequent oxidation can serve as an alternative to oxidation of solid crystalline Si, especially for thick insulation layers. However, the insulation layer mentioned here is the dielectric layer that is needed to insulate the Si substrate from the electric field created through the ionic liquid in the microchannels by means of the applied electric potentials. Thus, the critical points concerning the application and realization of the Si-based microchips with either integrated PG or solid silica layers in their interior have to be taken into account. The first parameters to be investigated are pore size and porosity, which are reduced due to oxidation. It was stated earlier that the dependency of the pore size, porosity and porous layer growth rate on the concentration of HF solution and/or the applied electric potential differs for every design and an individual optimization study has to be performed to find the proper parameters for the needs of the application. Such relationship was determined for the test structures, whose *I–V* relationships are shown in Fig. 3, to give an insight to the reader about the mechanisms of the process steps. Depending on the chosen application of chips, PS can be converted into PG or solid silica.

In order to avoid closure of the pores due to the viscous flow of silica, the optimum temperature was set to 900 °C for wet oxidation of the PS network. Fig. 6 shows close-up HR-SEM pictures of the porous network (same structures as shown in Fig. 4) before and after complete conversion of PS into PG. Since it was not possible to obtain reliable data with BET measurements for such small sample volumes,[33] as well as the reasoning given in section 3.1, the mean pore size and porosity estimations were performed by analyzing the HR-SEM images. The calculated porosities for PS and PG were around 49% and 34%, while the average pores sizes were around 5.4 nm and 3.8 nm, respectively. Thus the oxidation process resulted in around 31% decrease in porosity and 29% decrease in the pore size.

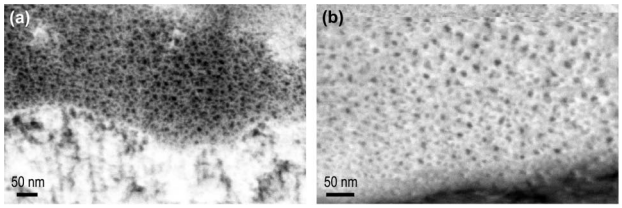

Fig. 6 HR-SEM pictures of PS before (a) and PG after (b) oxidation (at 900 °C). Porosity: 49%, pore size: 5.4 nm for PS. Porosity: 34%, pore size: 3.8 nm for PG. Note: The uniform portions of above images as well as the other images (not shown) were used for processing.

The reduction in the pore size and porosity is directly dependent on the initial state. Shrinkage of pore size means expansion of the Si skeleton wall, which is defined by the initial wall thickness. The applied potentials and currents for anodization experiments were selected for obtaining an average pore size of around 5 nm. HR-SEM analyses showed that the maximum thickness of the walls of the PS skeleton were around 100 nm. However, only 7% of the counted pores were in the range of 5 nm and the size distribution was between 2 to 30 nm. This indicates that the local reduction in pore size and porosity after oxidation depends on the PS morphology. Since the anodization was performed on 3-D structures, the initial state of a pore (hence the shrinkage after oxidation) also depends its location, as the intensity of the electric field lines created during the anodization process changes with the morphology.

This maximum wall thickness of around 100 nm, *i.e.* one hour of wet oxidation at 900 °C would be sufficient for full conversion of PS into PG. However, significantly longer oxidation times were required to generate a thick insulation layer to avoid electrical breakdown during application of high voltages for electrokinetic applications. For this purpose, a set of 30% loading test structures was fabricated (etched *via* DRIE for 10 μm channel depth) and anodized in 5% HF at the potential of 0.5 V for 10, 20 and 30 min. These samples were oxidized (wet) at 900 °C for 20 h. Fig. 7 shows HR-SEM pictures of cross-sections of cleaved pillars (located at the center of the wafer). The porous layer thicknesses obtained were 1.1 μm, 2.3 μm and 3.5 μm for 10 min, 20 min and 30 min, respectively (Fig. 7). The resulting silica thickness underneath the PG layers was 1.1 ± 0.5 μm (Fig. 7), which yielded around 1.5 μm increase in total thickness of the pillar, which was 10 μm prior to oxidation. As a reference, a non-processed p++ Si wafer was oxidized under the same conditions, yielding a silica layer

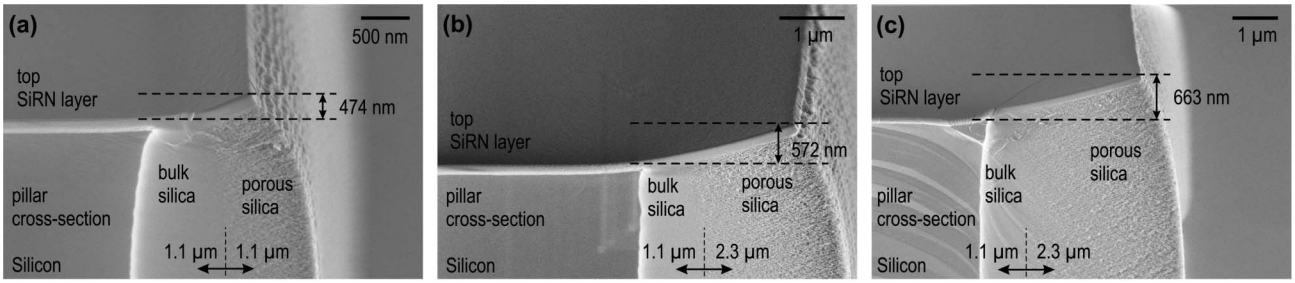

Fig. 7 HR-SEM pictures of 30% loading design for 10 min (a), 20 min (b), and 30 min (c) of anodization at 0.5 V in 5% HF followed by 20 h of wet oxidation at 900 °C.

thickness of 806 ± 10 nm. This provides evidence that the presence of a porous layer does not have a negative effect on the oxidation rate of the underlying Si. In other words, oxygen can easily diffuse through the porous skeleton and react with bulk Si to enable oxidation. Interestingly, the measured silica layer underneath the porous network was around 40% thicker than that on a non-processed wafer. A possible explanation for this could be that the size of the pores close to the bulk Si was significantly smaller compared to the outer part (Fig. 7), such that the complete closure of these pores could happen during the oxidation. The resulting silica layer could therefore be a combination of oxidized bulk and porous Si.

Expansion of the pillars during the oxidation caused an increase in not only their thickness but also their height because of the SiRN layer, which was used as a mask (Fig. 1). Expansion differences between Si/silica and PG on the sides of the pillars caused upward bending of the SiRN layer on top of the pillars (illustrated in Fig. 7). This is a well-known phenomenon: it is called the birds beak effect, which occurs during the selective oxidation of Si (LOCOS process).[49] The measured height differences were 474 nm, 572 nm and 663 nm for the total anodization times of 10 min, 20 min and 30 min, respectively.

In order to have a closed channel system, a glass wafer has to be bonded anodically as the last step of the fabrication process (Fig. 1). The above mentioned height difference caused by the upward bending of the SiRN layer may result in improper bonding. The anodization and oxidation times, hence the layer thicknesses of the PS and silica should be adjusted in order to restrict the amount of bending to a safe margin for enabling proper bonding (see Fig. ESI-4†).

3.3 Fluidic experiments

Although HR-SEM pictures demonstrated that the PS network and the bulk Si underneath were oxidized successfully, the full conversion of the PS skeleton into PG needed to be confirmed experimentally. Therefore, fluidic measurements were performed with the 30% loading design, *i.e.* 4 cm long, straight microchannels with 1 mm diameter reservoirs on both ends. As shown in Fig. 8(a), the channels for the experiments accommodated hexagonal pillars, whose length and the width were 100 µm and 20 µm, respectively. The PG layer thickness was 2.2 µm. A droplet of 10 µL of 1 mM Rhodamine B solution (Sigma-Aldrich, Zwijndrecht, The Netherlands) was placed into a reservoir in one end of the open channel. Fluorescent images were captured at the center of the channel while the solution

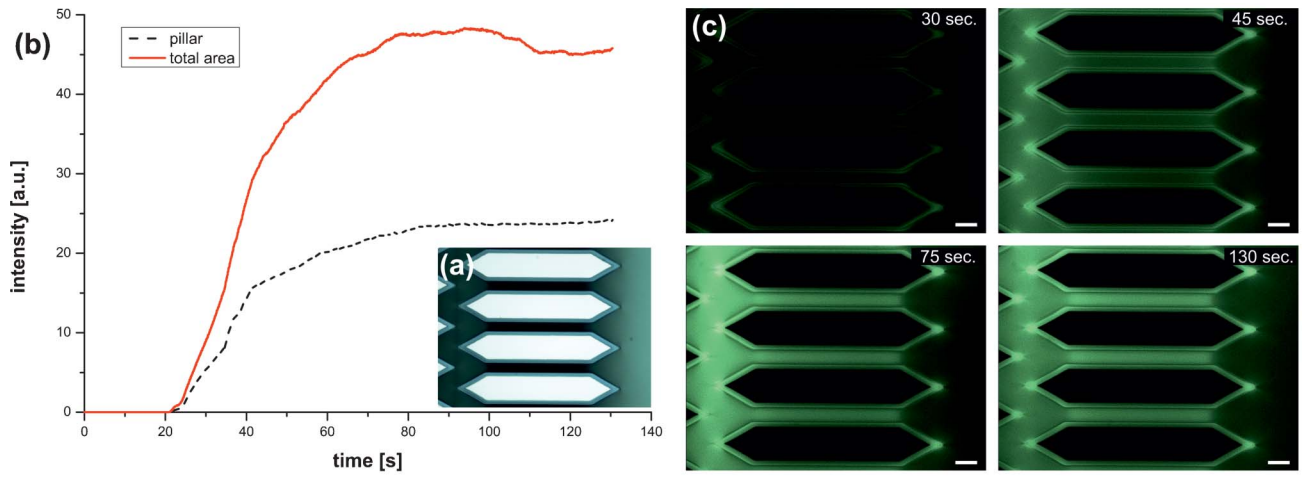

Fig. 8 Microscope image of ROI with hexagonal pillars before dye injection (a). The length and the width of the pillars are 100 µm and 20 µm, respectively. The PG layer thickness is 2.2 µm. The average intensities *vs.* elapsed time of the entire region shown in (a) and the PG layer surrounding a single pillar (b). Diffusion of Rhodamine dye into the PG network (c). Dye arrived at ROI (center point of a 4 cm channel) *ca.* 21 s after placement of the droplet into the reservoir. Snapshot images with timestamps illustrate the increase in the amount of diffused solution, which reached to a balance in around 1 min. Scale bars represent 10 µm.

was diffusing through the PG network. The change in intensity of the captured images was monitored in order to measure the increase in the amount of the sample transported by diffusion. Fig. 8(b) shows the change in the intensity with respect to the elapsed time for the region of interest (ROI) shown in Fig. 8(a). Fig. 8(c) shows a series of snapshot images of ROI where the fluorescent dye diffused into the PG layer, captured at different times. This experiment indicates that the obtained porous layer was totally transparent, which is not the case for PS. In addition, it was not possible to have the liquid diffuse into the PS layer because of the hydrophobic nature of its surface. PG is highly hydrophilic, which allowed diffusion and spreading of Rhodamine B through the entire PG network easily.

As seen in Fig. 8(c), the tips of the structures were brighter than the sides, which indicates that a higher amount of sample accumulated there. This phenomenon was observed for structures with corners or sharp tips, while the round shapes, such as circles, yielded a uniform distribution of Rhodamine B in the porous layer. This effect is due to a higher field strength at sharp corners during anodization, as compared to a flat surface. As mentioned earlier (section 3.1), the direction of the pore propagation coincides with the direction of the electric field lines during the anodization process. In addition, the field lines, as vectorial quantities, are always perpendicular to the surface exposed to the solution. As a result, the pores are formed on the surface, continue to grow in the direction perpendicular to it, merge when they coincide and create a canal, which can deliver higher amount of sample (see Fig. ESI-6†).

After investigating the PG network physically and optically on open channels, a series of electrical measurements was performed with closed channels. Simple cross layout microchips without any pillars were used for the electrokinetic experiments. The width and the height of the channels were 160 μm and 10 μm, respectively. The integrated PG layer thickness was 1 μm with an isolating solid silica layer underneath of 400 nm. Channels were filled with 10 mM, pH 9 sodium tetraborate buffer (Sigma-Aldrich, Zwijndrecht, The Netherlands) with a 50% acetonitrile (Sigma-Aldrich) volumetric composition and a neutral fluorescent dye, Coumarin 480D (Sigma-Aldrich) was used for flow measurements. C480D was injected electrokinetically and its migration was monitored. A Leica DMI5000 M inverted microscope system (Leica Microsystems, Rijswijk, The Netherlands) with an integrated motorized stage for electronic position control was used for the experiments. A Leica EL6000 unit light source, equipped with a mercury short-arc lamp (Osram HXP-R120W/45C VIS, Leica Microsystems) was used. The fluorescent emission from the sample was passed through a Leica filter cube D, which consists of an excitation filter (band-pass 355–425 nm), a dichromatic mirror (455 nm) and a suppression filter (long-pass 470 nm). The experiments were monitored using a Leica DFC300 FX color camera attached to the microscope. In order to measure the electroosmotic mobility, an increasing electrical potential was applied up to the dielectric breakdown limit. The maximum allowable voltage was 400 V, indicating a breakdown electric field of 10 MV cm^{-1} (it is typically 8–12 MV cm^{-1} for thermal oxide on bulk Si). The measured electroosmotic mobility was 2.6 × 10^{-9} m^2 V^{-1} s^{-1},

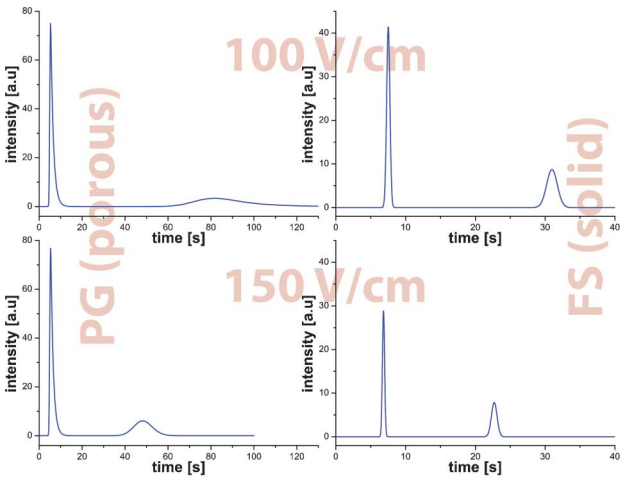

Fig. 9 Monitored peaks of Coumarin 480D for porous (PG) and non-porous (FS) cases at the injection point and 5 mm downstream. Mobile phase: sodium tetraborate buffer (10 mM, pH 9). Calculated plate heights for 100 V cm^{-1}: 14.5 μm for PG and 4.8 μm for FS; for 150 V cm^{-1}: 11.0 μm for PG and 2.8 μm for FS.

while the same chip design fabricated in fused silica (FS) with solid (non-porous) walls yielded 1.86 × 10^{-9} m^2 V^{-1} s^{-1}. Fig. 9 illustrates the monitored peaks at the injection point and 5 mm downstream for 100 and 150 V cm^{-1} e-fields for both PG and FS. Although it is difficult to draw a conclusion without applying higher e-fields and determining the optimum working potential, the reason for the higher dispersion for PG chip is that the porous layer is too thick compared to the channel height. Having the bottom of the channel porous but not the top glass lid (see Fig. ESI-4†) also enhances this dispersive effect. Moreover, the thickness of the porous layer should be optimized according to the channel geometry and the needs of the application.

3.4 Freestanding vertical structures of PS

During the experiments it was discovered that the processes discussed in this work can also be used for creating another interesting structure, namely fully released vertical-oriented cage-like structures composed of PS (Fig. 10). The fabrication of these structures was done as follows: For producing a typical *I–V* curve during anodization, the applied voltage was swept from 0 V to a certain value, which may exceed the electropolishing limit. This lead to the removal of the solid silicon layer behind the porous layer, and therewith creates vertical free standing porous walls. This method is related to previous work at our institute, giving porous tube-in-tube structures.[41] Fig. 10(a) shows the results of two voltage sweeps in 5% HF with the range of 0–5 V (56.5 s) and 0–15 V (67.9 s), respectively. The presented sample was a 5% loading design and the potential limit for polishing was 1.7 V (Fig. 3). Therefore, sweeping up to this potential resulted in a PS layer, whereas passing this limit yielded electropolishing which continued till the end of the sweep period after 56.5 s. A second sweep, performed for 67.9 s, caused thicker PS walls and higher void volumes. After the anodization, the SiRN layer on the top surface was removed. The result was two free

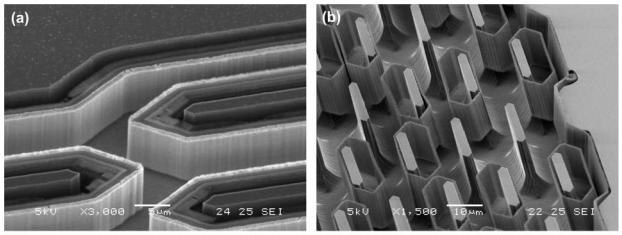

Fig. 10 SEM pictures of free standing vertical porous silicon walls obtained by voltage sweep applications in 5% HF. (a) 0–5 V for 56.5 s + 0–15 V for 67.9 s. (b) 0–10 V for 324 s.

standing, vertical and parallel porous walls with a void volume in-between.

Another voltage sweep was applied for the same design in 5% HF for the range of 0–10 V and a duration of 324 s. Increasing the time of anodization caused a significantly larger void volume behind the porous wall. Therefore, the porous walls collapsed/detached from the bulk Si because of the electrostatic forces upon removal of the SiRN layer (Fig. 10(b)). Such detached structures composed of porous walls can be fabricated in any geometry and transported with typical micro manipulators for integrating in microsystems. Oxidation of such freestanding vertical porous silicon walls/membranes into PG is the next step, but not yet investigated.

4 Concluding remarks

A method for fabricating the integrated PG layers in structured microchannels using microfabrication technology was presented. Determining the fabrication process steps, the anodization parameters were investigated for fabricating stable PS layers. The relationship between the applied voltage and the obtained current was revealed for such systems. Experiments showed that each design option has its own *I–V* characteristics. In other words, such *I–V* characterization curves should be produced for every design in order to determine the optimal working potential range for proper formation of PS. Complete conversion of a PS network into PG was performed by means of thermal oxidation (wet or dry). The effect of oxidation on pore size and porosity was determined. The critical parameters for realization of the Si based microchips with integrated PG were discussed. In order to validate the technique, successful full conversion of PS into PG was confirmed with HF etching of PG and flow visualization of fluorescent dye through the PG layer with microscopy. Eliminating the problems/drawbacks of existing methods for porous silica/glass fabrication and giving the possibility of integrating stable, uniform and crack-free PG layers onto 3-D microstructures during the micromachining processes, it is envisioned that this method has the potential of not only improving the current techniques such as membrane technology, catalyst supports, chromatography and electrokinetics, but also opening paths to new applications. Nanochannels can be fabricated by merging the pores during anodization and closing the pores while leaving the nanochannels open *via* subsequent thermal oxidation around reflow temperatures. PS or PG vertical walls can be fabricated in-between the microchannels for liquid/gas/biomolecule exchange/filtration/extraction applications.

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