A 100 – 800MHz 8-Path Polyphase Transmitter with Mixer Duty-Cycle Control achieving <-40dBc for ALL Harmonics

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Abstract—Radio transceivers capable of dynamic spectrum access require frequency agile transmitters with a clean output spectrum. High-Q filters are difficult to implement on chip and have limited tuning range. Transmitters with high linearity and broadband harmonic rejection can be more flexible and require less filtering. However, traditional Harmonic Rejection mixers suppress only a few harmonics. This paper presents an 8-path poly-phase transmitter, which exploits mixer-LO duty-cycle control and a tunable first-order RC low-pass filter to suppress ALL harmonics to below -40dBc. The optimum duty-cycle theoretically is 43.65% and a resolution of better than 0.1% is required to keep the spread in harmonic rejection within 1dB. We propose a simple monotonic duty-cycle control circuit and show by design equations and measurements that it achieves the required resolution over 3 octaves of frequency range. Also, analysis indicates that LO duty-cycle reduction compared to 50% improves power upconverter efficiency. A transmitter realized in 0.16μm CMOS works from 100-800MHz at a maximum single tone output power of 10.8dBm with an efficiency of 8.7%, outperforming previous designs. The OIP3 is >21dBm, while the LO leakage and image rejection is better than -45dBc.

Index Terms- Transmitter, Cognitive Radio, Dynamic Spectrum Access, Harmonic Rejection, Image Rejection, Mixer, Polyphase, Multipath, Power upconverter, Duty-cycle control.

I. INTRODUCTION

The FCC and other spectrum regulatory organizations are gradually moving towards allowing dynamic spectrum access of locally unused spectrum[1-3].Transmitters must avoid harmful interference with incumbent users of the frequency spectrum. In the TV bands, free channels of 6-8 MHz can be used, while keeping harmonics and distortion at other frequencies low. Agile transmission over a wide range of RF frequencies is desired, preferably with fully integrated hardware. As widely tunable high-Q band-pass filters are difficult to implement on chip, while switching high-linearity mixers produce many strong harmonics, there clearly is a challenge.

In literature we found three main approaches to address this problem. One approach exploits a sine wave like LO [4] driving a linear multiplier. However, high linearity analog multiplier design is challenging, while providing only modest output power compared to switching mixers. Also, flexible wideband sine wave LO-generation is non-trivial and the LO-amplitude is critical as it should not drive the LO-input of the multiplier into its non-linear region.

A second approach is to use switching mixers which do produce LO-harmonics, but cancel harmonics via multiple mixer paths exploiting different phases [5-9] or different phase and amplitude [10, 11]. These mixers can achieve high output power as they can operate in saturation. In order to achieve enough suppression multiple accurate phases of the LO and/or the baseband have to be generated, but digital clocks can be used. Flexibly programmable digital frequency dividers can be exploited, enabling software defined radios to benefit from Moore's law. Still, there are limits to the number of phases that can be realized at high frequency, while phase accuracy and power dissipation is also a concern [12, 13].

A third way to clean the transmitter spectrum obviously is to apply filters. However, frequency agile transmitters would require flexibly tunable RF filters, which are difficult to implement especially for high Q. Passive LC filters are linear but high-Q inductors are problematic certainly at low RF frequency and require large chip area. Active filter techniques can be used to suppress

higher order harmonics [11], but handling sufficient power at high linearity is a problem. On the other hand low-Q passive RC filters are suitable for on chip integration as well as being linear and power efficient, but generally do not provide enough suppression.

From the discussion above, we conclude that the multi-path mixer techniques exploiting digital square-wave LO-paths have the most attractive properties for agile dynamic spectrum access. In [10, 11], harmonic rejection is achieved using different LO-phases and amplitude weighting, sharing one baseband signal. If *multiple baseband phases* are also generated, we can realize a *Polyphase Multipath up-converter* (see Fig. 1, [5, 6]). Now, not only harmonics are cancelled, but also many distortion and side-band products [5, 6]. In other words: apart from harmonic rejection mixing, linearity benefits are achieved. Fig. 1 assumes that the non-linearity from the baseband – to-RF path is lumped into one nonlinear block. The multipath technique has also been exploited to cancel distortion products in a Digital to Analog conversion process [14] and also in a sine wave frequency synthesizer [15]. A modification of the technique has also been proposed [16], but it lacks image rejection. Although the polyphase multipath technique cancels many distortion products, it unfortunately *does not* cancel the problematic 2-tone IM3 inter-modulation distortion products at $2\omega_{bb1}$- ω_{bb2} and $2\omega_{bb2}$- ω_{bb1} [5], where ω_{bb} is the baseband (BB) signal. Digital predistortion [17] applied to the multipath architecture allows for suppression of these terms. Still challenges remain in achieving a broadband clean spectrum at reasonable complexity and power consumption. Furthermore, harmonic rejection techniques cancel many terms, but not all. The often cited mixer of [10] suppresses the 3^{rd} and 5^{th} harmonic of the LO, but the 7^{th} and higher harmonics are still there. The 18-path polyphase transmitter in [6] does cancel a larger number of harmonics and sidebands, however generating 18 clock phases consumes a lot of power and presents clock-distribution challenges, while a 6-path design doesn't suppress higher harmonics efficiently [6]. 18 paths would also require 18 Digital-to-Analog Converters (DAC) and baseband filters, making the complete transmitter design very complex and power hungry.

In this paper we present a power efficient 8-path transmitter with wideband cleaned spectrum.

The system concept verified by macro model simulations has been published in [9] (no circuit implementation). The principle is shown in Fig.2. It exploits three techniques: 8-path upconversion, duty cycle control and a first order filter with tunable cut-off frequency. The 8-path upconversion suppresses all even order harmonics of the LO, as well as the 3rd, 5th, 11th, 13th, along with many distortion products, while also having image rejection. The dominant un-cancelled 7th and 9th LO-harmonics are suppressed simultaneously, by making the LO duty-cycle ratio 0.4365 (~7/16) [9] (sweet spot in Fig.2). In this paper we aim to show that this is feasible in a power efficient way by tuning the rise time of the LO. Combined with a tunable 1st order low-pass filter, the worst case harmonic can be suppressed to below -40dBc. Note that this is achieved for ALL harmonics, while the transmitter works over 3 octaves of frequency (100–800MHz). Moreover, competitive distortion and power efficiency is achieved.

The paper is constructed as follows. Section II analyzes the duty-cycle control principle, its resolution requirements and its impact on transmitter efficiency. Section III then introduces the duty-cycle control circuit design and Section IV presents the complete transmitter implementation. Section V shows the measurement results, whereas section VI presents conclusions.

II. Principle and Implementation Considerations

Assuming square wave LO signals, without considering rise/fall times, the amplitude of the nth harmonic as a function of the duty- cycle D can easily be analyzed by Fourier analysis[9], giving:

$$V_n = \frac{A}{n \cdot \pi}\sqrt{2 - 2\ \cos(2 \cdot \pi \cdot n \cdot D)} \quad . \qquad (1)$$

Evaluating (1), in Table I, where A is the amplitude of the LO, we find an optimum duty-cycle of 0.4365 (43.65%) to achieve simultaneous rejection for both V_7 and V_9 to -31.9dBc compared to the fundamental. The conversion gain for the fundamental is -4.1dB, only slightly worse than the -3.9 dB ($2/\pi$) for 50% duty-cycle. The optimum is close to D= 7/16 (43.75%) [9], where we find -30.9dBc and -33dBc for the 7th and 9th harmonic. Comparing the results, we see that the optimum

is rather sensitive: a duty-cycle change of 0.1% from the optimum renders 1dB worse rejection. The variation in the 9th harmonic is less of an issue as higher harmonics undergo more attenuation by low-pass filtering.

From the analysis above, we conclude that a duty-cycle equal to 43.65%, very close to 7/16 is the sweet spot to reject both the 7th and 9th harmonic, whereas a reproducibility better than 0.1% is needed to keep the 7th harmonic suppression within 1dB of its target value. We will now examine the effect of using multiple paths and mismatch between paths.

A. Impact of multi-path and mismatch

A mathematical analysis of the effect of mismatch on multi-path polyphase circuits can be found in [5], providing an estimate of the Harmonic Rejection Ratio of cancelled (*C*) harmonics as:

$$E(HRR_{k,m})_C = \frac{P_{k,m,reference}}{P_{k,m,rejected}} = \frac{\mathrm{N}^2}{(\mathrm{N}-1)\left(\frac{\sigma_\varepsilon^2}{a_1^2} + {k_{LO}}^2\sigma_\theta^2 + m^2{\sigma_\delta}^2\right)} \quad . \qquad (2)$$

where $E(HRR_{k,m})$ is the expected value for a tone resulting from the k[th] harmonic of the LO (k_{LO}) and m[th] harmonic of the baseband signal, a_1 is the constant in the Taylor series approximation of a weak non-linear system, and N is number of paths [5]. $P_{k,m,reference}$ is the power before rejection, produced by a single path transmitter, while $P_{k,m,rejected}$ is the power after (imperfect) rejection by the multipath technique due to the presence of mismatch. ${\sigma_\theta}^2, {\sigma_\delta}^2, {\sigma_\varepsilon}^2$ are the variances of the stochastic variables θ (LO phase mismatch error), δ (BB phase mismatch error) and ε (amplitude mismatch error), respectively. Note that a higher number of paths has a positive effect on HRR. In order to find the effect of mismatch on the harmonics which are not cancelled *(index NC)*, a similar analysis is done, resulting in:

$$E(HRR_{k,m})_{NC} = \frac{P_{k,m,reference}}{P_{k,m,non-rejected}} = 1 - \frac{(N-1)}{N^2} \cdot \left(\frac{\sigma_\varepsilon^2}{a_1^2} + {k_{LO}}^2\sigma_\theta^2 + m^2{\sigma_\delta}^2\right) \qquad (3)$$

Note that the expected value of this equation for small values of amplitude and phase mismatch is very close to one. This is because the non-cancelled harmonics even in the presence of mismatch almost fully add up in phase. In the measurement section we will observe this effect.

B. Implementation Considerations

Theoretically, a 7/16 duty-cycle [9] mixing clock can be realized by dividing a 16x higher clock. Compared to a DLL, this is more power efficient for the same mismatch accuracy [12], but there is a limit to the maximum frequency which can be achieved. In the 160nm CMOS technology that we used, 16x800MHz was problematic. Moreover, from Table I we see that it is actually better for the 7^{th} harmonic rejection to tune the duty-cycle to a slightly lower value than 7/16.

Since 0.4365 is rather close to 0.50, we use an 8-phase 50% duty-cycle clock generated by a divide-by-4 circuit and delay the rising edge (only by a ratio of 0.063) to reduce duty-cycle (see Fig.3, node B). This low delay introduces a negligible phase noise degradation compared to other sources of noise. The buffer afterwards again makes the edge steep. To ensure a clean output spectrum, the harmonic content can be monitored and controlled by adapting the duty-cycle. A cognitive radio transceiver would likely have a spectrum analyzer on board [18]-[21]. The harmonics of the transmit frequency can be detected by the spectrum analyzer provided they fall within the band of the analyzer, which is likely for low transmit-frequencies, where the high harmonics are the most problematic. If the 7^{th} or 9^{th} harmonics are at a very high frequency outside the input frequency range of the spectrum analyzer, detection will require additional techniques, for instance exploiting harmonic mixing.

Spectrum sensing receivers should be very sensitive and able to measure very weak signal levels and with good degree of accuracy. Even if currently such receivers are not available commercially, we think that this will change. See for instance the performance numbers achieved in [18], [21]. In this paper we assume that detection of problematic harmonic content is feasible and aim for duty-cycle tuning to control this problem. We will exploit a switched transconductor

mixer [22] to provide linear upconversion mixing and power gain, while consuming low voltage headroom.

C. Power efficiency

In this section we aim to coarsely model the effect of duty-cycle reduction on power efficiency. We will model the mixers with ideal switches and equal and perfectly large-signal linear transconductors (G_m=g_m see Fig.4, where only the single ended mixer of the implemented differential architecture is considered for simplicity and where BB is the analog baseband input). During the on-time we assume operation around a DC overdrive-voltage V_{DC} with a baseband signal amplitude V_p<V_{DC}. With these assumptions, the DC current consumption is proportional to duty-cycle D, and the total DC power becomes:

$$P_{DC} = V_{DD} \cdot N \cdot G_m \cdot V_{DC} \cdot D \quad . \quad (4)$$

Note that in this multi-path transmitter with an even number of linear mixers, the baseband signal does not affect the total dissipation, as the increase of a current in one mixer is accompanied by an equal decrease in another anti-phase one (see Fig.4).

To calculate the desired output power, consider that all RF current-paths have the same phase and add up constructively, resulting in a power proportional to N^2. Using (1) for n=1, we find:

$$P_{rf-desired} = \frac{N^2 \cdot g_{m1}^2 \cdot V_p^2 \cdot (2 - 2\cos(2 \cdot \pi \cdot D))}{8 \cdot \pi^2} \cdot R_L \ . \quad (5)$$

Dividing (5) by (4), we find the power efficiency as a function of D as plotted in Fig. 5. The following practical values were used:N=8, g_m=35mS, V_p=0.2,V_{DC}= 0.32, V_{dd} =1.5. The efficiency curve peaks at a duty-cycle of around 0.37. The desired signal ($P_{rf\text{-}desired}$) starts to decrease after D=0.5, while the DC power (P_{dc}) continues to increase as shown in Fig. 5, therefore intuitively the optimal point should lie somewhere before that. In order to assess the validity of this very coarse model, circuit simulations (using the mixers discussed in Section IV.C) in a standard 160nm CMOS process are also shown in Fig. 5. The predicted shape is roughly right, but with a shift. This difference is mainly due to the assumption that one mixer path does not influence the

other and also assuming linear devices. Simulations done with different circuit parameters show the optimum efficiency point lies in the range D=0.25 and D=0.35. We conclude that the targeted duty-cycle D=0.4365 lies between D=0.5 and the optimum efficiency point. Although not exactly optimal, the power efficiency compared to D=0.50 is 10-20% better.

III. DUTY-CYCLE CONTROL CIRCUIT DESIGN

Fig.6 shows the block diagram of the system implemented on chip. Fig.7 shows how the controllable duty-cycle shown in Fig. 3 is realized on circuit level, by delaying the rising edge of a 50% clock. The clock divider output is buffered and then an inverter with controllable rising edge delay drives the last buffer stage. The control is accomplished via a tunable resistor, implemented as a triode PMOS transistor (MP2) as shown in Fig.7. For control purposes, monotonic control is desired, which is realized by controlling the gate voltage of the triode transistors by an intrinsically monotonic resistor ladder DAC. In order to achieve this control over multi-octaves of frequency range, additional triode transistors can be added via switches S_1-S_5 as shown in Fig.8, where DAC voltage (V_{DAC}) is shared. There are two main requirements on the design: 1) There should be sufficient resolution to keep the duty-cycling variations within 0.1% as discussed at the start of section II.2) The required duty-cycle should be provided over multiple octaves of frequency range.

The following sub-sections describe how these requirements can be met.

A. Duty-Cycle for the required accuracy

In order to estimate the delay caused by the inverter-PMOS and triode-PMOS combination, we will calculate the charge current for capacitor C_{in} in Fig.7. The current through the PMOS transistor MP1 degenerated by a resistance R_T can be coarsely modeled as:

$$I = \frac{\beta}{2}(V_{IN} - I \cdot R_T - V_{TH})^2 \quad . \quad (6)$$

Here R_T is the resistance of the triode transistor as given by (7) and $\beta=\mu_p C_{ox} \cdot \frac{W}{L}$.

$$R_T = \frac{1}{\beta_T \cdot \left(V_{gs_{MP2}} - V_{TH}\right)} \quad . \qquad (7)$$

Expanding (6) results in (8).

$$\frac{\beta}{2}\left(I^2 {R_T}^2 - I\left(2 \cdot R_T \cdot V_{IN0} + \frac{2}{\beta}\right) + {V_{IN0}}^2\right) = 0 \quad . \quad (8)$$

Where $V_{IN0} = V_{IN} - V_{TH}$, Solving the quadratic equation of (8) results in (9).

$$I = \frac{V_{IN0}}{R_T} + \frac{1}{\beta \cdot {R_T}^2} \cdot \left(1 - \sqrt{1 + 2 \cdot V_{IN0} \cdot \beta \cdot R_T}\right) \quad . \quad (9)$$

This current can be used to estimate the delay due to the triode PMOS by the following equation.

$$t_d = \mathrm{C_{in}} \cdot \frac{\Delta \mathrm{V}}{I} \quad . \quad (10)$$

where t_d is the rise time delay, C_{in} is the capacitance at the input of the last buffer and ΔV is taken as $V_{DD}/2$, the point where the last buffer switches. Equation 10 is plotted in Fig.9, after substituting the values of C_{in} =300fF, β=12.5mA/V^2, V_{IN}=1.5V, V_{TH}=0.5V and β_T is 0.78mA/V^2 for the LSB triode PMOS (MP2). Fig.9 also shows the simulated (in 160nm CMOS process) values of the delay plotted as a function of V_{gs} of the triode (MP2) transistor. The delays for the 2, 4, 8 and 16 times the LSB triode PMOS size are also shown. As |Vgs| for MP2 decreases from 1.5V to 1V, the delay becomes more than half of its initial value. A higher delay can be achieved by reducing the |Vgs| further, but larger |Vgs| is better to keep the variation in the resistance of MP2 limited due to V_{th} mismatch. Also larger |Vgs| keeps the MP2 PMOS in deep triode. The steepness of the delay curve is lower at larger |Vgs|, which is desired since it provides smaller delay steps. Therefore the range of Vgs chosen is from -1.5V to -1V. The gate voltage required is generated by a 5-bit resistor ladder DAC which achieves a resolution of 1.25ps (for 800MHz LO) with some margin (from (10)). High frequency VDD variations are coupled to the gate of the triode transistors with the capacitor Cc, attempting to leave V_{gs} unaffected.

B. Duty-Cycle over a Frequency Range

In order to achieve the required duty-cycle over the 3 octaves frequency range an estimate is needed of the resistance value of the tunable resistor. This resistance value should satisfy the boundary conditions of achieving the required delay over the frequency range. The total rising edge delay required is about 1/8 of the LO time period. As there will always be some fall time present in the LO path, that has to be taken into consideration as well. Also, depending on the exact shape of the transition edges, some fine tuning may be needed. From simulations done on the LO path the falling edge delay time at the mixer switch remains around 70-90ps for the 100-800MHz frequency range. After subtracting the fall time from the required rising edge delay time, an estimate of the rising edge delay t_d is found. This delay is in the range of 60ps to 1.1ns (for the highest and lowest frequency). The resistor values can be estimated by substituting (9) in (10) and solving the quadratic equation for R_T.

$$R_T = \frac{t_d}{V_{DD} \cdot C_{in}} \cdot \left(V_{IN0} + \sqrt{\frac{2 \cdot V_{DD} \cdot C_{in}}{\beta \cdot t_d}} \right) \quad . \quad (11)$$

Solving (11) we find that the biggest resistor required is almost 13 times bigger than the smallest value. A 5-bit resolution of the parallel triode transistor was chosen to be able to cover the frequency range with some overlap between switching of the binary weighted PMOS transistors. The switch sizes S1..S5 in Fig.8 were made big enough so as to not be dominanting the control mechanism. Since the DAC voltage is distributed to all the paths with some series resistance, a local decoupling capacitor is used to bypass the high frequency voltage components that can couple from the LO path to the DAC output.

C. Duty-Cycle variation with Temperature

In order to assess the behavior of the duty cycle control circuit with temperature variation, circuit simulations were performed on the circuit of Fig.8 and the duty cycle was measured at the input of the mixer switch (node C). The temperature was swept from -30°C to 80°C, while the

optimum code was set for 20°C. The results in Fig. 10 show that for around 25°C increase in temperature the duty cycle varies by 0.1%. Further simulations including the mixer reveal that there is a variation in harmonic responses of about 1dB from the optimum code if the temperature varies by ±10°C (20°C in total). So we would recommend doing an offline re-calibration for each 20 degree variation in temperature, as real time calibration during operation might cause harmful interference. This re-calibration could probably be done in a closed loop by sweeping through a set of subsequent codes starting from 50% duty cycle until a minimum in harmonic power is detected, exploiting the monotonic control characteristic discussed earlier in this section. Frequent recalibrations are probably not needed once chip temperature is stable within about 20 degrees.

IV. Transmitter Circuit Implementation

Each of the 8 paths in Fig.6 consist of a sample and hold block, buffer and baseband filter and a switched transconductor upconversion mixer. The current output of the mixer blocks is combined to drive the antenna load. A tunable lowpass filter at the output provides filtering over a wide band. A replica bias circuit is used to stabilize the bias current of the mixers over Process-Voltage-Temperature (PVT) variations, attempting to keep the output power stable. An 8-phase LO with 1/8 duty-cycle drives the eight sample and hold (S&H) switches. Another 8-phase LO with ~7/16 duty-cycle drives the eight upconversion mixer switches. The circuit implementation did not aim for any specific standard but rather explored what can be achieved with this technique in practice, especially compared to [6]. Circuit details for these blocks are given in the following sections.

A. Baseband Generation

Fig.11 shows the circuit present in each baseband and upconversion path, driven by an (external) DAC. The use of one DAC for all 8 paths is preferable to maximize matching of the signal paths. The 8 polyphase baseband signals are generated digitally and drive the DAC in a time interleaved

way at 8 times the baseband sampling frequency. The sample switch S1 in the S&H of each path de-interleaves the DAC signal into 8 parallel analog baseband signals. To this end, the S&H switches are driven by an 8-phase non-overlapping 1/8 duty-cycle clock (S&HLO). The S&H is designed such that it is not limiting the linearity of the upconverter at full swing; also the switch size is small (1u/0.16u) which does not require significant power consumption. The interleaving mechanism can be understood as the generation of a high frequency signal, while the de-interleaving could be understood as the down-conversion of a high frequency signal to baseband along with the generation of the required phases. Fig.12 shows an ideal time domain output of the DAC for a single tone polyphase baseband. Two of the de-interleaved baseband signals are also shown for visualization. The buffer provides isolation between the S&Hs and the baseband filters. Isolation during the on-time of the S&H is further improved by the switch $\overline{S1}$, which disconnects the baseband RC filter from the S&H during the S&H switching transients [23]. For a channel bandwidth of 6MHz (3MHz in both I and Q), the sampling frequency (f_s) was set at 48 MHz. The sinc response due to the DAC hold function and the baseband filter response are shown in Fig.13. The multiphase baseband when upconverted via the multiphase mixers results in cancellation of the first DAC replica image [24] occurring around f_s. The second DAC replica image around $2f_s$=96MHz is suppressed to <-55dBc due to the combination of RC filter and the sinc response as shown in Fig.13 (adding the attenuations). A cascade of three RC sections with increasing resistance but with equal pole frequency of 10MHz was used as low-pass filter. A replica bias circuit (discussed in the next section) controls the bias current of the mixer by adjusting V_{bb}.

B. Replica Biasing

A replica biasing circuit was utilized as shown in Fig.14. The aim was to keep the mixer current and hence delivered power to the load controlled by a bias current. To this end a scaled replica of the switched g_m mixer is biased by current I_{bias}. A diode-connected scaled g_m transistor absorbs

the current and generates a voltage V_{ref}. The gate of the lower transistor in the mixer replica is connected to VDD to mimic the ON state of the mixer switch. Now V_{ref} is the wanted DC bias voltage corresponding to wanted mixer bias point. This voltage should be generated by all buffers if their input is equal to V_{DAC_DC}, the middle of DAC range (externally generated here by a voltage source as the DAC was external). To do this, a buffer replica is connected to V_{DAC_DC} and an error amplifier adapts the gate of the PMOS current source MP_{cur}. The amplifier is implemented by a two stage op-amp. Its high gain forces voltage V_{track} equal to V_{ref} by adjusting voltage $V_{filter_bias,}$ making the mixer bias insensitive for PVT variations. The V_{filter_bias} voltage is used as bias for all the baseband paths. The compensation capacitor C_c makes sure that the phase margin of the loop is more than 70 degrees over all process corners.

C. Mixers

The switched transconductor (switched-g_m) mixer architecture in which a transconductor is switched on and off [22] was utilized to provide frequency translation as well as power gain. Fig**.**15a shows the switched-g_m mixer used in [6], where the lower transistors implement the switches and the upper ones the transconductor. In the current design, a split-switch architecture for the switched-gm mixer was utilized as shown in Fig**.**15b, where Vo+ and Vo- are the differential outputs across the load (2×50Ω). The switch size was divided equally between the two arms of the g_m, with negligible effect on the LO-buffer loading. This was done to shift the compression point to a higher input swing and to improve linearity. The ON resistance of the mixer switch now acts as source degeneration for the transconductor. As discussed in [5, 6] the optimum size of g_m transistors and switch transistors is equal for maximum amplification for a given area. However, reducing the size of the switch is beneficial for reducing the power consumption in the driver buffers. For the current design a size of 100µm/0.16µm was chosen for each switch transistor and 200µm/0.16µm for each trans-conductor. Simulations show that using

the split-switch mixer (Fig.15b) improves the compression point and OIP3 by 3dB and 1dB respectively as compared to the shared-switch mixer (Fig.15a).

D. Tunable 1st Order Low-Pass Filter

A tunable RC low-pass filter is applied at the output of the mixer to suppress the higher harmonics. A bank of switchable binary weighted capacitors in combination with the load resistor (50Ω, single ended) (shown in Fig.16) provide a first order RC roll off, where the current source represents the switched-g_m mixers. The NMOS switch sizes were kept large enough to keep their ON resistance low, so as not to limit the suppression achieved. The magnitude of the fundamental component can vary significantly with LO frequency if there is not enough resolution in the capacitance bank. In order to keep these variations <0.5dB from the nominal value, a 5 bit resolution was chosen. Alternatively a coil can be added to realize a band-pass filter with tunable center frequency. This can give more suppression but results in less tuning range for the same capacitor variation. Since this filtering occurs after the mixers, any nonlinearity added by this filter would not be cancelled. Therefore fringe capacitors were utilized, which are more linear than MOS capacitors. A summary of the different calibrations is shown in Table II.

V. MEASUREMENT RESULTS

The transmitter was implemented in a 160nm CMOS process, and its die photo is shown in Fig.17. The RF choke (see Fig.11) and the load (2×50Ω) are off chip. Fig.18 shows the measured fundamental power at 400MHz LO, as well as the 7th and 9th harmonic response for all the 1024 (5+5 bits) duty-cycle codes. Here the code 0 implies a duty-cycle ratio close to 0.5 (S_1-S_5 in Fig.8 all ON) and higher codes gradually move towards lower duty-cycle ratios as explained below. The abrupt jumps in the harmonic response occur when a binary scaled PMOS transistor is turned ON/OFF by S1-S5. The smaller steps occur when selecting a next tap of the ladder DAC, which increases the V_{DAC} increasing R_T and hence decreasing the duty-cycle. Clearly, there are more than enough codes to fine tune the harmonic power with better than 1 dB precision via the ladder

DAC (see inset of Fig. 18).This works uptill the maximum LO frequency of 800MHz, beyond which the divider stops working. At code 512, the MSB switches OFF and due to the un-symmetric layout of the MSB PMOS (B5), there is an upward jump in the harmonic response, which causes some repetition in the harmonic responses upto around code 700. This repetition along with the overlap in codes (2 or more codes giving the same harmonic response), can easily be detected and removed by a one-time calibration. This calibration can be done by selecting non-overlapping harmonic responses of adjacent MSB transitions as shown in the inset of Fig.18 (larger symbols). It should be noted here that the selected codes are the ones where the LSB switching due to the ladder DAC just begins, i.e. where V_{DAC} is zero. This is where the triode resistance is smallest rendering lowest delay and best delay resolution, since the V_{gs} is the maximum. After removing the redundancy a smoother curve results as seen in Fig.19, where the x-axis now only shows the non-overlapping codes. The figure shows the magnitude of the dominant un-cancelled harmonics, occurring around the 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics of the LO (at 400MHz). In this scheme the optimum point occurs at code 134. Even after removing the redundancy there is enough resolution such that the harmonic responses to the non-overlapping codes adjacent to the optimal point are within 0.5dB of each other. The 3^{rd} and 5^{th} LO harmonics are also better than -44dBc and -50dBc respectively. Measuring 10 chips from one batch (where the optimum code was extracted for 1 chip and applied to 9 other chips of the same batch), we found this optimal point to remain within 1dB and ±2 code steps of each other, which proves that the design has enough resolution to cover variations due to mismatch (as targeted in section III.A). Similarly the mismatch measured over 10 chips of one batch for the dominant uncancelled harmonics (for the same set of non-overlapping codes) is shown in Fig.20. Less than 1dB variation in the 7^{th}, 9^{th}, 15^{th} and 17^{th} harmonics occurs due to their in-phase addition as was predicted by (3). The measurements at harmonic number -1 and 0 are for image and LO leakage respectively.

It is also of interest to see the 5^{th} and 3^{rd} harmonic in Fig.19 decreasing in power around the non-overlapping codes 185 and 195 respectively, which theoretically correspond to the duty-cycle of 40% and 33% as predicted by (1) [9]. As the code increases the duty-cycle becomes smaller and smaller, and after code 200 it becomes significantly dominated by rise and fall times, resulting in a significant drop in the fundamental output power.

Fig.21 shows the harmonic response over LO-frequency with 5MHz steps, while the non-overlapping duty-cycle code was adjusted for each LO frequency by monitoring the spectrum analyzer data for the 7^{th} and 9^{th} LO harmonics and selecting the non-overlapping code where both of them are simultaneously suppressed. The RF filter was tuned in six steps from 100 MHz-250MHz, beyond which the filter was not required, as parasitics at the output of the chip keep the 15th and 17th harmonics already below -40dBc.

Fig.22 shows the measured mixer efficiency as a function of the non-overlapping duty-cycle code when the LO is at 400MHz. The efficiency reaches a maximum around the non-overlapping code 185 which implies a duty-cycle around 40%, which is close to the prediction made for the optimum by the analysis in section II.C. Fig.23 shows the image and LO leakage for a 2.5MHz single tone upconverted by 800MHz to 802.5MHz. Both are measured to be better than -45dBc without calibration, over the whole band for 10 chips. This is 10dB better than [6], and can be attributed to using a shared DAC for signal generation. The maximum single tone $P1_{dB}$ output power after filtering was measured to be +10.8dBm, while the mixers consume 59mA from a 1.5V supply. The divide by 4 circuit, LO buffers and control DAC consume 33mW at 500MHz. The baseband clock divider and buffers and the baseband filters consume 13.5mW and 16.5mW respectively. Overall the efficiency is at least 2x better than [6] and 5x better than [11] at lower frequency. For higher frequency [11] does not use the multipath mixer, but still the power efficiency of the current design is better.

Spectral purity was tested in several ways. A wideband spectrum for a 2.5MHz single tone upconverted by a 100MHz LO is shown in Fig.24. The harmonics are at <-45dBc upto the 15th

harmonic, while the 15th and 17th harmonic are also ≤-40dBc. A 2-tone test showed an OIP3 of +21 dBm at 100MHz. At higher frequencies this gradually drops to +18dBm mainly due to the drop in fundamental signal power. The thermal noise was measured to be -153dBc/Hz at 35MHz offset from the carrier. Below this offset the quantization noise of the 8-bit DAC and the baseband filter is dominant. The transmitter was tested with phase shifted signals generated digitally, but interestingly it is also possible to apply an analog signal centered at the sampling frequency and use the on chip de-interleaver to analogly produce the required polyphase signals, similar to [25]. In order to get an idea of the EVM performance, a DVB-T like OFDM signal is tested with 2048 sub carriers, in a 9.14 MHz BW, 1705 of which actively carry data (64-QAM) and pilot tones (BPSK) upconverted to 128 MHz shown in Fig.25. An EVM of -30 dBc (3.2%) was achieved at 4.6 dBm output power, while keeping 7^{th} and 9^{th} harmonics at 40dBc. The rejection of 7^{th} and 9^{th} harmonics is hardly impacted by the wide channel bandwidth of the signals. Instead, it is mainly dependent on the duty cycle of the LO and the RF filter. A comparison with other works addressing agile broadband clean transmission is shown in Table III. In comparison this design achieves better output power and efficiency, while also improving on LO Leakage and image rejection. The active area of the chip is also smaller.

VI. CONCLUSION

A frequency agile 8-path polyphase transmitter concept and circuit implementation has been presented, achieving a <-40dBc clean output spectrum for all harmonics. This is the first multi-path polyphase transmitter combining the baseband multi-phase generation and RF circuit on one chip, together with a new duty-cycle control circuit which simultaneously suppresses the 7^{th} and 9^{th} LO harmonics. The simple but effective duty-cycle control circuit can produce a close to 43.65% duty-cycle with less than 1dB error from the optimal point. Overall the agile power upconverter works over 3 octaves in frequency from 100MHz to 800MHz. Compared with other designs with similar frequency range, it is more power efficient, has better LO leakage and image

rejection. The maximum efficiency and OIP3 is better than 8% and 21dBm respectively, while the image strength and LO Leakage is also better than -45dBc. It suppresses ALL LO harmonics without any external filters.

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Captions :

Fig. 1. Basic Principle of Polyphase Multipath Up-conversion.

Fig.2. Three Techniques used in the power efficient8-path Transmitter.

Fig.3. Delay rising edge to reduce duty-cycle.

Fig.4. Model of the 8-path switched-g_m mixer.

Fig.5. Calculated vs. Simulated Mixer Efficiency.

Fig.6. Block Diagram of the implemented 8 path Transmitter.

Fig.7. Duty-cycle control varying R_T, implemented as a triode PMOS MP2 driven by a ladder DAC.

Fig.8. 7/16 LO-duty-Cycle Generation and Control over frequency.

Fig.9. Calculated and Simulated Delay.

Fig.10. Duty Cycle Variation with Temperature.

Fig.11. One Baseband to RF path with S&H, filter and mixer.

Fig.12. DAC output containing all the 8 polyphase baseband signals (2 of the phases are in bold).

Fig.13.Sinc and RC low-pass filtering, achieving <-55dBc at $2\times f_s$.

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Fig.15. (a) Mixer used in [6] (b) Mixer in current design.

Fig.16. Switch Capacitor bank providing output filter tuning.

Fig.17. Chip micrograph with active area < $0.32mm^2$ in 160nm CMOS.

Fig.18. Magnitude of 7^{th} and 9^{th} harmonics vs. Duty-Cycle code(LO at 400MHz). Bigger markers are for those duty cycle codes which give non-overlapping harmonic response.

Fig.19. Magnitude of harmonics vs. Non-Overlapping Duty-Cycle code(LO at 400MHz). Same graph as Fig. 18 but with overlapping harmonic responses removed.

Fig.20. Harmonic Strength measured for 10 chips (LO at 400MHz).

Fig.21. Measured magnitude of harmonics vs. LO-frequency for optimal code.

Fig.22. Measured Mixer Efficiency vs. Non-overlapping Duty-Cycle Code.

Fig.23. Image and LO Leakage magnitude.

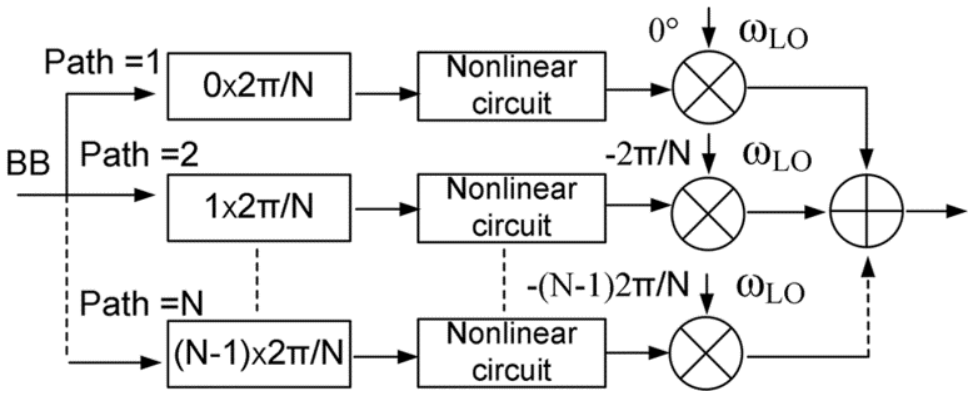
Fig.24. Measured wideband spectrum for 100MHz LO.

Fig.25. Measured Output Spectrum and Signal Constellation for a 64 QAM OFDM signal.

Table I. Harmonic Strength versus Duty-Cycle (calculation).

Table II. Summary of Calibrations.

Table III. Benchmarking to other Harmonic Rejection Transmitters.



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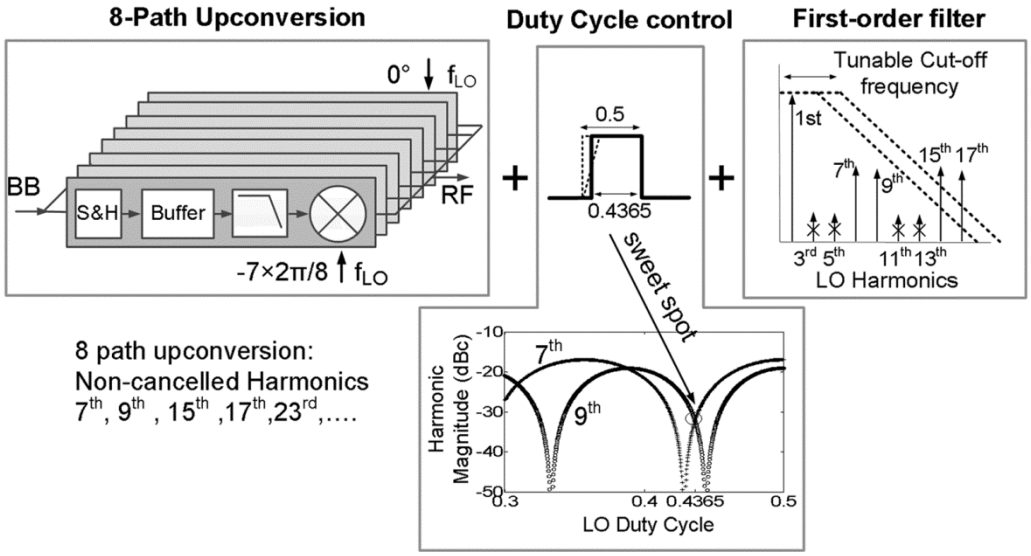
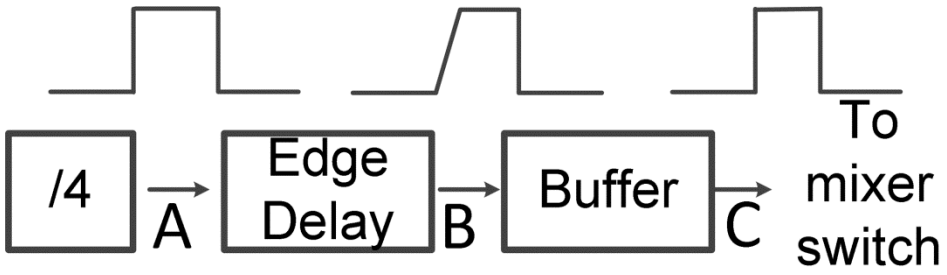


Fig.2.Three Techniques used in the power efficient 8-path Transmitter.

Table I. Harmonic Strength versus Duty-Cycle (calculation)

Duty Cycle	V_1 (dB)	V_2 (dB)	V_7 (dB)	V_9 (dB)
50.00%	-3.922	-121.466	-20.824	-23.007
43.55%	-4.101	-18.027	-37.200	-35.040
43.60%	-4.099	-18.091	-36.600	-35.530
43.65%	-4.096	-18.155	-36.039	-36.050
43.70%	-4.093	-18.220	-35.514	-36.606
43.75% (7/16)	-4.090	-18.286	-35.02	-37.202
43.80%	-4.088	-18.352	-34.553	-37.843



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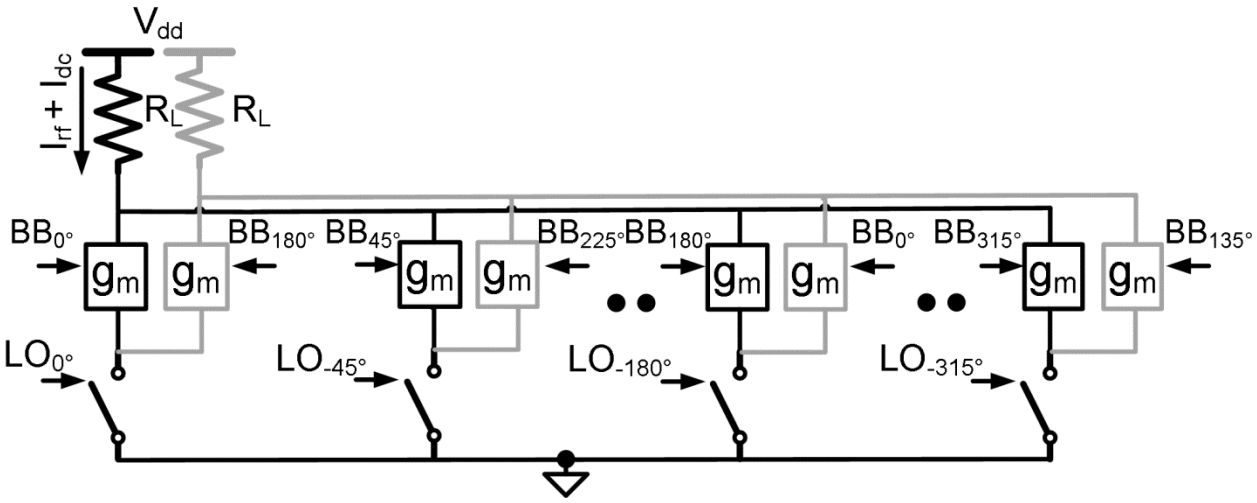

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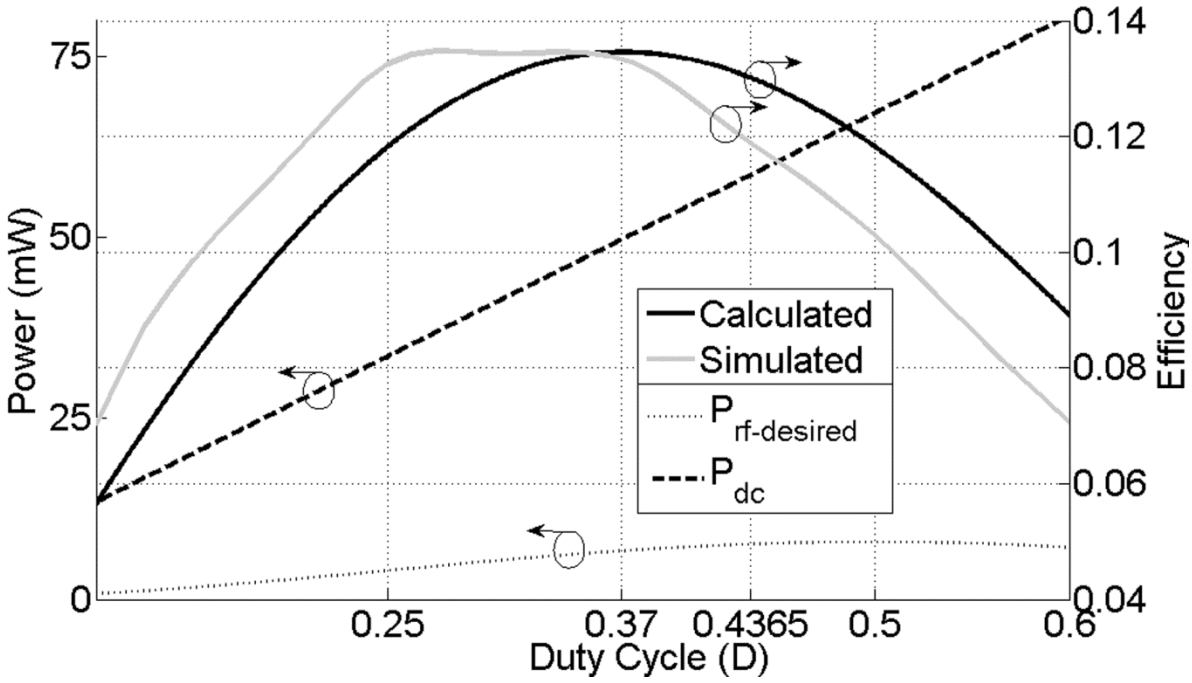
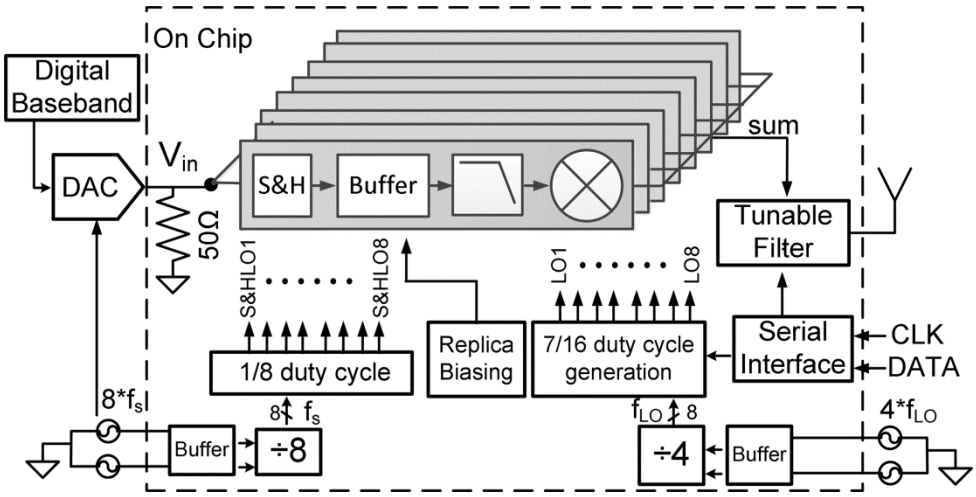


Fig. 5. Calculated vs. Simulated Mixer Efficiency



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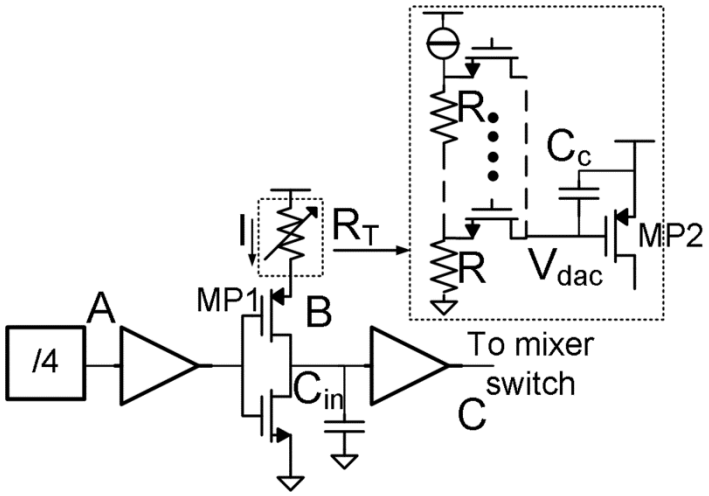
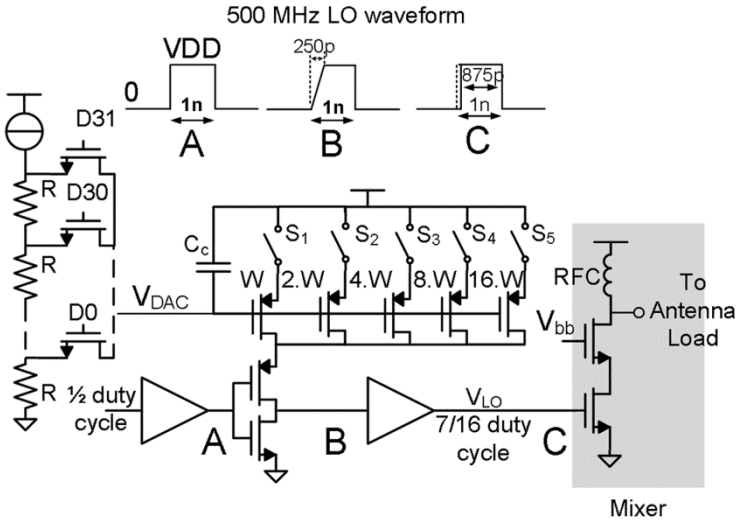


Fig.7.Duty-cycle control varying R_T, implemented as a triode PMOS MP2 driven by a ladder DAC.



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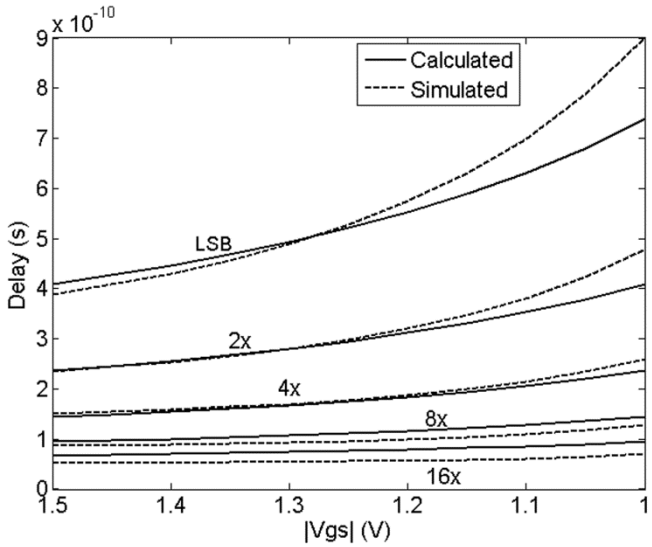

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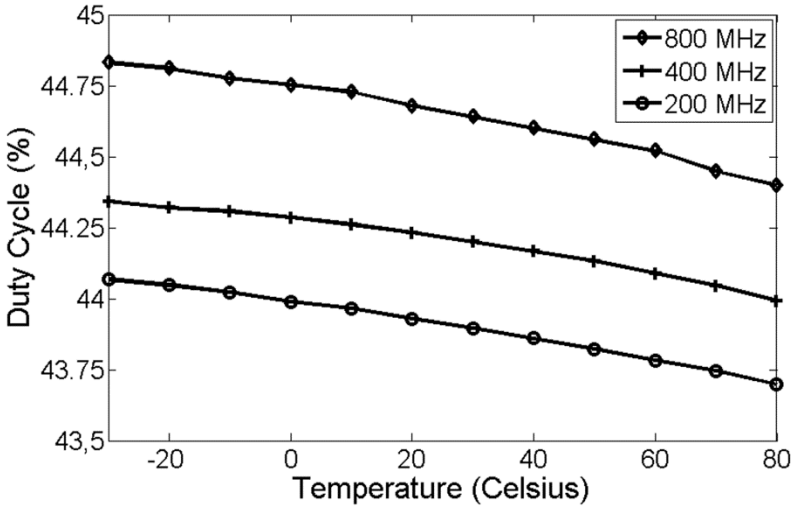
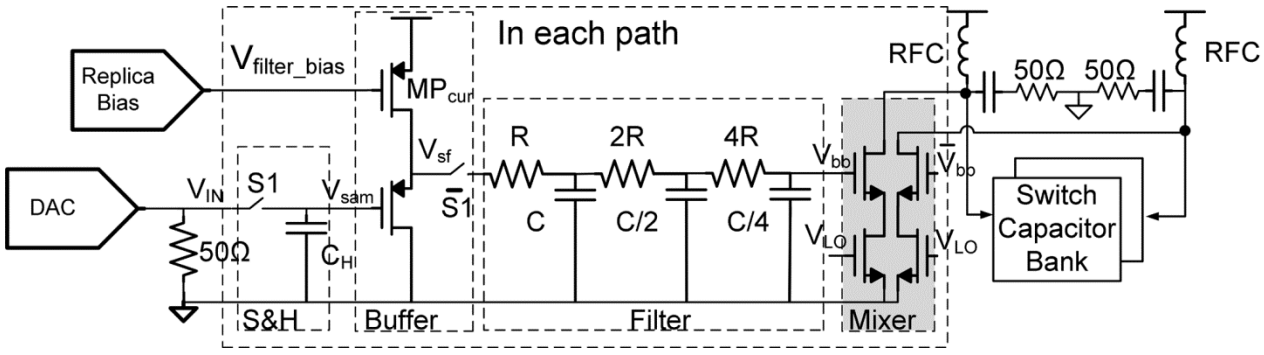


Fig. 10. Duty Cycle Variation with Temperature.



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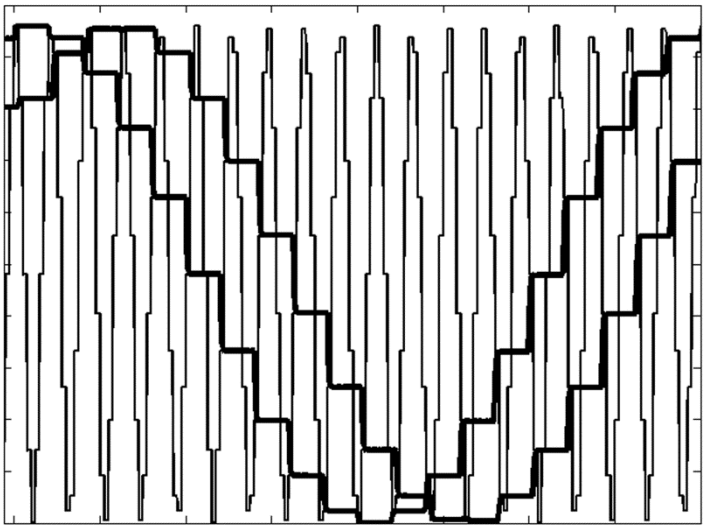
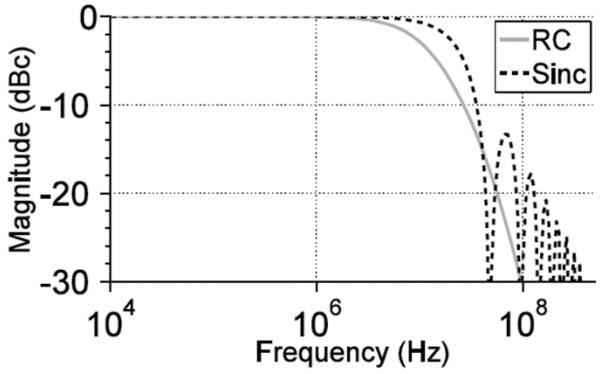


Fig.12. DAC output containing all the 8 polyphase baseband signals (2 of the phases are in bold).



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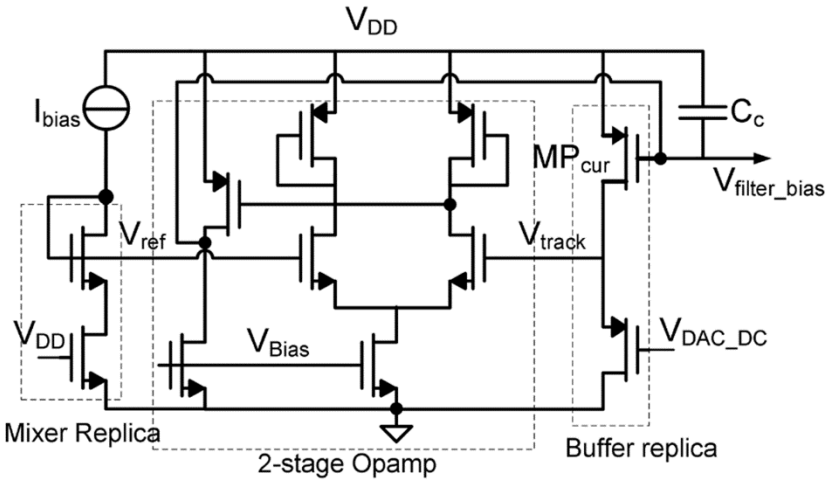

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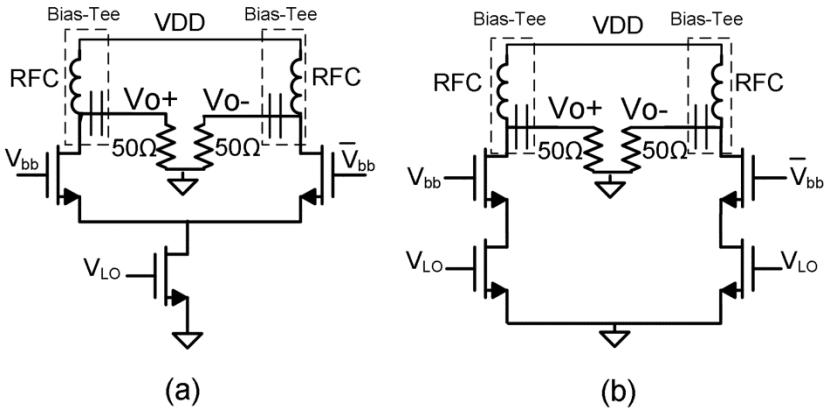

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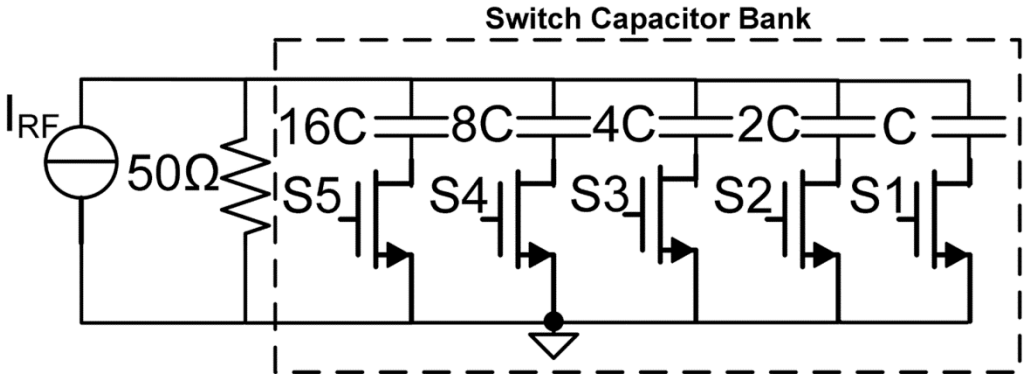


Fig.16. Switch Capacitor bank providing output filter tuning.

Table II. Summary of Calibrations

Initial power-on calibration	Set Bias, compensating for PVT.
	Set full scale of the control DAC.
	Set optimal duty cycle codes over frequency
	Set control bits of RF filter over frequency
Real Time compensation (not implemented)	Monitor transmitter harmonics and adjust the optimal codes.

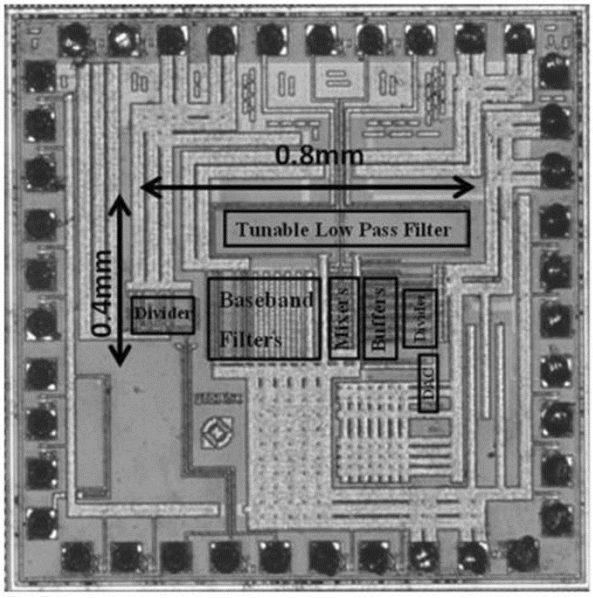
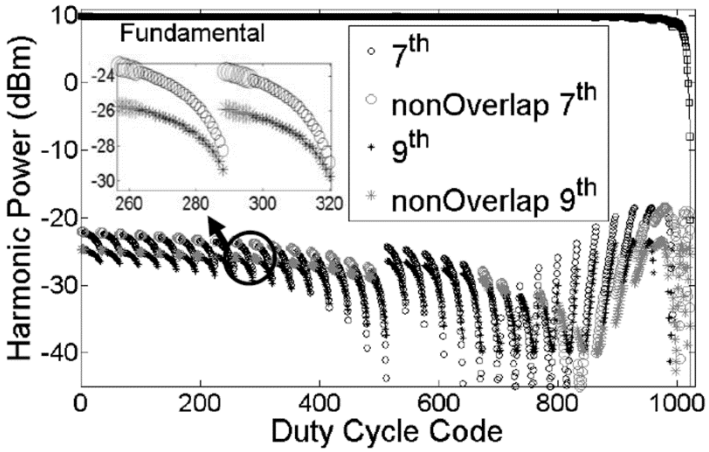


Fig.17. Chip micrograph with active area < 0.32mm^2 in 160nm CMOS



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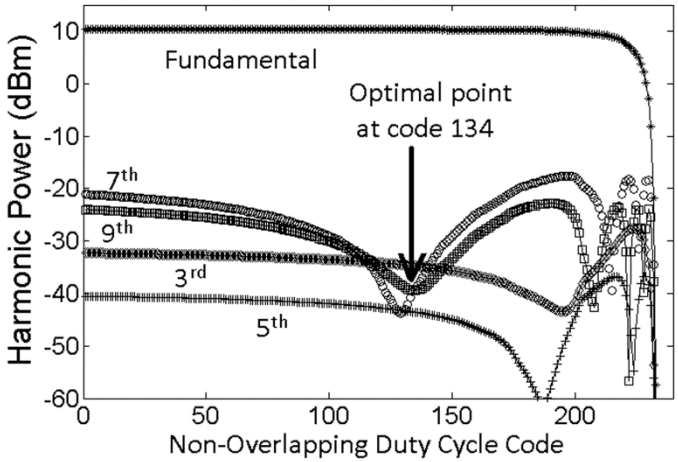

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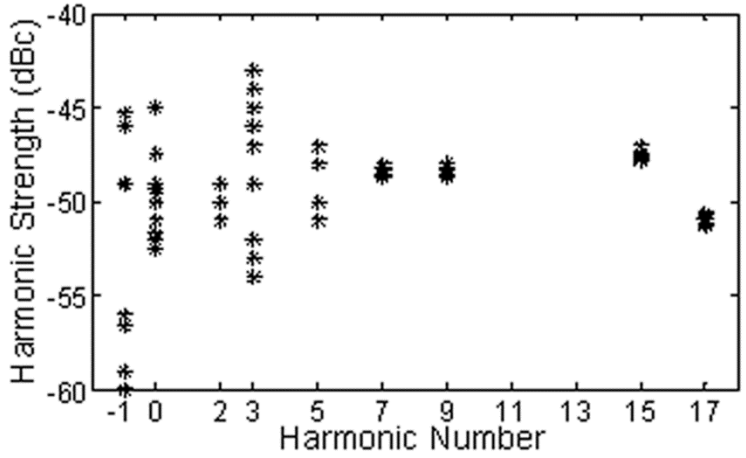
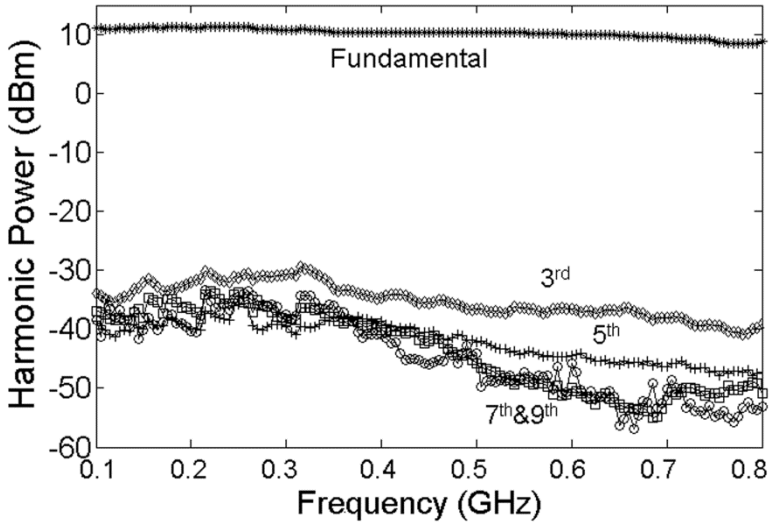


Fig.20. Harmonic Strength measured for 10 chips (LO at 400MHz)



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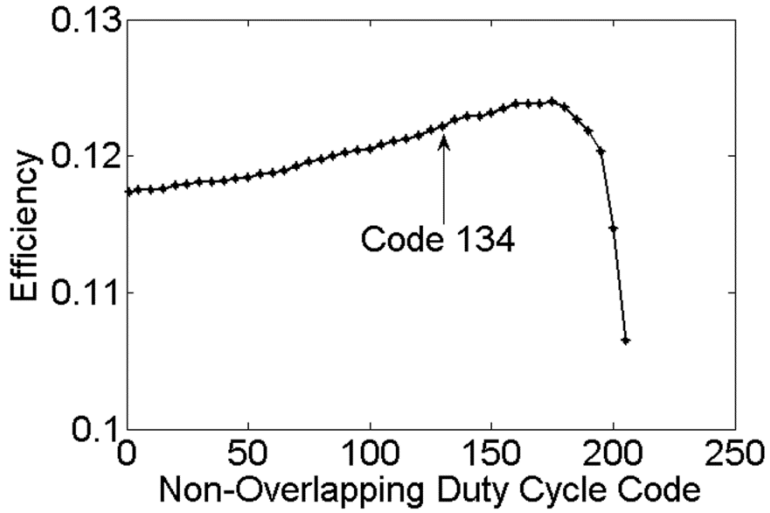

Fig.22. Measured Mixer Efficiency vs. Non-overlapping Duty-Cycle Code

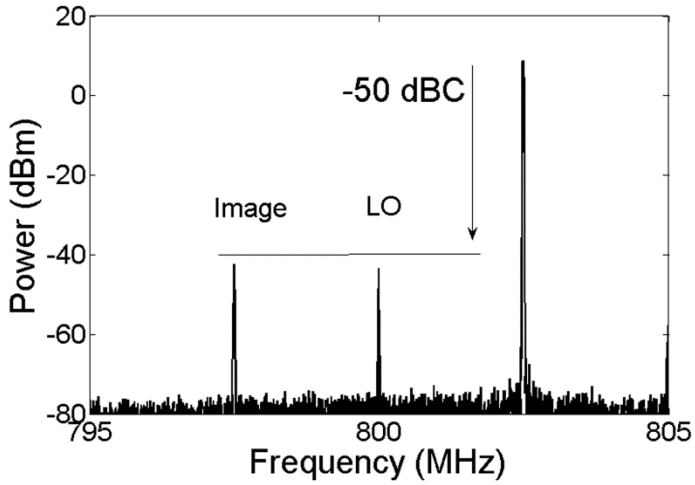

Fig.23. Image and LO Leakage magnitude

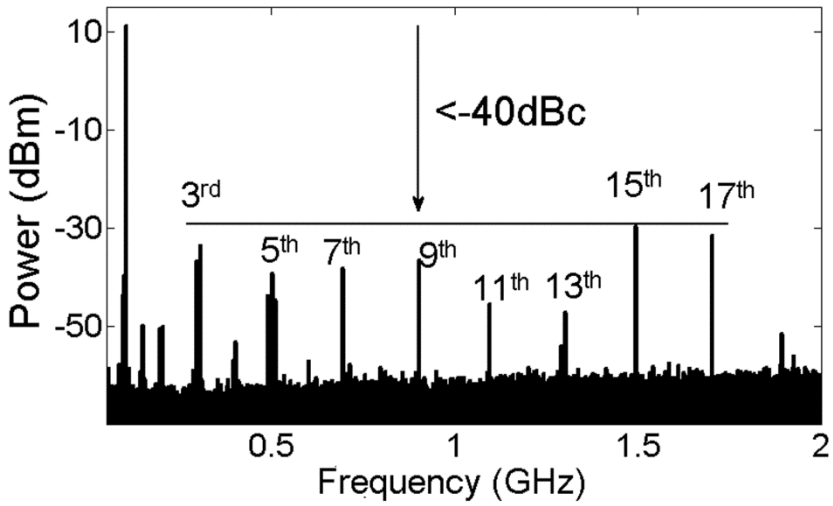

Fig.24. Measured wideband spectrum for 100MHz LO

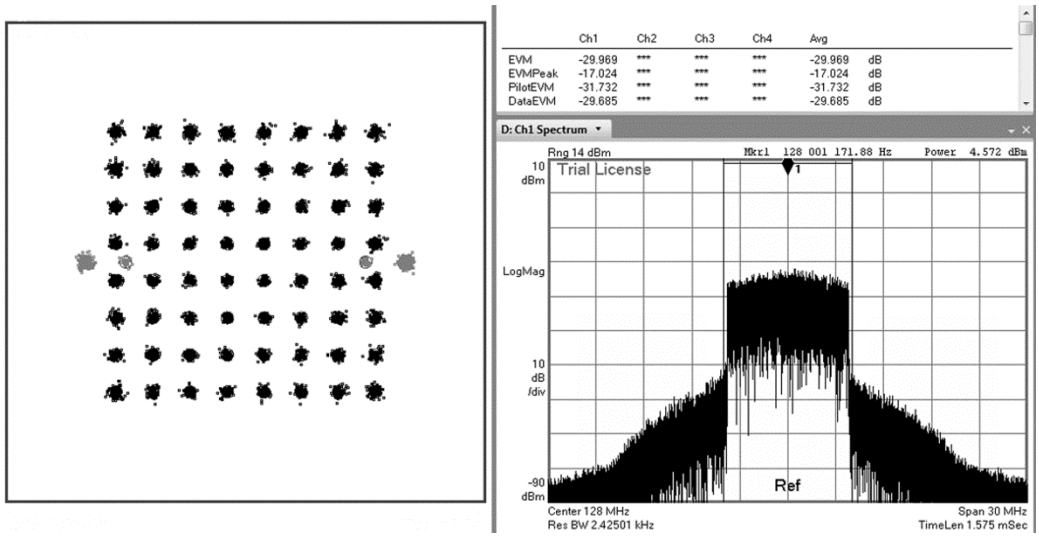

Fig.25 Measured Output Spectrum and Signal Constellation for a 64 QAM OFDM signal.

Table III.Benchmarking to other Harmonic Rejection Transmitters.

	This work		Shrestha [6]	Kim [11]	
Technology Supply voltage	160nm CMOS 1.5 V		130nm CMOS 1.2 V	180nm CMOS 1.8 V	
Frequency	100-800MHz		30-800MHz	54-862MHz	
Harmonic Rejection Principle	**Polyphase 8-path +duty-cycle control + RC-filter**		Polyphase 18-path + 1/3 duty-cycle	Harmonic Rejection Mixer + active gm-C filter + LC notch filter	
Output $P1_{dB}$	**9 ~ 10.8 dBm**		9 dBm	6.4 ~ 8.8 dBm	
Power Consumption Upconverter Mixers + Baseband circuits Multiphase clock	@100MHz 88 mW +30mW +11 mW	@500Mz 88 mW +30 mW +33mW	@? 72 mW NA +156 mW	@100MHz 171 mW 83mW*	@500MHz 131 mW 40mW*
P_{total}	129mW	151mW	228mW	254mW	171mW
Efficiency ($P1_{dB}/P_{tot}$)	**8.7 %**	**6.7%**	<3.5%**	1.7%*	4.4%*
OIP3	18~21dBm		NA	15.9~21.7dBm	
LO Leakage & Image Strength	**<-45dBc**		<-35dBc	<-41dBc	
Strongest Harmonic	<-40dBc		<-31dBc	<-42dBc	
Noise	-153dBc/Hz @ 35MHz		NA	-122dBc/Hz @ 1MHz*	
Area Transmitter Baseband Filter	**0.1 mm^2** **0.2 mm^2**		0.14 mm^2 NA	2.2 mm^{2***} 2 mm^{2***}	

*includes VCO/PLL **No baseband circuits ***Estimated from chip micrograph

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