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Research paper

Process induced poling and plasma induced damage of thin film PZT

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ABSTRACT

This paper treats processing sequence induced changes on PZT. Two kinds of metal-PZT-metal capacitors are compared. The top surface and sidewall of PZT in one kind of capacitor is directly bombarded by energetic particles during ion milling process, whereas PZT in the other kind of capacitor is not. The polarity of plasma charging may depend on the ion milling parameters and influence the self-poling of virgin PZT capacitors. Direct ion bombardment induces a significant decrease of PZT permittivity. The PZT reliability (both RVS and TDDB) at positive voltage worsens because of bombardments of energetic particles; whereas the PZT reliability at negative voltage is not influenced. It indicates that the process induced positively charged defects present in the upper part of the capacitor structure initiate the dielectric breakdown.

1. Introduction

$PbZr_{1-x}Ti_xO_3$ (PZT) material is widely used in piezoelectric MEMS (Micro Electro Mechanical Systems). Its applications include ultrasound medical imaging, robotic insects, inkjet printing, mechanically based logic, and energy harvesting [1]. Further improvement of piezoelectric MEMS requires an increased integration density and a decreased feature size [1,2]. Dry etching is more widely used than wet etching because of its anisotropic and accurate pattern transfer for PZT, especially for a small feature size [3]. Plasma induced damage of PZT during dry etching has been reported by several authors [4–13]. Notwithstanding the benefits of integration, plasma etching induced dielectric damage may become a more prominent issue with increasing integration density [14–19]. Therefore, it is important to study the effects and mechanisms that cause plasma induced damage in PZT based devices.

Both physical and chemical effects contribute to the detected PZT damage/degradation during plasma etching [4,7,9–11]. The physical effect stems from the bombardment of energetic ions; the chemical effect comes from the contamination of impurities in the plasma. Pan et al. think that the physical effect of ion bombardment is the main reason of the PZT degradation [4]. Stanishevsky et al. find that the impurity in etching gas contribute to the change of PZT chemical composition [7]. Lim et al. propose that residues like ZrCl and ZrF might worsen electrical properties [9]. Jung et al. detect the generation of H—O dipoles due to hydrogen reduction during plasma exposure [10]. Soyer et al. show a surface layer developed during plasma etching which contains fluorine and has poor electrical properties [11].

In case of pure ion etching, the chemical effect on PZT degradation during etching could be eliminated. In addition, the particle bombardment is assumed to be primarily responsible for the etching [6]. By using ion milling, it is possible to etch a global structure including several materials without having to change the etching gas, which is beneficial for MEMS applications [6]. Therefore, Ar ion milling is chosen for patterning of PZT capacitors for this study.

The PZT damage/degradation caused by physical effect of ion bombardments can manifest itself by the increase of surface roughness, shift of the hysteresis loop, decrease of permittivity, decrease of remnant polarization, and increase of coercive fields [6,8,13]. Soyer et al. study the PZT damage as a function of ion milling parameters [6]. The PZT grain boundaries contain more Pb than PZT bulk. The etching rate of Pb oxide is higher than Ti/Zr oxide. Thus PZT grain boundaries are preferentially etched and the PZT surface roughness increases [6]. The shift of the hysteresis loop indicates the generation of an internal electric field, which may correspond to the charge accumulation and releasing at the top electrode-PZT interface [6]. A damaged layer at the PZT surface (or sidewall) becomes non-ferroelectric due to the ion bombardments. The total capacitance is then the remained ferroelectric capacitance connecting in series (or in parallel) with the non-ferroelectric capacitance. Since the non-ferroelectric layer has much smaller

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permittivity than ferroelectric PZT, the total capacitance (thus the equivalent permittivity) decreases during the ion milling process [6,8,13]. The formation of a non-ferroelectric layer causes a reduction of the ferroelectric zone; thus it also explains the reduction of the remnant polarization. The pinning between the damaged layer and the undamaged PZT layer contributes to a loss of mobility of domain walls, resulting in an increase of coercive fields [6,13].

Besides the change of PZT properties mentioned above, the physical ion bombardments also influence the aging performance of PZT. Yang et al. also find that the clamping from the substrate is reduced by etching. The clamping from the substrate produces deep potential wells which prevent part of the spontaneous polarization to switch. The damaged PZT sidewall/surface produces shallow potential wells. The domains can be exited out of the shallow potential wells at high electric field, which increases polarization and worsen aging performance [13]. An increase of leakage current because of plasma etching is also detected in [9,12]. Some people find that the plasma etching induced PZT damage can be partly recovered by annealing [6,9].

However, the dielectric breakdown of PZT damaged by plasma etching is not studied in detail. To this purpose, in this paper, we compare two kinds of PZT capacitors processed in parallel, only one of them being directly damaged by ion bombardment. Except for ion bombardments, we also study the influence of plasma charging on the virgin PZT capacitors, which is similar to the antenna effect in industrial IC processes [19]. The ramped voltage stress (RVS) breakdown and time dependent dielectric breakdown (TDDB) of these two kinds of PZT capacitors are compared.

2. Materials and methods

In the present work, we simultaneously fabricate two kinds of metal-insulator-metal (MIM) PZT capacitors on TiO_2 terminated (001) oriented $SrTiO_3$ (STO) substrates. The schematic cross-section of the two kinds of PZT capacitors is shown in Fig. 1. Both kinds of capacitors have 80 nm thick of $SrRuO_3$ (SRO) bottom electrodes, and 800-nm-thick epitaxial $PbZr_{0.37}Ti_{0.63}O_3$ (PZT) thin films with (001) orientation. The PZT layer is deposited by pulsed laser deposition using a KrF Excimer laser (Lambda Physik, 248 nm wavelength) at a laser fluency of 2.5 J/cm^2, substrate temperature of 600 °C, pure oxygen pressure of 0.1 mbar, target-substrate distance of 6 cm, and 10 Hz repetition rate. The SRO electrode is deposited as in [21]. More fabrication detailed are found in [28].

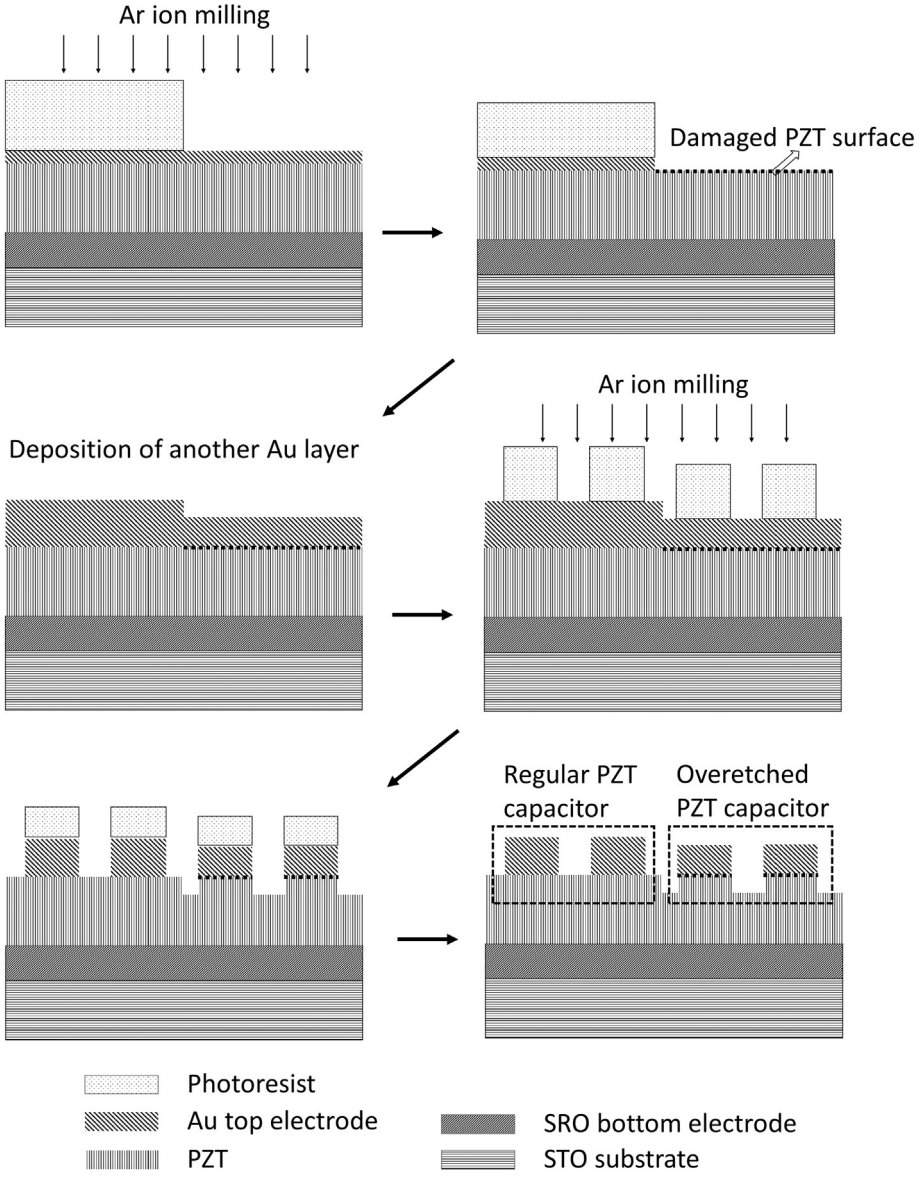

Fig. 1. Schematic cross-section of two kinds of PZT capacitors in main process steps.

The Au top electrode layer is deposited by sputtering. The square top electrode is defined by photolithography and then etched by Ar ion beam milling. A neutralizer is used during ion milling; so extra electrons are generated around the sample to compensate charges of Ar ions.

Firstly, a 20 nm Au layer is deposited and patterned by ion milling into four 4×4 mm^2 areas on the sample. The PZT outside the 4×4 mm^2 areas is also slightly exposed to the ion beam. After acetone clean, another 80 nm Au layer is deposited and patterned by ion milling into an array of 100×100 μm^2 squares across the sample (To be noticed: the latter ion milling uses larger neutralizer current and smaller ion beam current than the former ion milling). During the ion milling of this patterning step, the 20 nm gold film is also removed (unless where part of the 100×100 μm^2 squares). The photoresist is also removed by acetone. This results in two kinds of capacitor structures: 1) the regular capacitors situated inside the 4×4 mm^2 areas with a top electrode of 20 + 80 nm Au; and 2) the overetched capacitors outside the 4×4 mm^2 areas with a top electrode of 80 nm Au. Due to the simultaneous ion-milling processing the latter devices are overetched into the PZT, while for the former devices the PZT is only lightly exposed to the ion beam, as shown in the schematic cross-section in Fig. 1. The top electrode-PZT interface of the latter devices is rougher and more defective than that in the former devices, because of the first ion milling process. These two kinds of capacitors are made on the same wafer, have the same geometry and consist of the same materials.

3. Measurement results

All the electrical measurements in this paper are conducted by using a Keithley 4200 SCS at 150 °C in dry nitrogen ambient. The bottom electrode and chuck are grounded in all the measurements.

For low-field current-voltage (*I-V*), DC bias is applied to the top electrode using sweeps from zero to +8 or −8 V (as indicated by the arrows in Fig. 2) with a voltage step of 0.5 V. The timing of the current measurement is critical for detection of the PZT switching current. The 4200 instrument measures current during a time interval determined by the sweep mode. There are three parameters in each sweep mode: delay factor, filter factor and A/D integration time. In the presented study, we chose “quiet mode” operation. In this mode, the delay factor is 1.3; filter factor is 3; A/D integration time is based on the number of power line cycles, which is 16.67 ms for 60 Hz line power [32]. This long integration time is necessary to obtain an accurate current reading in the 100-pA regime.

Two other factors also determine the overall timing of this measurement [32]. The instrument will observe a certain (unpredictable) settling time when bias conditions change. The settling time can be reconstructed from the overall sample-to-sample time interval, which is about 0.8 s in the measurements reported here (The long settling time indicates a rather slow response of the dielectric stack to a changing bias, as discussed later). After this built-in settling time, a user-defined additional waiting time (termed sweep delay) can be added between instrument settling and the measurement period.

The *I-V* curves of both kinds of virgin PZT capacitors are shown in Fig. 2. For the regular PZT capacitor (with 80 + 20 nm Au top electrode), a current spike is detected at negative voltage but not at positive voltage. For the overetched PZT capacitor (with 80 nm Au top electrode), it is the opposite: a current spike appears only during positive voltage sweep. In all cases, the current spike will not appear if we repeat the *I-V* measurement in the same direction.

For small-signal capacitance-voltage (*C-V*) measurements of virgin capacitors, a DC bias is applied to the top electrode from +8 V to −8 V then back to +8 V (as indicated by the arrows in Fig. 3a) with a voltage step of 0.5 V. The capacitance-frequency measurement shows that both two kinds of PZT capacitors show a stable capacitance from 5 kHz to 4 MHz. Thus we choose AC voltage of 30 mV at 20 kHz for the small-signal *C-V* measurements. For both regular and overetched capacitors, the *C-V* curves show a butterfly shape. The capacitance peaks appear around the coercive voltages. Pintilie et al. show that the capacitance peaks in the butterfly-shape *C-V* curves directly relate to switching of ferroelectric polarization caused by the change of DC bias [31]. The capacitance of the regular PZT capacitor is larger than the overetched PZT capacitor, as shown in Fig. 3a. The column figure of capacitance at DC bias of 0 V in Fig. 3b also clearly show the difference between two kinds of capacitance: all the measured regular capacitors

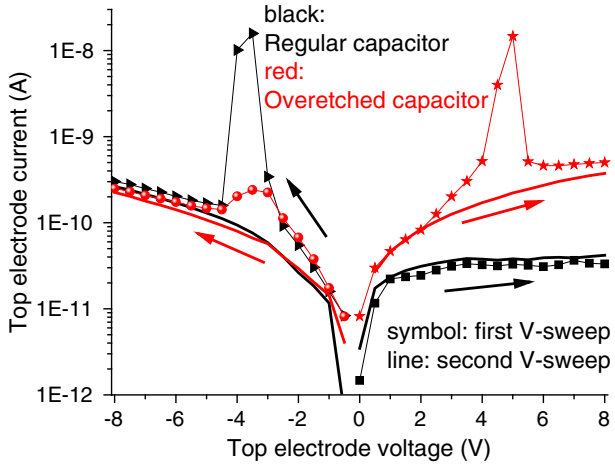

Fig. 2. Low field *I-V* curves of both kinds of virgin PZT capacitors; arrows indicate the directions of DC bias sweep; the current direction depends on the applied voltage, the absolute value of current is shown in the figure.

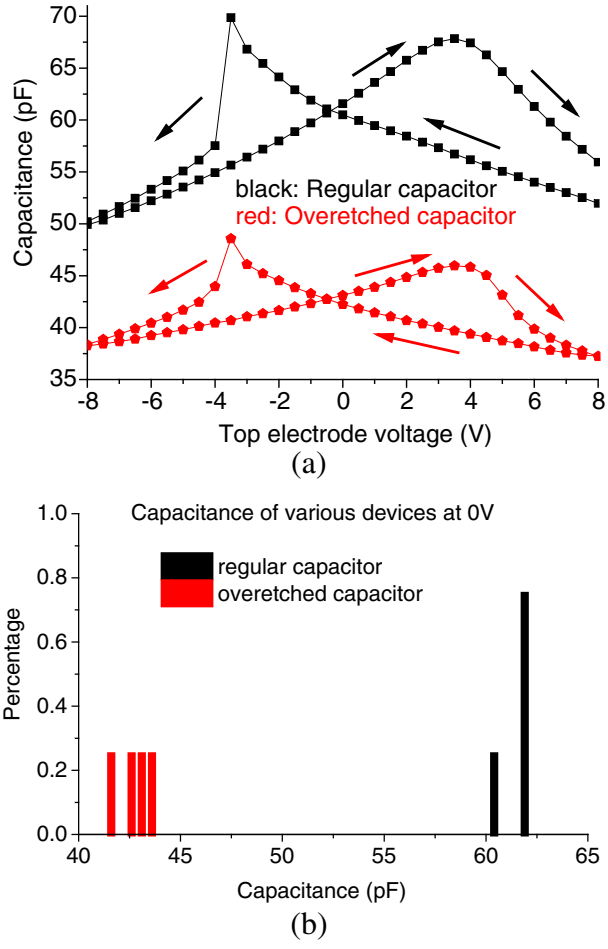

Fig. 3. (a) small-signal *C-V* curves of both kinds of virgin PZT capacitors; arrows indicate the directions of DC bias sweep. (b) Column figure of capacitance at DC bias of 0 V.

are above 60 pF and all the measured overetched capacitors are below 45 pF.

The ramped voltage stress (RVS) breakdown and time dependent dielectric breakdown (TDDB) of the two kinds of capacitors are also compared. For RVS measurement, a ramped voltage from 0 to ±200 V is applied to the top electrode, and breakdown voltage is measured. The voltage ramp rate is about 0.2 V/s. It slightly varies due to the measured current. The larger the measured current is, the higher is the voltage rise rate [32]. At negative stress voltage, there is no significant difference between these two kinds of PZT capacitors. However, at positive voltage, the regular PZT capacitor has larger RVS breakdown voltage, as shown in Fig. 4a.

The TDDB measurements also clearly show the reliability difference between regular and overetched capacitors at positive voltage. For TDDB measurement, a constant +70 V is applied to the top electrodes of two groups of PZT capacitors, and breakdown time of each capacitor is measured. The Weibull distribution is used for the statistical analysis of TDDB measurement, as shown in Fig. 4b. The two kinds of capacitors have similar Weibull shape parameters, which are both smaller than 1. This low value indicates that defects play an important role in the measured PZT breakdown. Compared with the overetched capacitor, the regular capacitor has larger Weibull scale parameter, indicating a statistically longer breakdown time.

4. Analysis and discussion

Switching current accompanies the large-scale switching of ferroelectric domains, which appears around the coercive fields [22]. Waser et al. mention that the switching times of ferroelectric domains in PZT are 1 to 10 ns [29]. Nie et al. report switching times in single crystals and in thin film PZT varying from nanoseconds to hundreds of seconds [24]. For the epitaxial PZT film, the switching current is a sharp spike at mA level in the *I-V* curves measured at 1 kHz [30]. Therefore, it is possible that our *I-V* measurement does not detect all the switching current, but is fast enough to detect part of the switching current besides the leakage current of the PZT layer. Nevertheless, for the present study the quantification of the total switching current is not necessary; what matters is whether it is present or not in a certain sweep.

We think that the switching current appears as a current spike in the low-field *I-V* curves in Fig. 2. If the voltage sweep in the *I-V* measurement is slow, a lower fraction or none of the switching current will be captured, resulting in a decrease or disappearance of the current spike in the *I-V* curve. Thus we increase the sweep delay to 10 s for the low-field *I-V* measurements of virgin capacitors. As shown in Fig. 5, the current spike disappears when the sweep delay increased to 10 s. It indicates that the switching time of the studied PZT is shorter than 10 s.

If the PZT layer is not poled, we should see the switching current around both the positive and negative coercive fields. If the PZT is positively, respectively negatively poled, the current spike should not show at positive, respectively negative coercive fields. Therefore, according to the *I-V* curves of virgin PZT capacitors, the regular capacitors are positively poled and the overetched capacitors are negatively poled during processing. When the *I-V* measurement is repeated in the same direction, the switching current does not appear because the PZT has been poled in this direction during the previous *I-V* measurement.

To understand why the two kinds of PZT capacitors are poled in the opposite direction during processing, we study the possible mechanisms of PZT self-poling. The self-bias of a MIM PZT capacitor is one well-studied reason to explain the self-poling of virgin capacitors. The self-bias is mainly induced by the lattice mismatch between the bottom electrode layer and the PZT layer [20,23]. A strained layer is formed in PZT next to the bottom electrode. The strain is relaxed by dislocation, and accompany by generation of charged defects [20]. The charged defects could be an extrinsic mechanism of self-bias; the strain gradient could be an intrinsic mechanism of self-bias [20]. The strain gradient makes the strained PZT layer a non-switchable polar layer, as a result, the direction of polarization in the switchable PZT layer prefers to be the same as the non-switchable PZT layer [23]. In our study, the two kinds of capacitors have different top electrode-PZT interfaces, and exactly the same bottom electrode-PZT interface. The top electrode-PZT interface hardly influences the self-bias, so we expect the same lattice mismatch and dislocation effect, resulting in PZT self-poling in the same polarity. Therefore, we do not think the PZT self-bias can explain the difference between virgin regular and overetched PZT capacitors in low-field *I-V* curves.

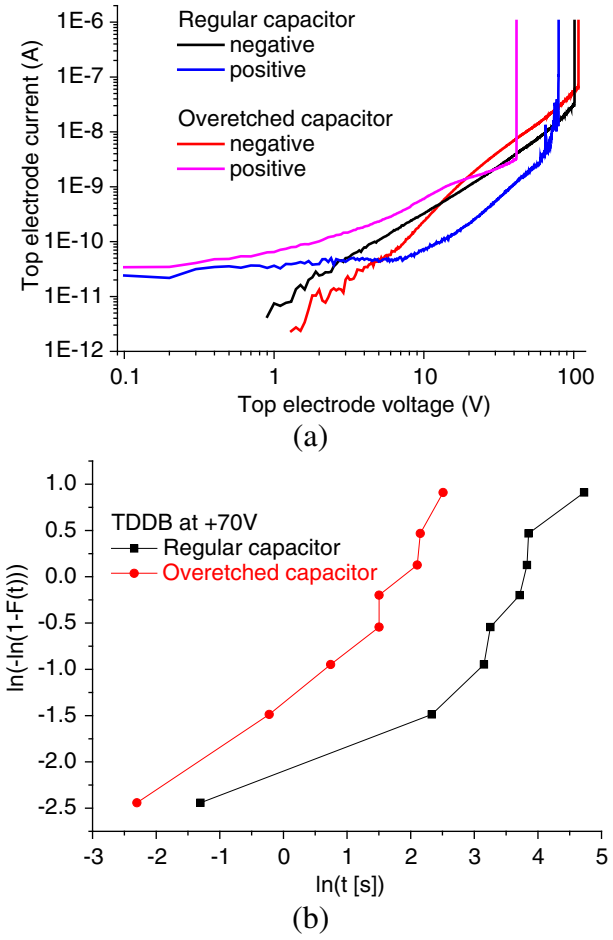

Fig. 4. (a) RVS and (b) TDDB results of two kinds of PZT capacitors.

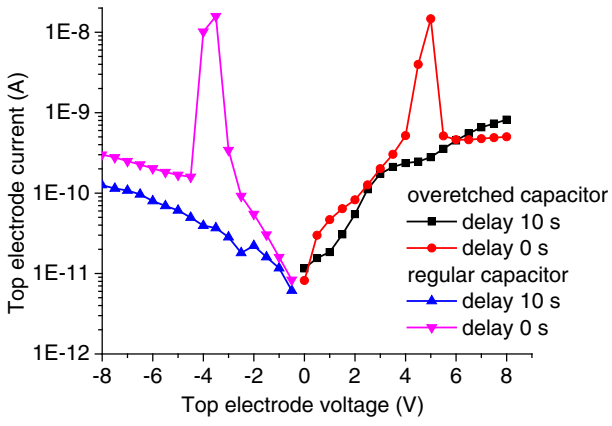

Fig. 5. Compare low-field *I-V* curves measured in two different sweep delay conditions; absolute value of current is shown in the figure.

Another possible reason of PZT self-poling is the plasma induced charging. Common origins of plasma induced charging are electron shading effect or spatial non-uniformity of plasma potential [19,27]. Specifically, electron shading effect means that the negatively charged photoresist repels the light electrons in case of etching a large aspect ratio pattern. Therefore, compared with the electrons, the positively charged ions more easily reach the electrode being etched, resulting in a positively charged electrode [16,19]. The trench aspect ratio of the sample studied in this paper is small enough to avoid an electron shading effect [16]. During overetching of low aspect ratio patterns, it is also possible to detect negative charges on the electrode being etched, which is called extended electron shading [16,19].

Spatial Non-uniformity of plasma potential means that there is always a potential difference towards the wafer and different transport properties of electrons and ions. Therefore, a net charging is likely to occur at the wafer surface [14]. The global potential difference relates to the global non-uniformity of plasma density or spatially imperfect neutralization of the ion beam [26]. During the ion milling process, positive charging is mainly caused by the high energy ion beam and background gas ions; negative charging is mainly caused by the electron shower generated by the neutralizer and plasma electrons [26]. The polarity of net charging may relate with the ion milling parameters, which can be either positive or negative [25,26].

A possible explanation of the *I-V* curves of the two kinds of PZT capacitors is given below. The four 4×4 mm^2 metal areas are positively charged during the first ion milling process and the 100×100 μm^2 square electrodes are negatively charged during the second ion milling process. The regular PZT capacitors are inside the 4×4 mm^2 areas and are positively poled during the first ion milling. During the second ion milling, the negative charges on 100×100 μm^2 electrodes are compensated by the positive charges on the 4×4 mm^2 metal areas, and do not influence the PZT of the regular PZT capacitors. The overetched PZT capacitors are outside the 4×4 mm^2 metal areas thus are negatively poled. Further experiments are needed to study the relation between ion milling parameters and net charging polarity. If the net charging is not compensated in time, it may gradually influence the properties of PZT underneath.

Besides the charging effect, the ion milling process also directly influences the PZT properties as described in the introduction. The damaged layer on upper surface of PZT in overetched capacitor is marked by dashed lines in Fig. 1. This damaged PZT layer may have lower permittivity than the undamaged PZT. The thickness of undamaged PZT is also reduced because of this PZT surface damage. Thus the permittivity of overetched PZT capacitors could be greatly decreased. The PZT damage at the sidewall could further worsen the permittivity decrease of overetched PZT capacitors. But we believe that the main damage is from the ion bombardment on PZT top surface, because the thickness of the etched sidewall is only about 20 nm. The PZT in regular capacitors is protected by the Au metal layer. Although the ion bombardments may also affect PZT in the regular capacitor through the influence on the top electrode-PZT interface, this influence on PZT is much less than that caused by direct ion bombardments. Therefore, the permittivity of regular PZT capacitors may not change much, and is much higher than the permittivity of overetched PZT capacitors, as shown in Fig. 3a.

The damaged layer is believed to be caused by the structural defects generated by ion bombardments [6,8,11–13]. The bombardments by energetic particles may induce lattice dislocation, bonding disruption, stress modification and plasma species permeation, resulting in defects generation [12]. We speculate that process induced positively charged defects initiate the dielectric breakdown. Those defects are probably present in the upper part of the overetched PZT capacitors, but not in the regular PZT capacitors. At negative voltage, such species are rapidly compensated with electrons and hence do not influence the reliability of PZT underneath. Therefore, we only observe significant reliability difference between regular and overetched PZT capacitors in RVS and TDDB measurements at positive voltage as shown in Fig. 4.

5. Conclusion

This paper shows that the processing sequence changes the PZT properties and influences the PZT reliability. By comparing the regular and overetched PZT capacitors, it appears that direct ion bombardments of the PZT surface may cause great PZT degradation/damage. When the PZT is protected by metal, the ion bombardment maybe still cause PZT degradation/damage through modification of the metal-ferroelectric interface, but the PZT degradation/damage is probably much slighter than that in case without metal protection.

The plasma charging generates net charge on the top electrode during fabrication. This creates an electric field across the PZT film, which may lead to process-induced poling of the virgin PZT capacitor. The polarity of the net charge depends on the ion milling parameters. The ion milling settings should be modified to reduce the net charge accumulating on the surface, because the plasma induced charging during ion milling may damage the PZT and might even trigger a dielectric breakdown when the PZT thickness decreases to a certain value.

The ion milling process probably generates positively charged defects in the upper part of the PZT capacitor when the energetic ions directly bombard on PZT. At negative voltage, such species are rapidly compensated with electrons and hence do not influence the reliability of PZT underneath. At positive voltage, such species could move into PZT underneath and initiate the dielectric breakdown. Thus applying negative voltage on top electrode of the PZT capacitors may be one feasible way to reduce the influence of plasma etching induced defects. Further study is required to investigate what kinds of defects are generated during ion milling and how they influence the PZT reliability.

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