Comb Capacitor Structures for On-Chip Physical Uncloneable Function

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***Abstract*—Planar inter-digitated comb capacitor structures are an excellent tool for on-chip capacitance measurement and evaluation of properties of coating layers with varying composition. These comb structures are easily fabricated in a single step in the last metallization layer of a standard IC process. Capacitive coupling of these structures with a coating layer is modelled based on the electric field distribution to have a detailed understanding of contributing capacitance components. The coating composition is optimized to provide maximum spread in capacitance values of comb capacitor structures. This spread in measured capacitance values can be used to implement a physical uncloneable function (PUF). A PUF is a random function which can be evaluated only with the help of a physical system. We present an on-chip capacitive PUF for chip security and data storage in which the unlock key algorithm is generated from capacitors which are physically linked to the chip in an inseparable way. The strength of this key increases with the spread in capacitance values and measurement accuracy.**

***Index Terms*—Comb capacitors, physical uncloneable function (PUF), postprocessing, security coating.**

I. Introduction

To meet the increasing demands and performance requirements microelectronic industries have to deliver complex technological solutions which require the input and or storage of personal and confidential information. For example, a smart card is a simple plastic card with an integrated chip equipped with a microprocessor and a memory to save and process information. Secure storage of information in a smart card is a necessity for the user and at the same time it is a challenge for the manufacturer. Different types of cryptographic encryption algorithms are implemented depending on the security level of the chip. Any physical attack on the smart card chip can be prevented by the use of an optically opaque and chemically inert security coating layer over the chip. This coating acts as a dielectric layer for the comb capacitor structures in which the measured value of capacitance depends on the presence and composition of the coating layer. Comb capacitor structures are for instance studied for applications like humidity sensors or gas detectors [1], [2] where the principle employed is the change in capacitance value with dielectric constant of the layer applied on top of these structures. Adding functionalities on top of metallization layers of a finished chip through extra layers is called postprocessing. For sensing applications the change in properties of the postprocessed layer (which may or may not be CMOS process based) with the measured parameter needs to be sensed and converted to measurable parameters. In this paper, an aluminum phosphate-based coating is applied as the postprocessed layer on top of the chip. This coating layer is hard, opaque, and relatively chemically inert and it is used as the first security measure to prevent physical attacks to the content of the chip. The advantages of this type of system are the relative simplicity of the measurement and the easy processing steps. At the first instance, the presence of the coating can be sensed by the comb capacitor structures. The composition of this postprocessed layer is varied by changing the composition of TiO_2 particles (contributing to the effective dielectric constant of the layer) and conducting TiN particles (as floating electrodes in the layer). This results in increased capacitance values with a large spread. This spread in capacitance values can be utilized as an additional security measure for on-chip data storage. This is implemented by a physical uncloneable function (PUF) function from the measured capacitance values to generate for example an access key to the chip. This type of PUF is called capacitive PUF or coating PUF (c-PUF), of which the schematic is shown in Fig. 1. PUF is a function that is realized by a physical system, such that the function is easy to evaluate but hard to characterize, model, and reproduce. PUF's were first introduced by Pappu *et al.* [3] and different variations in PUFs were presented, depending on the type of the key generation system used [4], [5]. To have larger information density the range of measured values of capacitance should be maximized. To achieve this, the comb structures have been modelled based on the electric field distribution between the combs and through the coating layer. The uncloneable nature of the security coating together with the comb structure will be elucidated. The properties and function of the different particles in the aluminum phosphate based coating matrix are evaluated. Based on these optimizations a physical model is proposed for increase and spread in the capacitance values for comb structures.

II. Test Structure Fabrication

The comb capacitor structures fabricated on the chip are as shown in Fig. 2(a). These structures have two interlinked finger-like metallic combs of equal height and width. Across the two combs a capacitance is established, the variation of which is used to analyze the coating layer. The advantages of using the comb structures are as follows:

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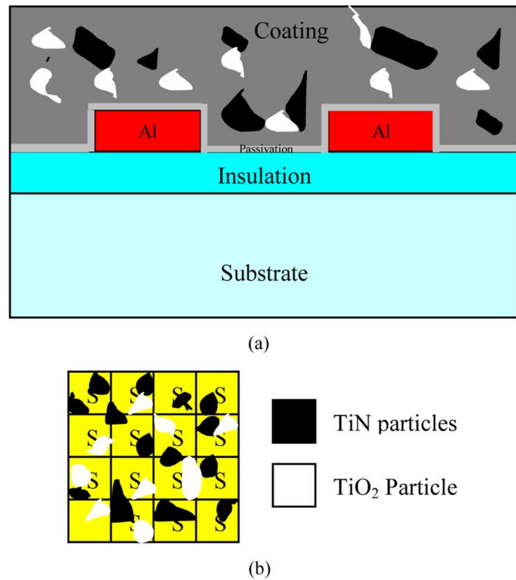

Fig. 1. (a) Schematic cross section of a coating PUF with particles. (b) Array of sensors.

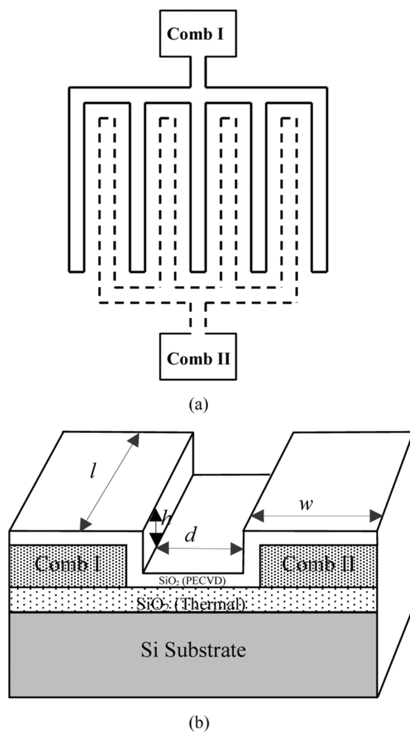

Fig. 2. (a) Comb capacitor structures. (b) Approximated parallel line model for the comb structure on silicon substrate.

1) easy processing in one single metal layer, usually the last metal layer;
2) capacitance optimization with coating is relatively simple by varying length, width, or distance between combs.
3) these structures have a significant amount of fringe capacitive coupling resulting in a larger variation in the measured capacitances with changes in the post-processed coating layer.

These comb capacitor structures are fabricated on boron-doped silicon substrates. The structures are isolated from the silicon substrate by a 1.5-μm-thick insulating layer of thermal oxide grown at 1100 °C. On top of this oxide layer a 1-μm-thick aluminum layer is formed by sputtering, which is subsequently patterned by lithography to form the comb capacitor structures. Over this patterned aluminum layer a 50-nm SiO_2 passivation layer is formed by plasma-enhanced chemical–vapor deposition (PECVD) at 400 °C to prevent chemical reaction between the postprocessed layer and the metallic comb structures. The different postprocessed layers are made from a liquid precursor (aqueous mono aluminum phosphate) into a matrix of aluminum-meta-phosphate (AMP) [6] with inclusion of TiO_2 (dielectric particles) and TiN (conducting particles). They are formed on top of the chip with an automatic spray coating unit. The layer is annealed at 400 °C for 30 minutes in an N_2 atmosphere. This makes it hard and porous and it binds the included particles in the porous matrix and it results in good adhesion to the substrate.

The capacitance between the combs is measured at room temperature using an HP 4257A Multi-frequency LCR meter by wafer level probing on the bond pads. The dimensions of the comb structure are measured using a Leica INM 100 optical microscope to account for the required corrections in calculations. The thickness of the passivation layer is characterized by a Nanospec 6100, Automated Film Thickness Measurement System. Detailed visual analysis of the structure and dielectric layers with conducting particles is done by scanning electron microscope (XL 40 SEM).

To simplify the capacitance calculations, interlinked comb structures are approximated to be two parallel lines as shown in Fig. 2(b). The height of the structures (h) is fixed to 1 μm. Test structures with four different lengths are available, $l = 1000, 2000, 5000,$ and $10\,000 \mu$m. For each of these different lengths there are structures with different width and distance between the combs (d). The respective widths of the combs are 2, 5, and 10 μm and the distance between the combs is 1, 2, 3, and 5 μm.

III. Electrical Evaluation of Comb Structures

A. Electrical Model of the Comb Structures

The comb capacitor structures fabricated are modelled based on the electric field distribution between the combs and silicon substrate as shown in Fig. 3. Detailed understanding of the measured capacitance involves determination of each of the capacitors in this model. The capacitors formed between the two combs are lateral capacitor (C_l) and lateral fringes $(C_{\mathrm{f1}}, C_{\mathrm{f2}})$. The capacitors C_{s1}, C_{s2}, and C_{s3} due to a thin SiO_2 passivation layer are not considered since the contribution of these capacitors in the capacitor model is negligible. For comb structures with parallel vertical edges, the lateral capacitance per unit length could be estimated by the parallel plate approximation with d as distance between plates. The fringe capacitors arise due to concentration of charges at the corners of the metallic structures. These fringe capacitances are a function of the width of the plates as well as separation between the plates and its value dependence could be modelled as a polynomial of d [7].

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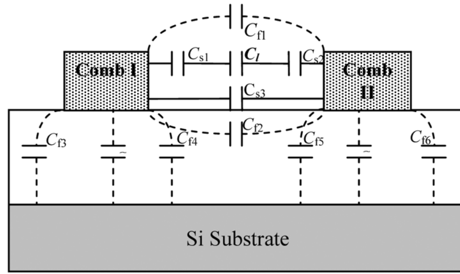

Fig. 3. Approximated comb capacitor model on Si substrate.

This fringe capacitance changes from zero to infinity as the distance between the combs is varied from infinity to zero. For a fixed separation between the combs, charge density induced on each comb due to a finite potential on the other falls gradually with the increasing distance from each other. This gradually becomes insensitive to a further increase on width. Another group of capacitors is the overlap capacitors (C_{a1}, C_{a2}) and overlap fringes (C_{f3}-C_{f6}) from the corners and the vertical faces of each comb to the silicon substrate. These capacitors could be seen as an MOS capacitor due to the stacking of metallic combs on silicon separated by an oxide layer. The overlap capacitance values could not be calculated numerically since the substrate is not held at a fixed potential.

To model the capacitors in the network measurements were done by varying the width and distance between the combs for each structure for a fixed length. The measured capacitance (C_e) includes overlap (C_a), lateral (C_l), and fringe capacitances (C_{f1}, C_{f2}). The capacitor C_a is the combination of overlap capacitors C_{a1} and C_{a2}, overlap fringes C_{f3}-C_{f6}, and the capacitance contribution due to the floating substrate. Equating the capacitance network of the comb structure in Fig. 2 to a parallel resistance-capacitance measurement network, the measured capacitance is approximated [8] as

$$C_e = C_l + C_{f1} + C_{f2} + \frac{C_a}{2}. \quad (1)$$

The approximation made in deriving this equation is that all capacitors in the network are ideal and the impedance contribution from the substrate is zero. In this capacitor model presented, only the value of lateral capacitor is well established. To separate the contribution of different capacitors from the measured capacitance value, measurements are carried out by varying the distance between the combs and by changing width of the combs. In Fig. 4(a), the capacitance is plotted with the reciprocal of distance between the combs. As the distance between combs increases lateral components C_l, C_{f1}, and C_{f2} become negligible and only the overlap component C_a remains. These could be obtained from the intercept of the curve with the capacitance axis. The value of C_a increases with the width of the combs due to an increase in the overlap capacitance values C_{a1} and C_{a2}. Similarly, in Fig. 4(b) the capacitance is plotted with the width of the combs and the curve is extrapolated to zero width.

From the intercept the lateral component C_l, part of C_{f1} and C_{f2}, and the overlap component C_{f4} and C_{f5}, including the substrate capacitance, is estimated. If these intercept capacitance values from Fig. 4(b) are plotted versus the inverse of the distance the lateral component could be eliminated and only the overlap component C_{f4} and C_{f5} including the substrate capacitance remains. By this analysis method, all the different capacitors in the network could be calculated. The application of a postprocessed layer on the comb structures acts like a dielectric layer for the lateral capacitors of the network. The result is a change in the value of these lateral capacitors depending on the dielectric constant of the layer applied. This changes the measured value of capacitance making the comb structures ideal for measurement of a post-processed layer. Change in capacitance measured with and without a postprocessed layer with length of the combs is shown in Fig. 5. Capacitance values increase with a postprocessed layer of dielectric constant of 32. This increase in capacitance is mainly due to the increase in contribution of the lateral capacitance. The capacitance increases with increasing length of the combs due to the increase in lateral area.

The comb capacitance is not only sensitive to the variation in dielectric constant of the layer but also to the variation in the thickness of the postprocessed layer. Fig. 6 shows the variation of the capacitance values with thickness of the postprocessed

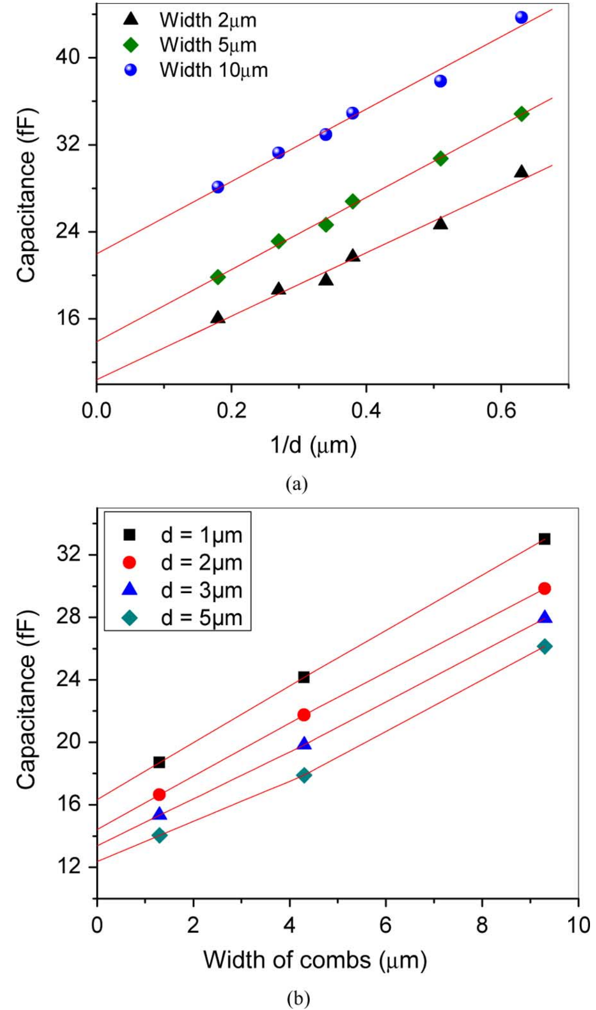

Fig. 4. (a) Capacitance with reciprocal of distance between the combs. (b) Capacitance with width of the combs.

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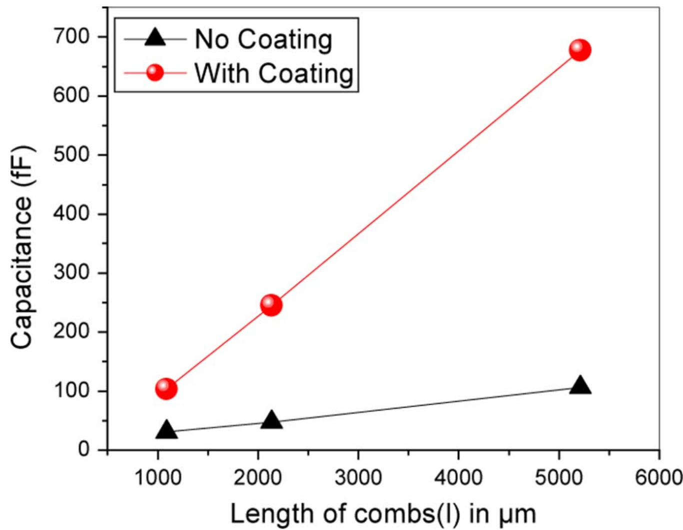

Fig. 5. Comb capacitance with length of structure.

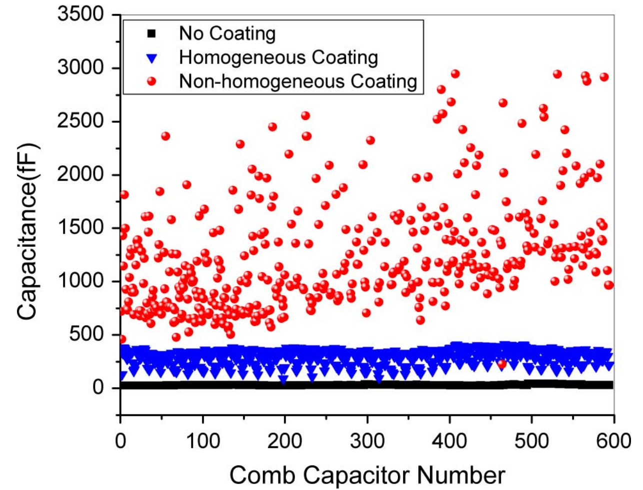

Fig. 7. Capacitance with and without coating over comb structures.

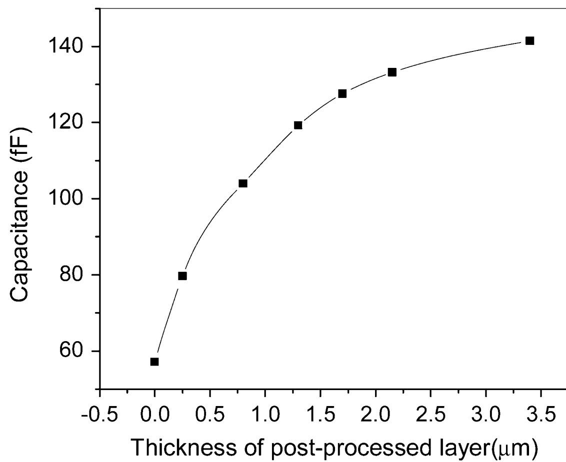

Fig. 6. Variation in comb capacitance with thickness of postprocessed layer.

layer on top of the structures. The capacitance increase with the thickness is due to increase in lateral fringe coupling, which saturates beyond a particular thickness. A further increase in layer thickness has no effect on lateral fringes.

B. Comb Capacitance With Different Coatings

Fig. 7 shows the plot of the measured capacitance value of a large number (600) of identical comb structures for three different situations. The first case is comb capacitor measurement without a processed layer, while for the other two situations the structures have a homogeneous and a nonhomogeneous postprocessed layer on top. The mixing of the uniform sized TiO_2 particles in an aluminophosphate matrix results in a homogeneous precursor for the homogeneous layer. The addition of conducting TiN particles of varying size to this homogeneous precursor results in a nonhomogeneous precursor solution. The size of TiO_2 particles is 300 nm while the size of TiN particles varies from 500 nm to 3 μm. This precursor solution is then spray coated over the comb capacitors and is baked in a furnace to subsequently result in a hard and solid postprocessed layer. The comb capacitance measurements without a postprocessed layer have the lowest mean value of 36 fF with a standard deviation of 5 fF. The spread in capacitance value is due to the variation in the fabrication process and measurement accuracy. Application of a homogeneous layer with relative dielectric constant of 32 results in a mean capacitance value of 212 fF with a standard deviation of 43 fF. This increase in mean capacitance value is due to the increase in lateral capacitance and fringes by the relatively high-k layer over the comb structures. The overlap capacitance remains unaffected. The spread in capacitance value is mainly due to variation in the layer thickness due to the spray coating process.

As shown in Fig. 7, the nonhomogeneous layers have a maximum capacitance value with maximum spread in capacitance values. The average capacitance value with this layer is 1125 fF with a standard deviation of 405 fF. The mechanism attributed to this increase in capacitance is first, the change in lateral coupling due to the presence of conducting TiN particles in the region between combs. This could effectively be seen as a reduction in distance between combs thereby increasing capacitance value. Fig. 8(a) shows an SEM image of conducting particles in nonhomogenous dielectric layer. The presence of these conducting particles enhances the lateral capacitance value by forming a capacitive network between themselves and to the combs as depicted in the SEM image. Second is the creation of an additional coupling between the conducting particles and the Si substrate. The resulting capacitive network with conducting particles in the vicinity of comb structures is shown in Fig. 8(b). Each of these conducting TiN particles creates an additional node in the equivalent capacitance network. The large standard deviation of the measured capacitance values can be understood from geometrical considerations. The size range of the TiN particles is 0.5–3 μm, the thickness of the coating is 3–5 μm and the distance between the metal combs is 1.5–2 μm for the measured structures (not in the SEM image). These TiN particles are incorporated in the dielectric layer in the lateral and vertical direction. This means that they will be distributed in position and

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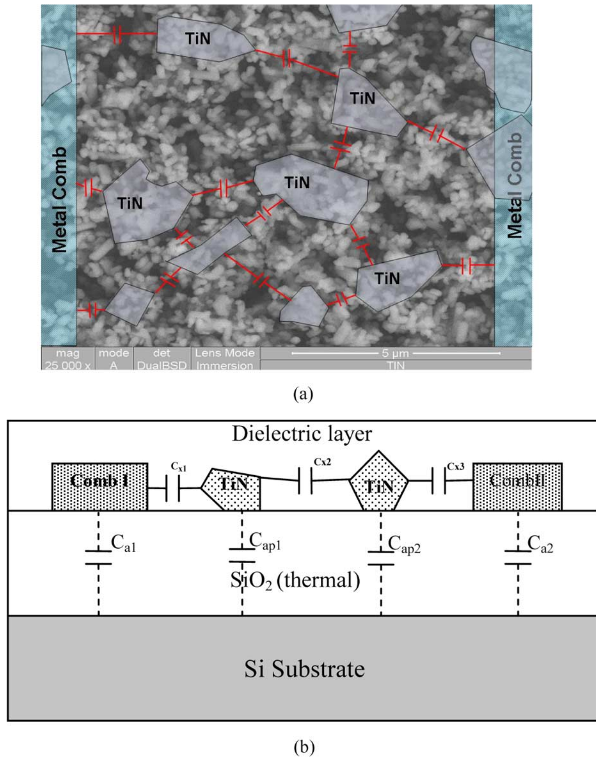
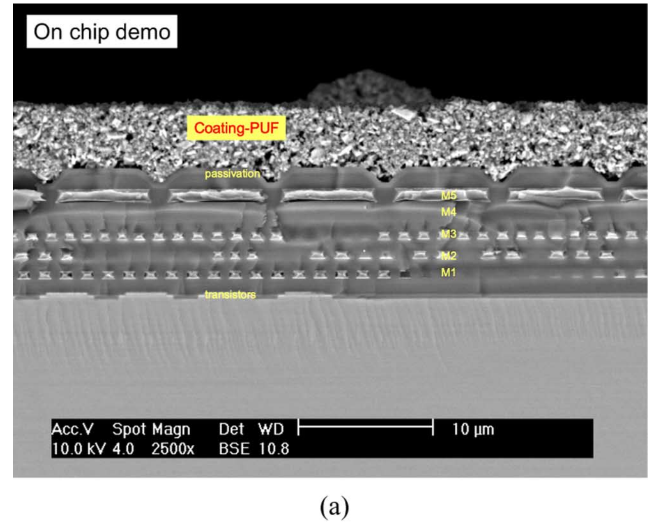
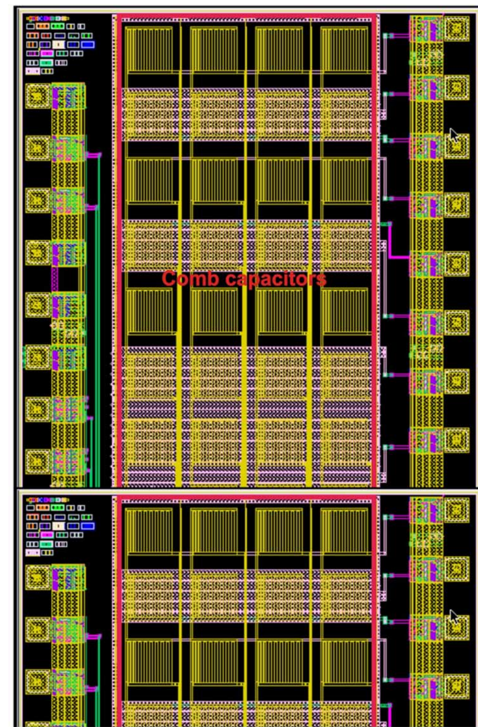


Fig. 8. (a) SEM image of nonhomogeneous coating over the comb structures. (b) Equivalent electrical model.



(a)



(b)

Fig. 9. (a) SEM cross-section of the chip showing the comb capacitor with the coating, (b) Floor plan of the coating PUF Chip.

size, leading to an unpredictable lateral and overlap coupling for each structure.

C. Implementation

These nonhomogeneous layers can be added to a standard CMOS18 process flow to implement the PUF function on the IC. In this section, the application of the coating will be described. A detailed description can be found in the book by *Tuyls et al.*, *Security with Noisy Data* [4]. Fig. 9(a) shows the SEM cross section of the chip showing comb capacitor with the coating and Fig. 9(b) describes the floor plan of the chip showing the array of comb capacitors, interface and control block, and the oscillator block. The upper metal layer of the IC structure is covered with an oxide-nitride passivation layer. The nonhomogeneous coating layer is applied on top of this passivation layer. This coating layer along with the passivation layer protects the IC from moisture and physical attacks. The comb capacitor array directly underneath the passivation layer senses the local presence of the coating layer. There are three main contributions to this measured capacitance: the coating, the oxide/nitride passivation stack, and the underlying interconnection/oxide structure.

The coating PUF capacitances are measured on-chip by means of a switched capacitor relaxation oscillator. High measurement accuracies (effects due to environment, voltage, temperature, and circuit inaccuracies can be eliminated) are reported [12]–[14] for this type of measurement method. A stable current source charges the selected capacitor until a certain threshold voltage is reached. The same current source is used to discharge the capacitor until a second threshold voltage is reached. Then, the whole process is repeated from the start. The frequency of the resulting current oscillation is inversely proportional to the capacitance. The capacitance measurement is done relatively to eliminate environment, voltage, temperature, and circuit inaccuracies. The relative measured capacitance is given as

$$\frac{(C_x - C_0)}{(C_{\text{ref}} - C_0)} \tag{2}$$

where C_x and C_{ref} represent the capacitances of the coated comb structures and a given reference capacitor. C_o is the ca-

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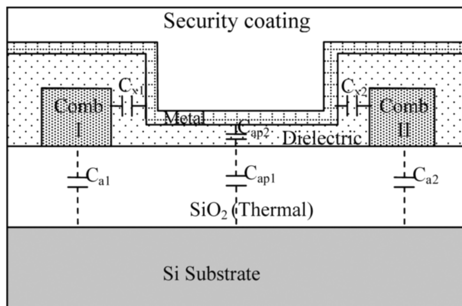

Fig. 10. Capacitor model with continuous metallic layer over comb structures.

pacitor that sets an offset oscillation frequency, which is located at the lower left of the array.

D. Maximum Capacitance

The presence of conducting particles in the region between the combs increases the capacitance value ultimately to a maximum. Fig. 10 shows the structure and the equivalent network with a thin metallic layer formed over comb structures separated by a 500-nm SiO_2 dielectric region. The measurements on these structures result in a mean value of 1746 fF with a low standard deviation. (For all the previous situations the passivation oxide is only 50 nm thick, which is why the maximum capacitance value is still lower.) This increase in capacitance is found to be highest since the metallic region fully determines the measured value of capacitance to C_{x1} and C_{x2} and also an additional coupling from metal layer to Si substrate is created. Application of a homogenous or nonhomogenous dielectric layer over these metal structures has no influence on the measured capacitance value due to shielding by the continuous metallic layer.

IV. Conclusion

The presence and properties of different coating layers are evaluated by capacitance measurements using comb structures. Based on the electric field distribution, an electrical model for the comb structure on silicon substrate with different capacitive components has been described. The different capacitive components are analyzed by varying the dimensions of the comb structure and properties of the coating. Measurements with these structures show that any change in the layer properties (e.g., dielectric constant and inhomogeneity) reveals itself as a significant difference in the measured capacitance values. The inclusion of dielectric (TiO_2) particles and conducting (TiN) particles in the layer modifies the capacitance network. The presence of floating conducting particles in the region between the combs intensifies the capacitive coupling due to the reduction in effective dielectric distance. On one hand, this increase in capacitance value is dependent on the size of the particles on the other hand the capacitor network between the combs is modified depending on the relative position of these particles. The presence of TiN particles of varying size in the dielectric layer results in a larger range in capacitance values, when measured over a large number of comb capacitors. This spread in the capacitance value and the modification in the capacitance network with TiN particles in the vicinity of the comb structures are modelled. This spread in capacitance values can be utilized as a PUF function for on-chip data storage. This is done by the generation of the cryptographic access key from these capacitance values. Ultimately, the capacitance value increases to a maximum by forming a continuous metallic layer over the comb structures. This metallic layer increases the capacitance value by determining the thickness of the dielectric layer while having a lower range due to formation of a fixed capacitor network.

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