RF Circuit Linearity Optimization Using a General Weak Nonlinearity Model

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***Abstract*—This paper focuses on optimizing the linearity in known RF circuits, by exploring the circuit design space that is usually available in today's deep submicron CMOS technologies. Instead of using brute force numerical optimizers we apply a generalized weak nonlinearity model that only involves AC transfer functions to derive simple equations for obtaining design insights.**

The generalized weak nonlinearity model is applied to three known RF circuits: a cascode common source amplifier, a common gate LNA and a CMOS attenuator. It is shown that in deep submicron CMOS technologies the cascode transistor in both the common source amplifier and in the common gate amplifier significantly contributes IM3 distortion. Some design insights are presented for reducing the cascode transistor related distortion, among which moderate inversion biasing that improves IIP3 by 10 dB up to 5 GHz in a 90nm CMOS process. For the attenuator, a wideband IM3 cancellation technique is introduced and demonstrated using simulations.

***Index Terms*—Attenuators, cascode amplifier, IIP3, linearity, circuit optimization, nonlinearity model.**

I. Introduction

IN recent years, the need for RF ICs with demanding performance specifications has been increasing significantly. Low intermodulation distortion is one of the most desirable design targets for the current wireless front-ends. Optimizing RF front-end circuits may be done using brute force numerical optimizers with a proper set of optimization constraints, or can (partly) be done by hand if sufficient design insight is present.

Circuit distortion analyses such as Volterra series have been used to either provide design insights on the RF circuit linearity [1] or to get numerical/symbolic solutions for the behavioral modeling of the front-end [2-4]. To reduce the complexity of Volterra kernels, [5] uses nonlinear system order reduction algorithms to produce compact macromodels based on Volterra series.

As alternative for the Volterra series, in [6] we presented a general weak nonlinearity model that was applied to relatively small RF circuits: the low noise amplifier (LNA). This model can easily be used to derive e.g. the circuit's intermodulation distortion in a compact closed-form expression. Due to the nature of the method, this closed-form expression is a linear combination of a number of nonlinearity coefficients of each MOS transistor and of terminal AC transfer functions. Since the AC transfer functions involve no complex calculations, it is straightforward to utilize the general distortion model for various topologies. Nevertheless, [6] only shows the accuracy benchmarking of this general model for different LNAs while no further circuit design insights are provided.

This paper extends the general weak nonlinearity analysis method in [6] to a number of small RF circuits with four-terminal transistors; the method is applied to explore the design space to optimize RF circuits and to provide design insights. Section II presents the closed-form expressions for the general nonlinearity model. Using this model, we introduce a nonlinearity cutoff frequency that indicates the relative significance of capacitive nonlinearities with respect to resistive terms for MOS transistors. This is used to simplify the general model by removing many insignificant terms from the weakly nonlinear circuit model. Section III and IV discuss insights on the linearity optimization for the cascode common source RF amplifier and common gate LNA. It is shown that the distortion generated by the cascode transistor easily become dominant in the amplifier's overall distortion behavior due to the relatively large output conductance and its associated large nonlinearities. The analytical expressions indicate an IM3 cancellation scheme for amplifiers biased in the moderate inversion region. In section V the model is applied to the analysis and optimization of a CMOS attenuator consisting of two switches and two resistors. It is shown that proper sizing of the two switches leads to a process-robust wideband IM3 distortion cancellation between these two switches. The overall conclusions are summarized in section VI.

II. The General Weak Nonlinearity Model

A. The MOS transistor nonlinearity model

The dominant source of nonlinearity in RF circuits is usually the transistors' nonlinearity. A MOS transistor is a four-terminal device, in which all currents into the terminals and charges attributed to the terminals are nonlinear functions of the voltages across any two terminals. Mathematically the transistor can be modeled as a three-port network with the gate-source, drain-source and bulk-source voltage as the input ports and gate current, drain current and bulk current as outputs for any given DC bias, see Fig. 1. For analytical weakly

Manuscript received June 13, 2011. This work was supported by NXP Semiconductors.

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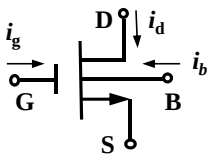

nonlinear distortion analyses, Taylor series have been dominantly used to describe MOS transistor nonlinearity, where typically only the resistive nonlinearity is modeled [1-4, 7-11]. Here we present a complete weak nonlinearity model of the MOS transistor taking into account both the resistive and capacitive nonlinearity, which is given by

$$i_k(t) = \sum_K \left[G_{nml}^{ks} v_{gs}^n v_{ds}^m v_{bs}^l + C_{nml}^{ks} \frac{d(v_{gs}^n v_{ds}^m v_{bs}^l)}{dt} \right] \qquad (1)$$

$K = \{(n,m,l) | n,m,l \in \mathbb{N}; n+m+l \in (1,2,3)\}$ and $k \in \{g,d,b\}$

where

$$C_{nml}^{ks} = \frac{1}{n!}\frac{1}{m!}\frac{1}{l!}\frac{\partial^{(n+m+l)} Q_k}{\partial v_{gs}^n \partial v_{gs}^m \partial v_{gs}^l}\Bigg|_{\substack{V_{gs}=V_{GS} \\ V_{ds}=V_{DS} \\ V_{bs}=V_{BS}}} \quad \text{and}$$

$$G_{nml}^{ks} = \frac{1}{n!}\frac{1}{m!}\frac{1}{l!}\frac{\partial^{(n+m+l)} I_k}{\partial v_{gs}^n \partial v_{gs}^m \partial v_{gs}^l}\Bigg|_{\substack{V_{gs}=V_{GS} \\ V_{ds}=V_{DS} \\ V_{bs}=V_{BS}}},$$

are respectively the capacitive and resistive coefficients. Q_k is the charge attributed to the terminal k (gate, drain or bulk) and I_k is the current into terminal k. For the first order Taylor series terms we have $(n+m+l) = 1$, which implies that a first derivative is taken with respect to just one port voltage. For the second order terms $(n+m+l) = 2$, which means that either one second derivative is used or that two first order derivative are taken with respect to port voltages. In this paper we use only the first, second and the third order terms, for the latter of which $(n+m+l) = 3$. For the drain terminal, the first-order coefficients G_{100}^{ds}, G_{010}^{ds} and G_{001}^{ds} correspond to the linear small signal parameters g_m, g_{ds} and g_{mb} while C_{100}^{ds}, C_{010}^{ds} and C_{001}^{ds} are their capacitive counterparts. The higher order resistive coefficients (G_{200}^{ds}, G_{300}^{ds}), (G_{020}^{ds}, G_{030}^{ds}), and (G_{002}^{ds}, G_{003}^{ds}) describe second-order and third-order dependency of the resistive drain-source current respectively on V_{GS}, V_{DS} and V_{BS} while (C_{200}^{ds}, C_{300}^{ds}), (C_{020}^{ds}, C_{030}^{ds}), and (C_{002}^{ds}, C_{003}^{ds}) are their capacitive counterparts. The other coefficients are the cross-modulation conductive and capacitive terms describing the dependency of drain-source current on either any two terminal or three terminal voltages. These cross-modulation terms are significant in deep sub micron CMOS technologies.

B. Generalized weakly nonlinear analysis

In the circuit example we analyzed in [6], the transistors are assumed to be three-terminal devices with interconnected bulk and source terminals. Here, we assume four-terminal transistors obeying the weakly nonlinear model given in (1). It is assumed that these transistors are dominant in the nonlinear behavior of the circuit with *N* transistors. We assume a two-tone input voltage $V_{\mathrm{IN}}(\mathrm{e}^{j\omega_1 t} + \mathrm{e}^{j\omega_2 t})$ with sufficiently small amplitude (V_{IN}) to ensure circuit operation in the weakly nonlinear region. The voltage swing at each port (v_{gs}, v_{ds} and v_{bs}) of each transistor results in distortion currents ($i_{gs,D}$, $i_{ds,D}$ and $i_{bs,D}$) by that transistor as described by (1). These distortion currents in turn generate a voltage at the ports of all transistors:

$$v_{ks,j} = \sum_{j,p=1}^{N} [E_{gs,p}^{ks,j} \cdot i_{p,D}^{gs} + E_{ds,p}^{ks,j} \cdot i_{p,D}^{ds} + E_{bs,p}^{ks,j} \cdot i_{p,D}^{bs} + F^{ks,j}(\omega_1) \cdot V_{\mathrm{IN}} e^{j\omega_1 t} + F^{ks,j}(\omega_2) \cdot V_{\mathrm{IN}} e^{j\omega_2 t}]$$

where *N* is the number of transistors in the circuit, $E_{xs,p}^{ks,j}$ is the transfer function from the current in port (*x*,*s*) of transistor *p* to the terminal voltage v_{ks} of transistor *j*, and $F^{ks,j}$ is the transfer function from voltage input to port *(k,s)* of transistor *j*, with $k, x \in \{g,d,b\}$. Since (2) is carried out in the frequency domain, (1) is rewritten into an admittance notation, $i^{ks} = \sum_K [Y_{nml}^{ks} v_{gs}^n v_{ds}^m v_{bs}^l]$ with $Y_{nml}^{ks}(\omega) = G_{nml}^{ks} + j\omega C_{nml}^{ks}$. The generated distortion voltages result in additional distortion currents. The recursive dependency of (1) and (2) can be numerically solved by the harmonic balancing technique [7], which is often implemented in simulators. A known issue with harmonic balancing is that oversampling is required to prevent significant aliasing of higher harmonics. For the weakly nonlinear analyses done in this paper, we assume a maximum mixing order of 3: all terms higher than third order are truncated. For weakly nonlinear systems this does not introduce significant errors, while by truncating the terms higher than third order, the number of terms remains finite and the set of equations can be analytically solved.

After truncation of higher order terms, only the terms with fundamental tones contribute to the second-order distortion, while the second-order distortion is proportional to V_{IN}^2; similarly, only the terms with fundamental tones and second-order distortion components tones contribute to the third-order distortion components resulting in the third-order distortion proportional to V_{IN}^3. Now, a next step in the reduction of computational effort is the selection of only the frequency components leading towards the output signal component at the desired frequency (denoted as ω_D). As a result, the set of equations consisting of (1) and (2) can be analytically solved; the distortion at the circuit output is now a linear combination of the distortion contributions of each individual transistor.

$$v_{\mathrm{out}} = \sum_{p=1}^{N} [H_p^{gs} \cdot i_{p,D}^{gs} + H_p^{ds} \cdot i_{p,D}^{ds} + H_p^{bs} \cdot i_{p,D}^{bs}] \qquad (3)$$

where $i_{p,D}^{ks}(\omega_D) = \sum_K \beta_{nml}^{\omega_D} \cdot Y_{nml,p}^{ks}(\omega_D)$ with $\beta_{nml}^{\omega_D}$ the function that selects only the ω_D components from the product of voltages: $\beta_{nml}^{\omega_D} \triangleq (v_{gs}^n v_{ds}^m v_{bs}^l)(\omega_D)$. For IM2 calculations the function $\beta_{nml}^{\omega_D}$ thus is (with *n+m+l=2*):

$$\beta_{nml}^{\omega_{IM2}} = 0.5 \times [n v_{gs}^*(\omega_2) v_{gs}^{n-1}(\omega_1) v_{ds}^m(\omega_1) v_{bs}^l(\omega_1) + m v_{ds}^*(\omega_2) v_{ds}^{m-1}(\omega_1) v_{gs}^n(\omega_1) v_{bs}^l(\omega_1) + l v_{bs}^*(\omega_2) v_{bs}^{l-1}(\omega_1) v_{gs}^n(\omega_1) v_{ds}^m \omega_1] \qquad (4)$$

where *v** denotes the complex conjugate of *v*. The corresponding $\beta_{nml}^{\omega_D}$ for IM3 calculations is somewhat more

elaborate and is given in appendix I. Note that H_p^{ks} is the AC transfer function from the current in port (*k,s)* of transistor *p* to the output voltage and can be easily obtained by small signal analysis.

In summary, since no topology information is involved in deriving (3), the analysis result can be reused in any topology by deriving the topology-dependent AC transfer functions. The presented model transforms the circuit distortion calculation that usually is done by Volterra-series into rather simple AC transfer function calculations using a topology-independent transformation. When this model is used for automatic symbolic analysis of time-invariant weakly nonlinear circuits, only AC symbolic analysis is required.

C. Simplifying the transistor nonlinearity model

The nonlinearity model provides the possibility to further simplify the MOS transistor nonlinearity model given by (1). In (3) the resistive and capacitive coefficients (G_{nml}^{ks} and C_{nml}^{ds}) are combined into $Y_{nml}^{ks} = G_{nml}^{ks} + j\omega C_{nml}^{ks}$. Then a cutoff frequency $f_{nml}^{ks} = G_{nml}^{ks}/(2\pi C_{nml}^{ks})$ can be used to estimate whether the resistive nonlinearity or the capacitive counterpart is dominant for certain operating frequencies in a specific technology for specific biasing conditions and transistor sizes. However, for transistors with fixed length (e.g. minimum length) and width that is not close to minimum width, f_{nml}^{ks} is fairly independent of transistor size (This is usually true for RF applications). This effectively leaves only bias dependent f_{nml}^{ks} factors in a certain technology.

When f_{nml}^{ks} is very high, Y_{nml}^{ks} can be reduced to a purely resistive component. Similarly, for Y_{nml}^{ks} having f_{nml}^{ks} much lower than any signal frequency, the Y_{nml}^{ks} can be seen as purely capacitive. As a result, evaluating f_{nml}^{ks} provides an approach to simplify the MOS transistor nonlinearity model for all of the weakly nonlinear RF circuits in the same transistor technology. This is different from previous work, as [3, 16] do not take the capacitive nonlinearities into account, while [17] takes a transistor as a black box and does not distinguish between the resistive and capacitive nonlinearities. Moreover, [3] removes insignificant resistive nonlinearities based on a system-level circuit model, which makes it topology-dependent, while our f_{nml}^{ks} is mainly dependent on bias conditions and technology parameters, and therefore largely topology-independent (appendix II shows an example for f_{210}^{ds} for an NMOS transistor). Hence, the nonlinearity parameters only need to be estimated once for a certain technology, and can then be (re)used in calculations or simulations using e.g. a look-up table.

In this paper, a commercial 90nm CMOS process is used for demonstration purposes. All simulations are done in Spectre circuit simulator, using the PSP compact MOSFET model [18] fitted to our 90nm CMOS process. The PSP model is known to correctly fit derivatives up to the third order [12,13] and to satisfy the so-called Gummel symmetry test (GST) [14,15]. Fitting derivatives up to the third order is essential to reliably estimate distortion levels for all presented circuits in this paper. Passing the GST is essential for accurate simulation of distortion in the attenuator circuit in section V.

Equation (3) shows that the relative importance of the nonlinearity between different terminals in one transistor can be determined by evaluating $H_p^{gs}(\omega_D) \cdot Y_{nml,p}^{gs}(\omega_D)/[H_p^{ds}(\omega_D) \cdot Y_{nml,p}^{ds}(\omega_D)]$ and $H_p^{bs}(\omega_D) \cdot Y_{nml,p}^{bs}(\omega_D)/[H_p^{ds}(\omega_D) \cdot Y_{nml,p}^{ds}(\omega_D)]$. Since $H_p^{ks}(\omega_D)$ are linear transfer functions that depend on the actual circuit topology, the evaluation of the relative impact of the nonlinearities between ports can only be used to simplify the MOS transistor nonlinearity model for individual circuits, similar to the situation in [3].

III. Cascode Amplifier Linearity Optimization

The cascode amplifier topology shown in Fig. 2 is widely used because of its superior properties over the common-source amplifier [19-23]. Typically the distortion contribution from cascode transistor M_2 is neglected [24-28], which is valid for sufficiently large output impedance levels of M_1. However, CMOS technology scaling yields relatively low output resistance for short transistors [29]. The distortion contribution of M_2 then can no longer be neglected.

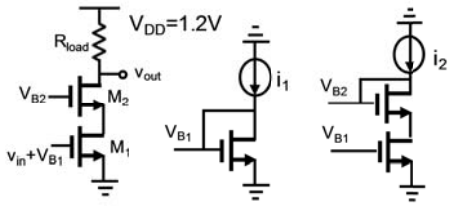

Fig. 2. Circuit schematic of the cascode amplifier.

In [30-31] only the effect of the transconductance nonlinearity G_{300}^{ds} in M_2 is analyzed, while the other nonlinearities related to the output conductance of M_2 (e.g. the third order output conductance nonlinearity G_{030}^{ds}, and the cross terms G_{210}^{ds} and G_{120}^{ds}) are neglected. In this section we take into account all nonlinearities up to the third order and demonstrate that for low supply voltage and large gain, G_{030}^{ds}, G_{210}^{ds} and G_{120}^{ds} may be dominant in the total distortion. Note that we focus on the distortion due to the cascode transistor, therefore we ignore the input matching for the CS amplifier and do not focus on good noise figure (NF). For simulation purpose we put a 50Ω resistor at the gate of M_1 for input matching.

Analysis results for output IM3 and a description are given below. The analysis described in the previous section shows that capacitive nonlinearities are not significant for this type of circuits in the low GHz range and can be neglected. The first-order approximation (see appendix III for the derivation) of the output IM3 of the cascode amplifier is

$$v_{out}^{\omega_{IM3}} \approx \frac{-3 \times {V_{IN}}^3 R_{load}}{4\left(g_{ds}^{M_1} + g_m^{M_2}\right)} \times \left[g_m^{M_2} \times \left\{ G_{300,M_1}^{ds} - \left(\frac{g_m^{M_1}}{g_{ds}^{M_1} + g_m^{M_2}}\right)^3 G_{030,M_1}^{ds} + \left(\frac{g_m^{M_1}}{g_{ds}^{M_1} + g_m^{M_2}}\right)^2 G_{120,M_1}^{ds} - \left(\frac{g_m^{M_1}}{g_{ds}^{M_1} + g_m^{M_2}}\right) G_{210,M_1}^{ds} \right\} \right. \quad (5)$$

$$+g_{ds}^{M_1}\left(\frac{g_m^{M_1}}{g_{ds}^{M_1}+g_m^{M_2}}\right)^3 \times \left\{G_{300,M_2}^{ds}+\left(g_m^{M_2}R_{load}-1\right)^3 G_{030,M_2}^{ds}\right.$$
$$\left.\left(g_m^{M_2}R_{load}-1\right)^2 G_{120,M_2}^{ds}-\left(g_m^{M_2}R_{load}-1\right)G_{210,M_2}^{ds}\right\}\Big]$$

Assuming $g_m^{M_1} \approx g_m^{M_2} \gg g_{ds}^{M_1}$ and $g_m^{M_2}R_{load} \gg 1$, (5) can be further simplified to

$$v_{out}^{\omega_{IM3}} \approx \frac{-3\times {V_{IN}}^3 R_{load}}{4\left(1+g_m^{M_2}r_{ds}^{M_1}\right)}$$
$$\left[g_m^{M_2}r_{ds}^{M_1}\left(G_{300,M_1}^{ds}+G_{120,M_1}^{ds}-G_{030,M_1}^{ds}-G_{210,M_1}^{ds}\right)\right.$$
$$-\left(g_m^{M_1}R_{load}\right)^3\cdot G_{030,M_2}^{ds}-g_m^{M_1}R_{load}\cdot G_{210,M_2}^{ds}$$
$$\left.+G_{300,M_2}^{ds}+\left(g_m^{M_1}R_{load}\right)^2\cdot G_{120,M_2}^{ds}\right] \quad (6)$$

where transistor nonlinearitis G_{300}^{ds}, G_{030}^{ds}, G_{120}^{ds} and G_{210}^{ds} are extracted from simulation as shown in Fig. 3.

Fig. 3(a) shows that in the strong inversion region the nonlinearities G_{300}^{ds} and G_{120}^{ds} have the same sign (negative) while G_{030}^{ds} and G_{210}^{ds} have the opposite sign (positive). It follows from equation (6) that the contribution from each third-order nonlinearity adds up in the circuit output. Equation (6) also shows that a large output resistance of M_1, $r_{ds}^{M_1}$, results in negligibly small distortion contributions of M_2 for the total IM3 compared to the contributions of M_1. However, in deep submicron CMOS technologies, typically the output resistance of M_1 is relatively low: the IM3 distortion contribution from M_2 then may become dominant. On top of that, the low supply voltage together with high gain operation tends to push M_2 out of the deep saturation region, resulting in a very significant increase of the third-order output conductance nonlinearity term G_{030,M_2}^{ds} and the cross-modulation nonlinearities G_{120,M_2}^{ds} and G_{210,M_2}^{ds}, see Fig. 3(b).

To demonstrate the increasing IM3 contribution from M_2 as the gain increases, Fig. 4 shows simulation results for the cascode amplifier in Fig. 2 for different gain settings by only changing R_{load} (from 100Ω to 250Ω) for a constant bias current. The two-tone signals are at 1GHz and 1.01GHz and the IIP3 is extrapolated by sweeping the input power from -35 to -25dBm. Fig. 4(a) shows that the model given by (5), including only the third-order transistor nonlinearity terms, provides an accurate IIP3 estimation for different gain settings. Fig. 4(b) shows that the voltage gain increases while the IIP3 decreases with increasing R_{load}. For larger R_{load} the drain voltage of M_2 decreases and M_2 comes out of deep saturation. As a result, the third-order nonlinearity terms G_{030,M_2}^{ds}, G_{120,M_2}^{ds} and G_{210,M_2}^{ds} increase significantly which results in a significant increase of IM3 distortion. Fig. 4(b) illustrates that the IM3 contribution of the cascode transistor M_2 then can be higher than that of M_1. Therefore in deep submicron CMOS technologies, linearity optimization must take into account not only G_{300}^{ds} and G_{030}^{ds}, but also cross-modulation terms G_{210}^{ds} and G_{120}^{ds}. These cross modulation-terms are usually neglected [30-31].

Expression (6) suggests that optimal bias for linearity should prevent M_2 from approaching the triode region where the third-order output conductance nonlinearity G_{030,M_2}^{ds} and the cross-modulation nonlinearity (G_{120,M_2}^{ds} and G_{210,M_2}^{ds}) are maximum. This leads to the following three linearity optimization approaches:

- optimiz the gate bias voltage of cascode transitor
- use components to bypass part of the DC bias current
- use distortion cancellation for the transistors.

For demonstration purposes the linearity optimization is performed for the cascode amplifier in Fig. 2 with $R_{load} = 250\Omega$, where transistor M_1 and M_2 are biased in strong inversion. The dimension and bias condition (g_{m1}=g_{m2}=20mS, W_1/L_1=W_2/L_2=50/0.1um, I_{DC}=2.23mA, V_{B1}=0.6V, V_{th}=0.42V and V_{B2}= V_{DD}=1.2V) provide 12.8dB voltage gain, 7.4dB NF, -4.5dBm IIP3 and -14dBm $P_{1\text{-dB}}$. The IIP3 is extrapolated by sweeping the input power from -35 to -25dBm with a two-tone signal at 1GHz and 1.01GHz. This design serves as reference for comparison with the optimized designs.

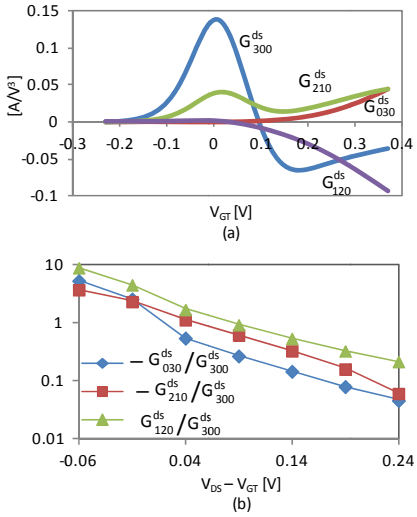

Fig. 3. (a) Simulated third-order nonlinearity of an NMOS as a function of the overdrive voltage V_{GT}. W/L=50/0.1 um, and V_{DS} = 0.3V. (b) Simulated third-order nonlinearity ratio ($-G_{030}^{ds}/G_{300}^{ds}$, $-G_{210}^{ds}/G_{300}^{ds}$ and $G_{120}^{ds}/G_{300}^{ds}$) of an NMOS as a function of the drain-source voltage V_{DS}- V_{GT}. W/L=50/0.1 um, and V_{GT} = 0.2V.

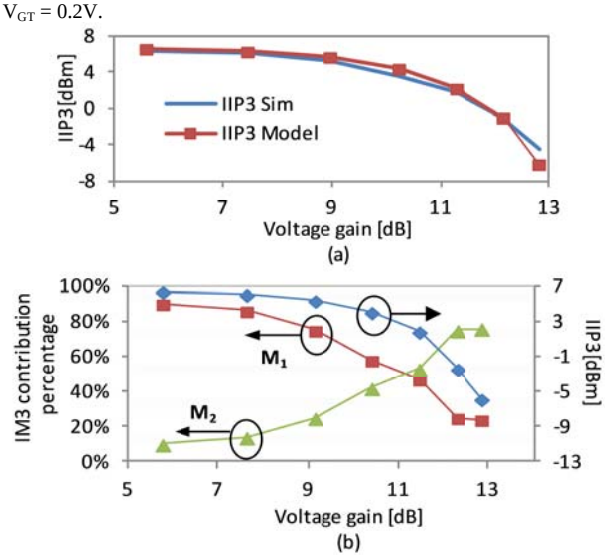

Fig. 4. (a) The simulated IIP3 and the calculated IIP3 by the model which only includes the transistor third-order nonlinearity. For M_1, W/L=50/0.1um, V_{B1}=0.6 V, V_{th}=0.42 V; for M_2, W/L=50/0.1um, V_{B2}=1.2 V. (b) The calculated IM3 contribution from M_1 and M_2 to the circuit output and simulated IIP3 in different voltage gain settings.

A. *Optimizing the cascode transistor gate bias voltage*

One approach for linearization is to adjust the gate bias of cascode transistor M_2. Usually the gate voltage is equal to the supply voltage V_{DD}. In this section it is shown that other (DC-) voltages may result in better performance; we do not address applying AC-variations (e.g. gain boosting) for simplicity reasons.

It can be derived from (6) and the relations between the transistor nonlinearities and biasing conditions that by adjusting the gate bias of M_2 (V_{B2}) the overall circuit linearity can be optimized. For low cascode gate bias levels, M_1 is biased between the saturation region and triode region where its output conductance nonlinearity G^{ds}_{030,M_1} and the cross-modulation nonlinearity (G^{ds}_{120,M_1} and G^{ds}_{210,M_1}) are high, resulting in rather low IIP3. At high cascode gate bias voltage levels the cascode transistor M_2 may go out of saturation which increases its nonlinearities G^{ds}_{030,M_2}, G^{ds}_{120,M_2} and G^{ds}_{210,M_2}. In between these two extremes, the total distortion of the two transistors is minimum, and typically dominated by the third-order transconductance nonlinearity G^{ds}_{030} of M_1. Fig. 5 shows that for the reference LNA design a cascode transistor gate bias in the range of 1 V to 1.05V yields maximum IIP3 with slightly degraded NF and voltage gain.

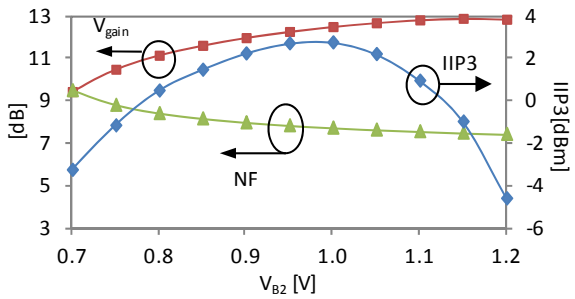

Fig. 5. The simulated noise figure, voltage gain and IIP3 of the cascode amplifier shown in Fig. 2 as a function of the gate bias V_{B2} of M_2 for a constant power consumption. For M_1, W/L=50/0.1um, V_{B1}=0.6 V; for M_2, W/L=50/0.1um.

B. *Usage of bypass components*

One of the dominant effects with respect to distortion is the limited voltage headroom for either M_1 or M_2, which is among others limited by the DC-voltage drop across the resistor. Using components to bypass part of the DC-current increases the headroom and hence decreases distortion.

One way to implement this is to add a pMOS load or an (on-chip) inductor in parallel to R_{load}. A parallel pMOS load (M_3) conducts a part of the DC current and lifts up the drain voltage of M_2. As a result, the output conductance nonlinearity G^{ds}_{030,M_2} and the cross-modulation nonlinearity terms (G^{ds}_{120,M_2} and G^{ds}_{210,M_2}) of M_2 decrease. For the first-order approximation the output IM3 of the cascode amplifier given by (6) changes to

$$v_{out}^{\omega_{IM3}} \approx \frac{-3\times V_{IN}{}^3 R_{load}}{4\left(1+g_m^{M_2} r_{ds}^{M_1}\right)} \times \left[g_m^{M_2} r_{ds}^{M_1} \left(G^{ds}_{300,M_1} + G^{ds}_{120,M_1} - G^{ds}_{030,M_1} - G^{ds}_{210,M_1}\right) - \left(g_m^{M_1} R_{load}\right)^3 \cdot G^{ds}_{030,M_2} - g_m^{M_1} R_{load} \cdot G^{ds}_{210,M_2} + G^{ds}_{300,M_2} + \left(g_m^{M_1} R_{load}\right)^2 \cdot G^{ds}_{120,M_2} - \left(1 + g_m^{M_2} r_{ds}^{M_1}\right) \cdot \left(g_m^{M_1} R_{load}\right)^3 \cdot G^{ds}_{030,M_3} \right] \quad (7),$$

where the last term represents the distortion contribution from M_3 via its output conductance nonlinearity G^{ds}_{030,M_3}. Although M_3 contributes additional distortion, the circuit linearity can still be improved with a proper design. Fig. 6 shows the simulation result for the cascode amplifier with pMOS load M_3 in parallel to R_{load} by sweeping the width of M_3 (W_3). A channel length three times the minimum length is used to increase the output resistance of M_3 for keeping the voltage gain almost unchanged. As W_3 increases, the drain voltage of M_2 increases since less dc current passes through R_{load}. The IIP3 increases as M_2 enters further into the saturation region. More DC current through M_3 further increases the drain voltage of M_2. This pushes M_3 out of deep saturation and causes more distortion and noise from M_3. The IIP3 is optimum at the region where both the cascode transistor M_2 and the M_3 are in saturation. Then the output conductance nonlinearity G^{ds}_{030,M_2}, the cross-modulation nonlinearity (G^{ds}_{120,M_2} and G^{ds}_{210,M_2}) of M_2 and the output conductance nonlinearity G^{ds}_{030,M_3} of M_3 are less significant than the third-order transconductance G^{ds}_{030,M_1} of M_1. Alternatively an on-chip stacked inductor load can also be used to increase the drain voltage of M_2 [32]. However, for frequencies in the lower GHz range, the low quality factor introduces rather small shunt parasitic resistance that limits the amplifier gain. Moreover, on-chip stacked inductors typically consume much more area than a pMOS load [32-33].

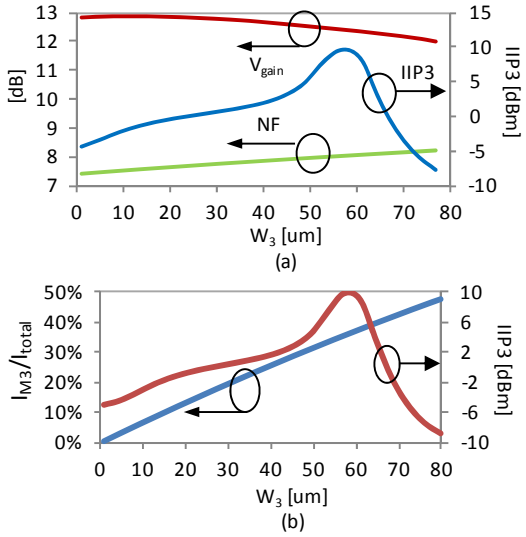

Fig. 6. Simulation results of the cascode amplifier with the pMOS load as a function of the width M_3. (a) NF, voltage gain and IIP3. (b) IIP3 and the dc current supplied by the pMOS load M_3 divided by the total dc current.

C. *Optimal bias in moderate inversion region*

Assuming that the main nonlinearity of a MOS transistor arises from transconductance nonlinearity G^{ds}_{300}, the IIP3 sweet spot of the single transistor amplifier coincides with the setting at which G^{ds}_{300} is zero [9]. Due to increasingly nonlinear output conductance and cross terms in submicron CMOS

technologies, the actual IIP3 sweet spot of a single transistor amplifier however does not coincide with zero-G_{300}^{ds} [9, 11]. As the cascode transistor may contribute significant distortion, the effect of the cascode transistor on the IIP3 sweet spot needs to be included.

The simplified model in (6) is used to estimate the IIP3 sweet spot of the cascode amplifier. Fig. 3(a) shows that in moderate inversion the nonlinearities G_{300}^{ds}, G_{030}^{ds} and G_{210}^{ds} are positive and G_{120}^{ds} is negative. Thus the distortion generated by G_{300}^{ds} of M_1 and M_2 cancels the distortion of all the other nonlinearities within M_1 and M_2 as suggested by (6). As illustration for this, Fig. 7 shows the simulation and calculation result for the cascode amplifier where M_1 and M_2 are set to have a constant g_m of 20mS at 1GHz, which is the same as in the reference design. Firstly, Fig. 7(a) shows that the model given by (6) including only the third-order transistor nonlinearity provides an accurate IIP3 estimation for the moderate inversion bias region. As shown in (6) and Fig 4(a), for very low V_{GS}, G_{300,M_1}^{ds} and G_{300,M_2}^{ds} are large and dominantly contribute to the output distortion. As V_{GS} increases, G_{300,M_1}^{ds} and G_{300,M_2}^{ds} start to decrease and their distortion cancels the distortion generated by the other transistor nonlinearities; this enables a high-IIP3 region around V_{GT}=70mV, which is about 20mV away from the zero-G_{300}^{ds} setting illustrated by the dashed line in Fig. 7(a). For large V_{GS} when the transistors enter strong inversion, G_{300,M_1}^{ds}

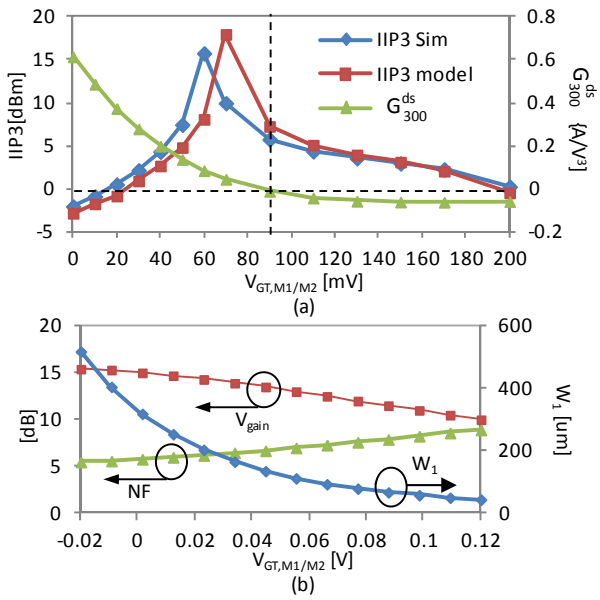

Fig. 7. (a) The simulated IIP3 and the calculated IIP3 modeling only third-order nonlinearity. (b) NF, voltage gain and transistor width as a function of V_{GT} for a constant 1.17 mA current.

and G_{300,M_2}^{ds} get negative and there is no distortion cancellation. Based on Fig. 7 we choose one optimal design (W_1/L_1=W_2/L_2=104/0.1um, V_{GT}=70mV, I_{DC}=1.17mA). Compared to the reference cascode amplifier design, the transistor width is doubled while the DC current is about halved.

Fig. 8 shows that for a set of 200-time Monte Carlo simulation with mismatch and process corner spread the moderate inversion optimal region enables mean IIP3 of 12.5dBm at 1GHz, which is an improvement of about 16dB compared to the reference design operating in strong inversion. To illustrate frequency-dependencies, Fig. 9 shows the simulated results of this optimal design for input signal frequency from 0.1GHz to 10GHz. Fig. 9 shows that optimal bias in the moderate inversion improves IIP3 by more than 10dB for frequencies up to 10GHz. The cancellation degrades at higher frequencies because of increasing phase shifts between the distortion components generated by G_{300}^{ds} and by the other nonlinearity components. The simulated IM3 and HD1 for varying input power in Fig.10 shows that the IM3 cancellation in the moderate inversion region becomes less effective for input signals larger than -15dBm. This is due to higher-order transistor nonlinearities. Since the voltage drop

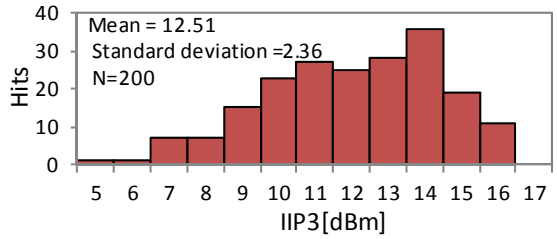

Fig. 8 Simulated IIP3 of the cascode amplifier optimized in the moderate inversion region in Monte Carlo simulation (200run) for mismatches and process corner at 1GHz.

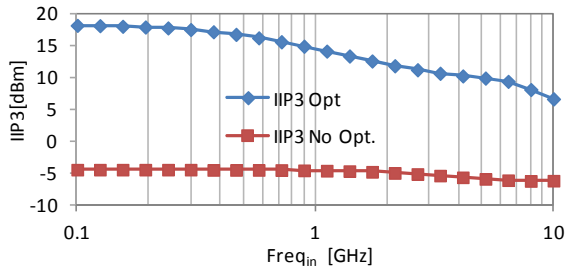

Fig. 9 Simulated IIP3 of the cascode amplifier optimized in the moderate inversion region over input frequency.

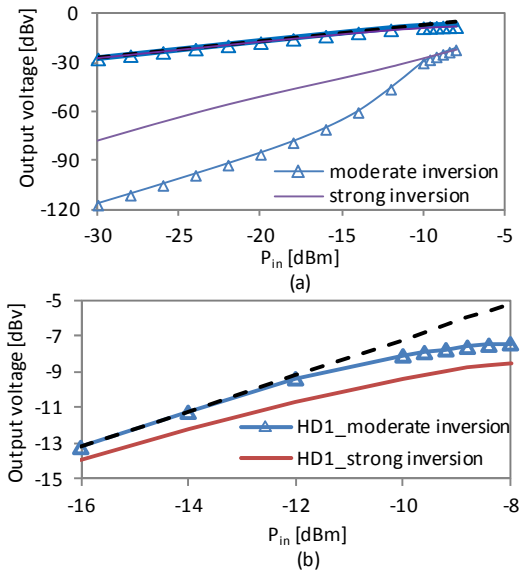

Fig. 10. (a) Simulated HD1 and IM3 for varying input power. (b) Simulated HD1 for varying input power denoting the 1dB compression.

across R_{load} is halved in the moderate inversion region, there is more headroom for the output swing and hence increases $P_{1\text{-dB}}$ from -14dBm to -10dBm.

D. Summary

The general weak nonlinearity model used for the cascode amplifier topology shows that the cascode transistor M_2 may contribute significantly to the overall distortion, especially in high gain settings in deep submicron CMOS. A number of ways to minimize distortion were discussed, among which optimum gate biasing of the cascode transistor, using DC-current bypass components, and enabling distortion cancellation in moderate inversion operation.

Table I lists the simulation results of optimal linearity designs using the three optimization approaches discussed in section III. The optimal designs are obtained using the data in Fig. 5, Fig. 6 and Fig. 7 respectively. Table I shows that only adjusting the cascode transistor gate bias (Opt.A) increases IIP3 by 6dB while gain and noise are slightly affected. This approach takes no extra active area. For higher IIP3 either the pMOS load (Opt.B) should be used or the cascode amplifier should be biased in the moderate inversion (Opt.C). Both Opt.B and Opt.C need extra active area while gain and noise are slightly affected. However, biasing the amplifier in the moderate inversion (Opt.C) uses about 50% less current and achieves the largest IIP3 improvement due to the distortion cancellation between M_1 and M_2 while little effect on gain and NF. Less dc bias current provides more headroom for the output swing and increases $P_{1\text{-dB}}$. As shown in section III.C, for all process corners and for frequencies up to 10 GHz biasing in moderate inversion appears to be optimum.

TABLE I
COMPARISION OF IIP3 OPTIMIZATION APPROACHES

	I_{DC} [mA]	IIP3 [dBm]	Gain [dB]	NF [dB]	Active area [um^2]	$P_{1\text{-dB}}$ [dBm]
Ref. Design	2.23	-4.5	12.8	7.4	10	-14
Opt. A	2.23	2.7	12.5	7.7	10	-11.7
Opt. B	2.23	9.7	12.5	8	27.1	-13.8
Opt. C	1.17	14.5	12.8	7.1	20.8	-10

Opt.A: cascode transistor gate bias adjustment.
Opt.B: pMOS load.
Opt.C: moderate inversion biasing.

IV. COMMON-GATE LNA LINEARITY OPTIMIZATION

Due to the strict demands on input matching, the transconductance (g_m) for a common-gate (CG) LNA is fixed, resulting in difficulties in simultaneously providing NF< 3dB and high gain [34-39]. The cross-coupled capacitors shown in Fig. 11 are frequently used for g_m boosting in order to achieve high gain and low NF [34-36, 38-39]. For 50Ω input matching, M_{1a} and M_{1b} are dimensioned for a fixed transconductance ($g_m = 1/2R_s$): for high gain and a low NF then a large R_{load} is required. Similar to the discussions in section III for the cascode common source amplifier, the large R_{load} decreases the drain voltage of M_{2a}/M_{2b} and tends to push M_{2a}/M_{2b} out of deep-saturation. As a result, the third-order output conductance nonlinearity G^{ds}_{030,M_2} and the cross-modulation nonlinearity (G^{ds}_{120,M_2} and G^{ds}_{210,M_2}) increases dramatically and contributes more IM3 distortion. For demonstration, we simulate the CG LNA shown in Fig. 11(a) in different gain settings by

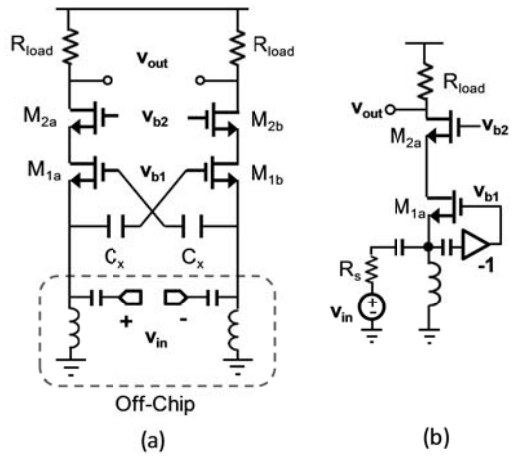

Fig. 11 Schematic of the capacitive cross-coupled common-gate LNA. (a) Differential schematic and (b) half-circuit model.

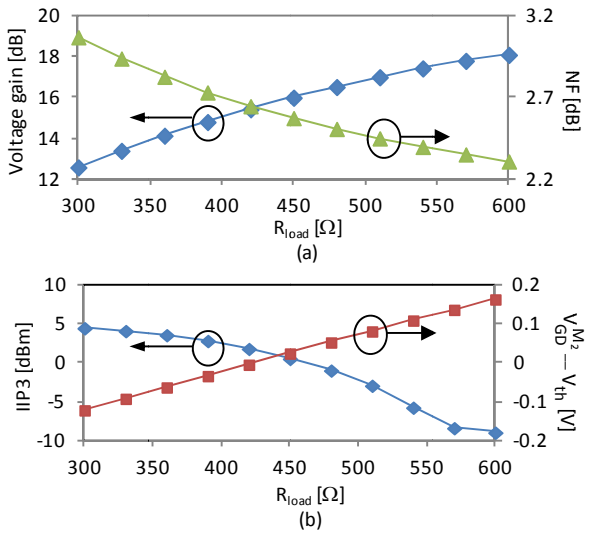

Fig. 12 The simulated (a) NF and voltage gain (b) $V_{GD}^{M_2} - V_{th}$ of M_{2a}/ M_{2b} and IIP3 of the CG LNA shown in Fig. 10a as a function R_{load} for a constant power consumption. For M_1 and M_2, W/L=26/0.1um, V_{GTM1}=0.16 V, V_{b2}=V_{dd}=1.2 V.

sweeping R_{load} (from 300Ω to 600Ω) for a constant 2 mA DC current while keeping S_{11}<-10dB. The two-tone signals are at 1 GHz and 1.01 GHz and the IIP3 is extrapolated by sweeping the input power from -35 to -25 dBm. Fig. 12 shows that larger R_{load} improves NF and gain at the price of decreasing IIP3 since M_{2a}/M_{2b} are pushed out of the deep saturation region.

The optimal bias region can be estimated using the expression for the output IM3 of the CG LNA half-circuit model shown in Fig. 11(b) (see appendix IV for the derivation):

$$v_{out}^{\omega_{IM3}} \approx \frac{-3 \times V_{IN}{}^3 R_{load}}{32\left(g_{ds}^{M_1} + g_m^{M_2} + g_{ds}^{M_1} g_m^{M_2} R_s + 2 g_m^{M_1} g_m^{M_2} R_s\right)} \times \left\{ g_m^{M_2} \times \left[-8 G^{ds}_{300,M_1} + \left(\frac{1}{g_m^{M_2} R_s} - 1\right)^3 G^{ds}_{030,M_1} - 2\left(\frac{1}{g_m^{M_2} R_s} - 1\right)^2 G^{ds}_{120,M_1} + 4\left(\frac{1}{g_m^{M_2} R_s} - 1\right) G^{ds}_{210,M_1} \right] \right. \quad (8).$$

$$+\frac{g_{ds}^{M_2}}{\left(g_m^{M_2}R_s\right)^3}\times\left[-G_{300,M_2}^{ds}+\left(g_m^{M_2}R_{load}-1\right)^3G_{030,M_2}^{ds}\right.$$
$$\left.-\left(g_m^{M_2}R_{load}-1\right)^2G_{120,M_2}^{ds}+\left(g_m^{M_2}R_{load}-1\right)G_{210,M_2}^{ds}\right\}$$

Assuming that $g_m^{M_1}\approx g_m^{M_2}\approx 1/2R_s \gg g_{ds}^{M_1}$ and $g_m^{M_2}R_{load}\gg 1$, (8) can be simplified to

$$v_{out}^{\omega_{IM3}}\approx\frac{-3\times V_{IN}{}^3R_{load}R_s}{32}\times$$
$$\left\{g_m^{M_2}\times\left(-8G_{300,M_1}^{ds}+G_{030,M_1}^{ds}-2G_{120,M_1}^{ds}+4G_{210,M_1}^{ds}\right)\right. \quad (9).$$
$$+8g_{ds}^{M_2}\left[-G_{300,M_2}^{ds}+\left(g_m^{M_2}R_{load}\right)^3G_{030,M_2}^{ds}\right.$$
$$\left.\left.-\left(g_m^{M_2}R_{load}\right)^2G_{120,M_2}^{ds}+\left(g_m^{M_2}R_{load}\right)G_{210,M_2}^{ds}\right]\right\}$$

For the common gate LNA, (9) suggests a similar IM3 cancellation scheme as for the cascode CS amplifier discussed in section III. In the moderate inversion region the transconductance nonlinearities G_{300}^{ds} turn into positive values. Thus the distortion generated by G_{300}^{ds} of M_1 and M_2 cancels the distortion of all the other nonlinearities within M_1 and M_2. Fig. 13 shows the simulated IIP3 of the CG LNA as well as the calculated IIP3 using (8). Both M_1 and M_2 have the same dimension and a constant transconductance (g_m=9mS for S_{11}<-25dB) for different overdrive voltage V_{GT}. The load R_{load} is set to 600Ω to achieve 18dB voltage gain and 2.3dB NF. The two-tone signals are at 1 GHz and 1.01 GHz and the IIP3 is extrapolated by sweeping the input power from -35 to -25 dBm. Fig. 13 shows that the model given by (8) provides a good prediction on the IIP3 changing trend. For very low V_{GT}, G_{300,M_1}^{ds} and G_{300,M_2}^{ds} are large and dominantly contribute to theoutput distortion. As V_{GT} increases, G_{300,M_1}^{ds} and G_{300,M_2}^{ds} start to decrease and their distortion cancels the distortion generated by the other transistor nonlinearity terms. This cancellation enables a high-IIP3 region around V_{GT} =50mV. For large V_{GT} the transistors enter the strong inversion region, and G_{300,M_1}^{ds} and G_{300,M_2}^{ds} become negative and as a result no distortion cancellation can take place between M_1 and M_2. For comparison we simulate two LNA designs at 1GHz. The load R_{load} is set to 600Ω and a 100nH inductor with Q=80 is used to model the off-chip inductor. In both designs M_1/M_2 are set to g_m=9mS, while in LNA1 the transistors are biased in strong inversion region and in LNA2 the transistors are biased in moderate inversion. Table II shows that in the optimal moderate inversion region, IIP3 is improved by 15dB, the DC current is decreased by 50% while NF, gain and input matching stay the same. However, the price to be paid is about 3dB smaller bandwidth since the transistor width increases by about two times in the optimal moderate inversion region.

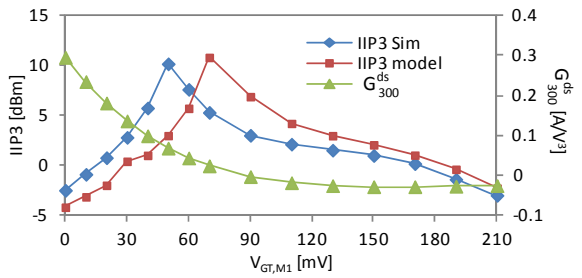

Fig. 13 The simulated and the calculated IIP3 and G_{300}^{ds} as a function of overdrive voltage of M_1 and M_2.

A 200-sample Monte Carlo simulation with mismatch and corner spread shows in Fig. 14 that moderate inversion biasing yields a mean IIP3 of 9.4dBm, which is about 14dB higher than biasing in saturation. Fig. 15 shows the IIP3 for the designs as a function of frequency from 0.1GHz to 10 GHz. It is shown that the optimal bias in the moderate inversion improves IIP3 by more than 10dB up to 5GHz. The distortion cancellation degrades towards higher frequencies because of phase shifts between the distortion components due to G_{300}^{ds} and due to the other nonlinearity terms. Fig. 16 shows the simulated IM3 and HD1 as a function of input power; the IM3 cancellation in moderate inversion becomes less effective for input signals

TABLE II
COMPARISION OF CG LNA IN DIFFERENT BIAS REGIONS

	V_{GT} [mV]	I_{dc} [mA]	IIP3 [dBm]	Gain [dB]	NF [dB]	S_{11} [dB]	$P_{1\text{-dB}}$ -dBm]	$W_{M1/M2}$ [um]
LNA1	170	1.92	-5	18.2	2.35	-29	-15.5	26
LNA2	48	1	10	18	2.32	-26	-13.5	56

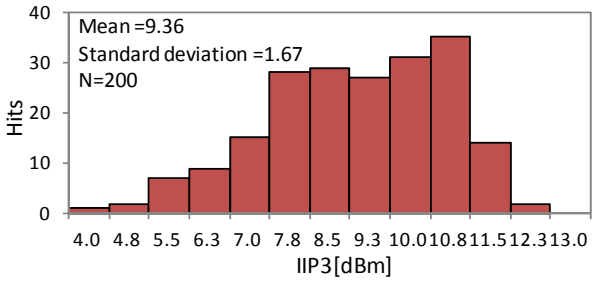

Fig. 14 Simulated IIP3 of the cascode amplifier optimized in the moderate inversion region in Monte Carlo simulation (200run) for mismatches and process corner.

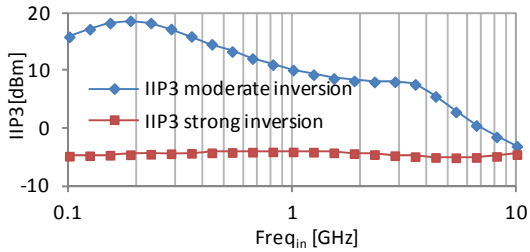

Fig. 15 Simulated IIP3 of the CG LNA optimized in the moderate inversion region over input frequency.

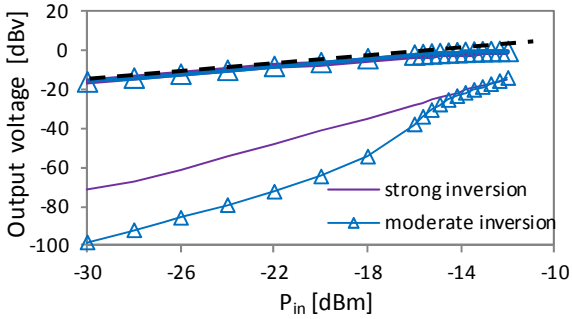

Fig. 16 Simulated HD1 and IM3 for varying input power.

larger than -18dBm. This is due to transistor nonlinearities higher than third-order. Since the voltage drop across R_{load} is halved in the moderate inversion region, there is more headroom for the output swing and hence this increases $P_{1\text{-dB}}$ from -15.5dBm to -13.5dBm.

V. Attenuator Linearity Optimization

Many RF receivers such as mobile TV receivers experience input signals with high dynamic range. This large input power variation can be decreased using precise gain control circuits, which is traditionally implemented as variable-gain amplifiers (VGAs). However, CMOS-switch-based attenuators can provide precise gain control, and may show superior performance in linearity and power consumption [40-43].

One way to set the attenuation factor in a CMOS attenuator is to implement voltage controlled resistances in one resistive division network [40-42]. Another way is to switch between different (mainly passive) attenuator branches [43] where each individual attenuator branch provides one specific attenuation value. One advantage of this latter implementation is that each attenuator branch can be highly optimized (individually).

This section focuses on the linearity optimization of the CMOS attenuator shown in Fig. 17 that is used in attenuator networks. The input power source is modeled by the voltage source $v_s = 2v_{in}$ with source impedance R_s. Note that this attenuator can be regarded as a part of a PI- or T-attenuator, but with one transistor/resistor less because there is no inverse matching (typically not needed on-chip). Assuming perfect input matching provided by the attenuator, the input voltage for the attenuator is v_{in} and the attenuation is defined by $A = v_{out}/v_{in}$. When the switch transistors M_1 and M_2 enable the input-matching, the signal attenuation is provided via the network of resistor R_1, resistor R_2, transistor M_1 and transistor M_2. The large resistors $R_G^{M_1}$ and $R_B^{M_1}$ are used to minimize the

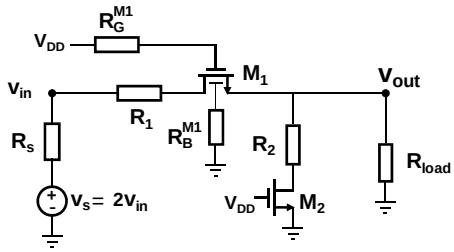

Fig. 17. The schematic of the CMOS attenuator

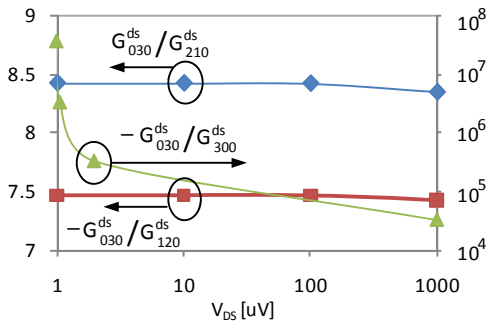

Fig. 18. Simulated third-order nonlinearity ratio ($G_{030}^{ds}/G_{210}^{ds}$, $-G_{030}^{ds}/G_{300}^{ds}$ and $-G_{030}^{ds}/G_{120}^{ds}$) of an NMOS switch as a function of the drain-source voltage V_{DS}. W/L=100/0.1 um, and V_{GS} = 1.2V.

source-gate voltage swing and source-well voltage swing: with sufficiently large resistors these voltages are purelyAC-coupled [40]. In that case $v_{gs}^{M_1} \cong 0.5 v_{ds}^{M_1}$ and $v_{bs}^{M_1} \cong 0$. This firstly extends the bandwidth of this attenuator, and secondly minimizes the nonlinearity related to $v_{gs}^{M_1}$ and $v_{bs}^{M_1}$.

As a first-order approximation (see Appendix V for the derivation) the output IM3 of the attenuator is

$$v_{out}^{\omega_{IM3}} \approx \frac{3}{4} \times {V_{IN}}^3 \times \left\{ \frac{A \cdot {R_{on}^{M_1}}^4}{2{R_s}^3} \cdot \left[8G_{03,M_1}^{ds} + \frac{G_{120,M_1}^{ds}}{2} + \frac{G_{210,M_1}^{ds}}{4} + \frac{G_{300,M_1}^{ds}}{8} \right] - \frac{(2-Att)\cdot(1-Att)^4 {R_{on}^{M_2}}^4}{2{R_s}^3} \cdot G_{030,M_2}^{ds} \right\} \tag{10}$$

Both transistors operate either in the off-state which is not very relevant for distortion analyses or in deep triode. In deep triode the dominant nonlinearity is the third-order output conductance nonlinearity G_{030}^{ds}, as suggested in Fig. 18. This allows for simplification of (10) into:

$$v_{out}^{\omega_{IM3}} \approx \frac{3 \times {V_{IN}}^3}{8{R_s}^3} \times \left[A \cdot {R_{on}^{M_1}}^4 G_{030,M_1}^{ds} - (2-A)(1-A)^4 \cdot {R_{on}^{M_2}}^4 G_{030,M_2}^{ds} \right] \tag{11}$$

To the first order approximation, the R_{on} is inversely proportional to the transistor width W and the third-order output conductance nonlinearity G_{030}^{ds} is proportional to W, we use $R_{on} = K_{Ron}/W$ and $G_{030}^{ds} = K_{G_{030}^{ds}} \cdot W$ which yields:

$$v_{out}^{\omega_{IM3}} \approx \frac{3{V_{IN}}^3 \cdot K_{Ron}^4 \cdot K_{G_{030}^{ds}}}{8{R_s}^3} \times \left(\frac{A}{{W_{M_1}}^3} - \frac{(2-A)(1-A)^4}{{W_{M_2}}^3} \right) \tag{12}$$

From (12) it follows that:

1) The IM3 distortion from the switch is inversely proportional to W^3.
2) With any sensible attenuation value, $A \in (0,1)$, the IM3 distortion from the switch transistor M_1 can cancel the distortion from switch M_2 for a specific ratio between the widths of the two switch transistors $\frac{W_{M_2}}{W_{M_1}}$.

With the simplified expression above, the optimum switch width is:

$$W_{M_2,opt} \approx \sqrt[3]{\frac{(2-A)(1-A)}{A}} \cdot (1-A) \cdot W_{M_1} \tag{13}$$

For demonstration purposes, we simulate the attenuator circuit in Fig. 17 by sweeping the width of M_2 for three attenuation values (A=-6dB, A=-12dB and A=-20dB). For the simulations, the width of M_1 is fixed to 200um while the values for R_1 and R_2 are set in such a way that both input impedance matching and the specified attenuation are obtained. The two-tone signals are at 1GHz and 1.006GHz and the IIP3 is extrapolated by sweeping the input power from -10 to 0 dBm. Fig. 19(a) shows that the attenuator achieves the targeted attenuation with very good input matching. Fig. 19(b) shows that for every attenuation level an optimal IIP3 can be achieved at certain $\frac{W_{M2}}{W_{M1}}$. In Table III the optimal W_{M2} obtained by

simulation in Fig. 19(b) is compared with the optimal W_{M2} estimated by (13),which shows the good accuracy of our model. As suggested by (12), for small W_{M2} the distortion generated by M_2 is much larger than that from M_1. Therefore IIP3 is determined by M_2. As W_{M2} increases, IIP3 increases until its highest value when the amplitude of the distortion from M_2 is equal to that of the distortion from M_1. For large W_{M2} the IIP3 is determined by M_1 and because in this simulation W_{M1} is fixed, the IIP3 does not change as W_{M2} increases to very large values. The simulation results show that in higher attenuation setting the IM3 cancellation is effective for wider M_2, which also follows from (13).

The demands on linearity are usually the highest for high attenuation setting (i.e. small levels of *A*). Therefore, we simulate the effect of mismatch and process spread and operation frequency on this IM3 cancellation scheme for the attenuator with -20dB attenuation, The two-tone signals at 1GHz and 1.006GHz are used and the IIP3 is extrapolated by sweeping the input power from -10 to 0dBm. Equation (12) shows that near the minimum distortion setting of the attenuator circuit the sensitivity towards spread and mismatch may be large, which is shown in Fig. 20(a) that for small switches (W_{M1}=30um and W_{M2}=74um) the IIP3 peak is narrower than for wide switches (W_{M1}=200um and W_{M2}=475um). Note that the calculated IIP3 using our model in (14) matches simulation very well. The overall result of spread and mismatch on the IIP3 is estimated using 200-time Monte-Carlo simulations

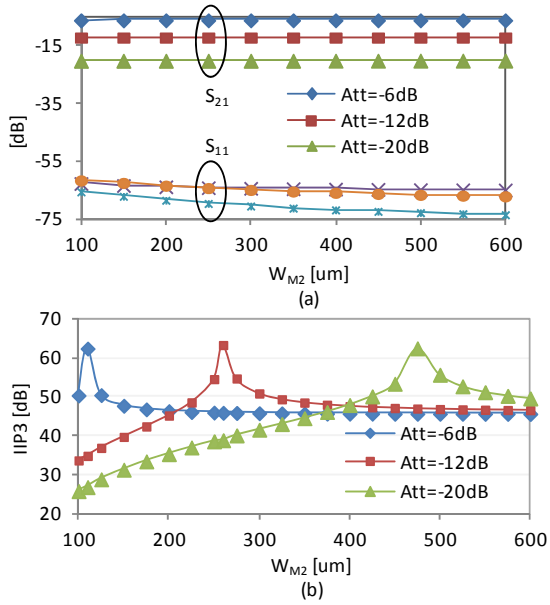

Fig. 19. The simulation results of the attenuator designed for three attenuation values (-6dB, -12dB and -20dB) as a function of the width of M_2. (a) S_{21} and S_{11} and (b) IIP3.

TABLE III
MODEL ESTIMATION OF $W_{M2,OPT}$ FOR IIP3 OPTIMIZATION

Attenuation[dB]	Estimated $W_{M2,OPT}$ [um]	Simulated $W_{M2,OPT}$ [um]
-6	113	110
-12	260	250
-20	464	475

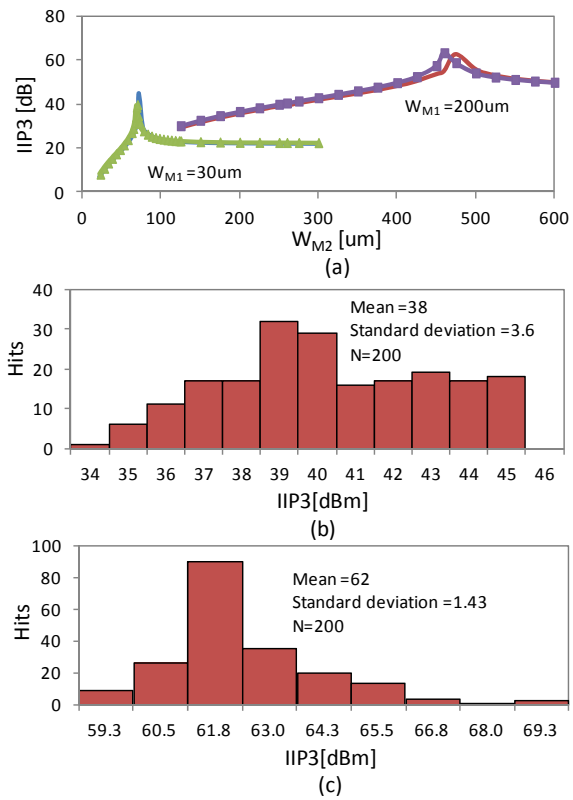

Fig. 20. The simulation results of the attenuator designed for high attenuation values (-20dB). (a) Simulated IIP3 (line) and calculated IIP3 (line with symbol) as a function of the width of M_2 for small M_1 (W_{M1}=30um) and wide M_1 (W_{M1}=200um) repectively. IIP3 in Monte Carlo simulation for mismatch& process corner at 1GHz for small switches (b) and wide switches (c).

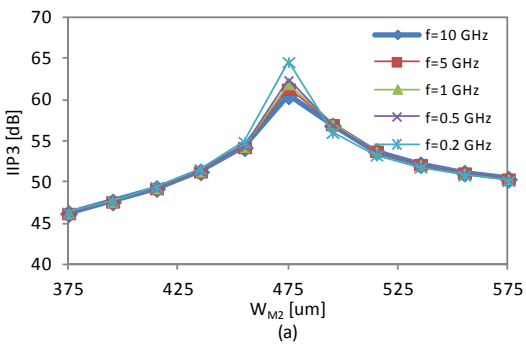

Fig. 21. The simulated IIP3 of the attenuator (*A*=-20dB) for 0.2GHz-10GHz band.

shown in Fig. 20(b-c). For the optimal design with small switches (W_{M1}=30um and W_{M2}=74um) the mean IIP3 is 38dBm (nominal IIP3 is 45dBm). For the optimal design with wide switches (W_{M1}=200um and W_{M2}=475um) the mean IIP3 is 62dBm (nominal IIP3 is 62dBm). As a result, the sensitivity of this IM3 cancellation scheme can be reduced by using wide switches. Note that for small switches optimized with IM3 cancellation (W_{M1}=30um and W_{M2}=74um), the worst-case IIP3 in the Monte-Carlo simulation still reaches 34dBm, which is 12 dB higher than in the design with the same W_{M1} (30um) but wider W_{M2} (250um). In this analysis it was assumed that there is no significant frequency dependency. An illustration of this is given in Fig. 21, where the IIP3 is shown as a function of W_{M2}

with a fixed W_{M1} (200 um) for frequencies from 0.2 GHz to 10GHz.

In summary, the general weak nonlinearity model provides an accurate analytical expression for the linearity optimization of the CMOS attenuator in Fig. 17.

VI. Conclusion

We introduced a generalized weak nonlinearity analysis method, which is somewhat related to harmonic balance analyses. It can obtain closed-form expressions for circuit distortion. Due to the nature of the method, the obtained expressions consist of technology dependent transistor nonlinearity parameters and topology-dependent AC transfer functions only. Simple techniques were introduced to maximally decrease computational effort, such as limiting calculations in such a way that only signals leading to the targeted distortion component are included in the calculations. Secondly a nonlinearity cutoff frequency f_{nml}^{ks} was used to determine the relative importance between the resistive nonlinearity and its capacitive counterpart and to allow for omission of nonlinearity terms. The characterization results of f_{nml}^{ks} is topology-independent and can be (re)used for all the circuit designs in the same process, which improves the efficiency of numerical circuit optimization.

The general weak nonlinearity model is applied to three RF circuits to explore the design space for linearity optimization insights that is usually available in today's deep submicron CMOS technologies. We show that in a standard cascode LNA circuit, the cascode transistor can significantly contribute to distortion in deep submicron CMOS technologies. This is due to the low supply voltage and the decreasing output resistance. A number of ways to decrease the distortion with (almost) unchanged NF and gain are discussed, including DC-current bypass components and biasing the transistor in the moderate inversion region to get distortion cancellation. For both common source amplifier and common gate LNA, this IM3 cancellation scheme provides robustly more than 10dB IIP3 improvement for signal frequencies up to 5GHz in a 90nm CMOS process. For a CMOS attenuator circuit, a novel and robust IM3 cancellation technique is demonstrated; with a proper sizing, the distortion from the two switches in the attenuator can cancel each other, yielding more than 10dBm IIP3 improvement from 0.2GHz to 10GHz.

Acknowledgment

The authors thank E.A.M. Klumperink for fruitful discussions.

Appendix I

For calculating the output IM3, the following function takes into account only the terms leading to the signals at $\omega_{IM3} = 2\omega_2 - \omega_1$

$$\begin{aligned}\beta_{nml}^{\omega_{IM3}}\Big|_{n+m+l=3} &= \frac{V_{IN}^{\ 3}}{4}\cdot[n\cdot v_{gs}^{\ *}(\omega_1)v_{gs}^{\ n-1}(\omega_2)v_{ds}^{\ m}(\omega_2)v_{bs}^{\ l}(\omega_1) \\ &\quad +m\cdot v_{gs}^{\ n}(\omega_2)v_{ds}^{\ *}(\omega_1)v_{ds}^{\ m-1}(\omega_2)v_{bs}^{\ l}(\omega_2) \\ &\quad +l\cdot v_{gs}^{\ n}(\omega_2)v_{ds}^{\ m}(\omega_2)v_{bs}^{\ *}(\omega_1)v_{bs}^{\ l-1}(\omega_2)\,]\end{aligned} \tag{A1}$$

$$\begin{aligned}\beta_{nml}^{\omega_{IM3}}\Big|_{n+m+l=2} &= \frac{V_{IN}^{\ 3}}{4}\cdot[n\cdot v_{gs}^{\ *}(\omega_1-\omega_2)v_{gs}^{\ n-1}(\omega_2)v_{ds}^{\ m}(\omega_2)v_{bs}^{\ l}(\omega_1) \\ &\quad +m\cdot v_{gs}^{\ n}(\omega_2)v_{ds}^{\ *}(\omega_1-\omega_2)v_{ds}^{\ m-1}(\omega_2)v_{bs}^{\ l}(\omega_2) \\ &\quad +l\cdot v_{gs}^{\ n}(\omega_2)v_{ds}^{\ m}(\omega_2)v_{bs}^{\ *}(\omega_1-\omega_2)v_{bs}^{\ l-1}(\omega_2) \\ &\quad +n\cdot v_{gs}^{\ *}(\omega_1)v_{gs}^{\ n-1}(2\omega_2)v_{ds}^{\ m}(2\omega_2)v_{bs}^{\ l}(2\omega_2) \\ &\quad +m\cdot v_{gs}^{\ n}(2\omega_2)v_{ds}^{\ *}(\omega_1)v_{ds}^{\ m-1}(2\omega_2)v_{bs}^{\ l}(2\omega_2) \\ &\quad +l\cdot v_{gs}^{\ n}(2\omega_2)v_{ds}^{\ m}(2\omega_2)v_{bs}^{\ *}(\omega_1)v_{bs}^{\ l-1}(2\omega_2)]\end{aligned} \tag{A2}$$

In this, $*$ denotes the complex conjugate function.

Appendix II

The MOS transistor resistive nonlinearity can be extracted in many ways in time domain or in frequency domain. In this work we derived the non-linearity coefficients from simulations using Spectre and a well fitted PSP model. The PSP model is known to be able to correctly fit at least up to the third derivative [12, 13, 18]. Using a PSP model has advantages over getting derivatives from measurements mainly because measurement noise is largely eliminated: the PSP model can be used to accurately smoothen measurement results.

The resulting nonlinearity parameters scale (as a good approximation) linearly with transistor width which allows normalization with respect to transistor width. Furthermore, transistor length is assumed to be minimum. Then the nonlinearity parameters are mainly functions of port voltages, and need to be determined just once for each technology. Storing them in e.g. a look-up table then allows for computational efficient use in e.g. calculations.

As an example, the f_{210}^{ds} is extracted from simulations, as a function of V_{GS} and V_{DS} for a minimum length transistor, for the 90nm CMOS process used throughout this paper. The resulting contour plot of f_{210}^{ds} is shown in Fig. A1; for readability, $\lg(f_{210}^{ds}/1GHz)$ is plotted; the minimum value of 2 in the plot hence corresponds to $f_{210}^{ds} = 100$GHz. The plot indicates that at frequencies lower than 10 GHz, G_{210}^{ds} is dominant compared to C_{210}^{ds} and hence C_{210}^{ds} can be neglected.

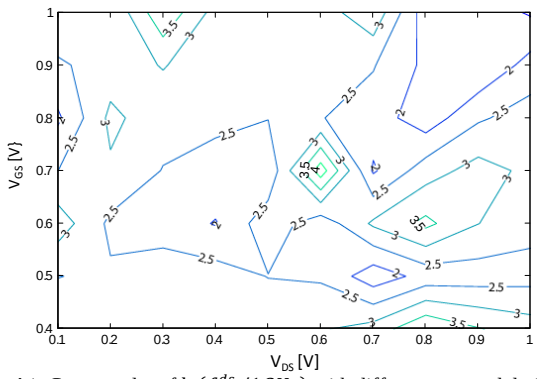

Fig. A1. Contour plot of $\lg(f_{210}^{ds}/1GHz)$ with different gate and drain bias.

Appendix III

The drain-source resistive nonlinearity of M_1, the drain-source resistive nonlinearity of M_2, the gate-source capacitive nonlinearity of M_2 and the bulk-source capacitive nonlinearity of M2 contribute to the IM_3 of the cascode amplifier shown in Fig. 2. Applying the general weak

nonlinearity model given in (3) to the cascode amplifier yields

$$v_{out}^{\omega_{IM3}} = \sum_K H_{M_1}^{ds}(\omega_{IM3}) \cdot \beta_{nml,M_1}^{\omega_D} G_{nml,M_1}^{ds} + \sum_K \beta_{nml,M_2}^{\omega_D} \cdot [H_{M2}^{ds}(\omega_{IM3}) \cdot G_{nml,M_2}^{ds} + H_{M_2}^{gs}(\omega_{IM3}) \cdot j\omega_{IM3} C_{nml,M_2}^{gs} + H_{M_2}^{bs}(\omega_{IM3}) \cdot j\omega_{IM3} C_{nml,M_2}^{bs}]. \quad \text{(A3)}$$

Using the model shown in Fig. A2(a) to calculate the H function, (A3) can be rewritten into

$$v_{out}^{\omega_{IM3}} = \sum_K \frac{-g_m^{M_2} r_{ds}^{M_1} \cdot R_{load}}{1 + g_m^{M_2} r_{ds}^{M_1}} \cdot \beta_{nml,M_1}^{\omega_D} G_{nml,M_1}^{ds} + \sum_K \frac{-R_{load}}{1 + g_m^{M_2} r_{ds}^{M_1}} \cdot \beta_{nml,M_2}^{\omega_D} \cdot [G_{nml,M_2}^{ds} - g_m^{M_2} r_{ds}^{M_1} \cdot j\omega_{IM3} C_{nml,M_2}^{gs} - g_m^{M_2} r_{ds}^{M_1} \cdot j\omega_{IM3} C_{nml,M_2}^{bs}]. \quad \text{(A4)}$$

For e.g. M_2, the relative importance between the gate-source capacitive nonlinearity, the bulk-source capacitive nonlinearity and the drain-source resistive nonlinearity can be determined by

$$f_{nml.M2}^{\frac{ds}{gs,bs}} = G_{nml,M_2}^{ds} / [g_m^{M_2} r_{ds}^{M_1} \cdot \omega_{IM3} (C_{nml,M_2}^{gs} + C_{nml,M_2}^{bs})] \approx G_{nml,M_2}^{ds} / [10\omega_{IM3} \cdot (C_{nml,M_2}^{gs} + C_{nml,M_2}^{bs})] \quad \text{(A5).}$$

Characterization of $f_{nml.M2}^{ds/(gs,bs)}$ shows that for M_2 in the cascode amplifier the dominant nonlinearity is the drain-source resistive nonlinearity. Then (A4) can be simplified to

$$v_{out}^{\omega_{IM3}} = \sum_K \frac{-g_m^{M_2} r_{ds}^{M_1} \cdot R_{load}}{1 + g_m^{M_2} r_{ds}^{M_1}} \cdot \beta_{nml,M1}^{\omega_D} G_{nml,M1}^{ds} + \sum_K \frac{-R_{load}}{1 + g_m^{M_2} r_{ds}^{M_1}} \cdot \beta_{nml,M2}^{\omega_D} \cdot G_{nml,M2}^{ds} \quad \text{(A6)}$$

Firstly assuming that the drain-source resistive nonlinearity related to the bulk-source voltage swing can be neglected, and secondly only including the third-order nonlinearity, we use the model shown in Fig.A2b to calculate the β functions, yielding equation (5) in section III.

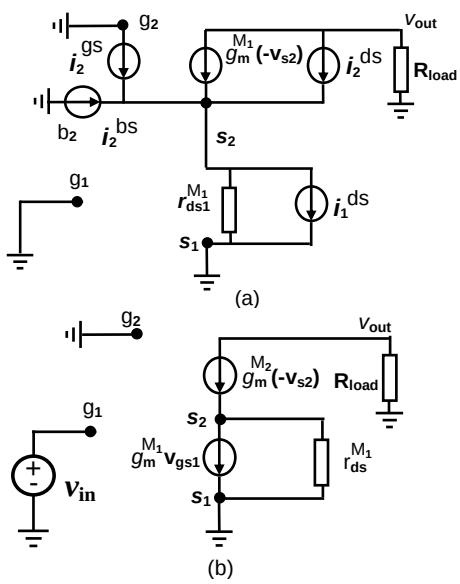

Fig.A2. (a) the equivalent model for calculating the H function. (b) the equivalent model for calculating the β functions.

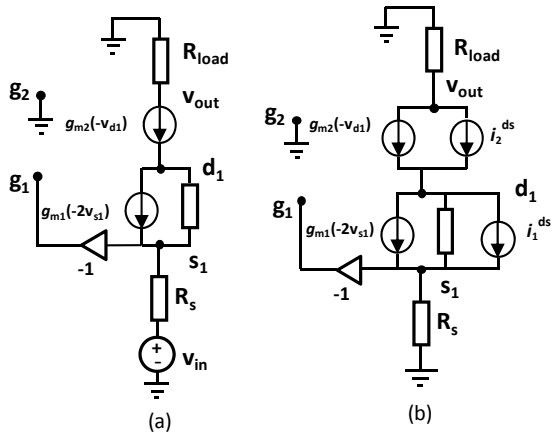

Fig.A3. (a) the equivalent model for calculating the β function and (b) the H functions in the CG LNA.

APPENDIX IV

For the CG LNA shown in Fig. 11b, assuming firstly that the resistive nonlinearity is dominant between the drain-source terminal, and secondly including only the third-order nonlinearities, the general weak nonlinearity model given in (3) can be rewritten as

$$v_{out}^{\omega_{IM3}} = \sum_K H_{M_1}^{ds}(\omega_{IM3}) \cdot \beta_{nml,M_1}^{\omega_D} G_{nml,M_1}^{ds} + \sum_K H_{M_2}^{ds}(\omega_{IM3}) \cdot \beta_{nml,M_2}^{\omega_D} G_{nml,M_2}^{ds} \quad \text{(A7).}$$

Assuming perfect input matching ($R_s = \frac{(g_{ds}^{M_1} + g_m^{M_2})}{g_m^{M_2}(g_{ds}^{M_1} + 2g_m^{M_1})}$), we use the model shown in Fig. A3 to calculate the H and β functions. Then (A7) can be rewritten as equation (8) in section IV.

APPENDIX V

The characterization of f_{nml}^{ks} is performed for minimum length MOS transistors with $V_{GS} = 1.2V$ and $V_{DS} \in (1uV, 0.1mV)$. It shows for the intermodulation distortion below 10GHz that the resistive nonlinearity is dominant between the drain-source terminal.

For the switch M_2 in Fig. 17 the nonlinearity between the gate-source terminal and bulk-source terminal can be neglected since the gate, bulk and source are ac connected. For the switch M_1 the gate-source terminal and bulk-source terminal can also be neglected since two large series resistors minimize the voltage swing v_{gs} and v_{bs}. As a result, only the drain-source resistive nonlinearities in M_1 and M_2 are considered. Applying the general weak nonlinearity model given by (3) to the attenuator yields

$$v_{out}^{\omega_{IM3}} = H_{M_1}^{ds} \sum_K \cdot \beta_{nml,M_1}^{\omega_{IM3}} G_{nml,M_1}^{ds} + H_{M_2}^{ds} \sum_K \cdot \beta_{nml,M_2}^{\omega_{IM3}} G_{nml,M_2}^{ds} \quad \text{(A8).}$$

In the equivalent model shown in Fig. A4, the input power source is modeled by the voltage source $v_s = 2v_{in}$ in series with R_s. Assuming a perfect input matching provided by the attenuator, the input voltage for the attenuator is v_{in} and the attenuation is defined by $A = v_{out}/v_{in}$. Let $R_x = R_1 + R_{on}^{M_1}$,

$R_y = R_2 + R_{on}^{M_2}$, $R_{load} = R_s$, for the input matching to R_s, we

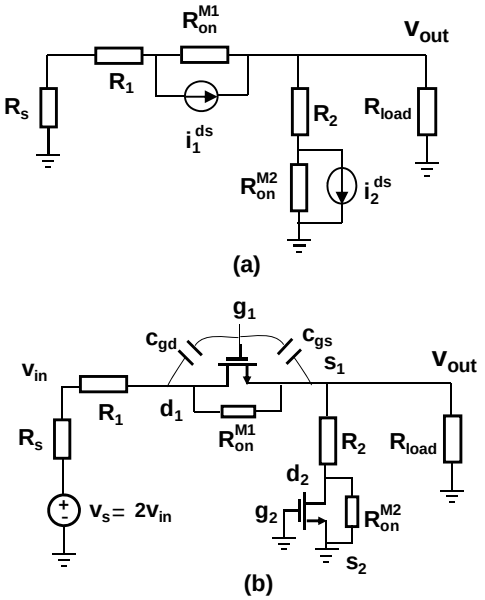

Fig.A4. (a) the equivalent model for calculating the H function. (b) the equivalent model for calculating the β functions.

have $R_x = R_s(1-A)$ and $R_y = A \cdot R_s/(1-A)$. Using the model shown in Fig. A4, the H functions and the voltage transfer functions for β functions in (A9) are given by

$$H_{M1}^{ds} = \frac{v_{out}}{i_1^{ds}} = \frac{A \cdot R_{on}^{M_1}}{2} \quad \text{(A9)}$$

$$H_{M2}^{ds} = \frac{v_{out}}{i_2^{ds}} = \frac{(2-A)\cdot(1-A)R_{on}^{M_2}}{2} \quad \text{(A10)}$$

$$\frac{v_{ds1}}{v_{in}} = \frac{R_{on}^{M_1}}{R_s} \quad \text{(A11)}$$

$$\frac{v_{gs1}}{v_{in}} = \frac{\frac{c_{gd}}{c_{gs}+c_{gd}} v_{ds1}}{v_{in}} = \frac{R_{on}^{M_1}}{2R_s} \quad \text{(A12)}$$

$$\frac{v_{ds2}}{v_{in}} = \frac{(1-A)R_{on}^{M_2}}{R_s} \quad \text{(A13)}$$

To the first-order approximation we only include the third-order nonlinearity, substituting (A9-A13) to (A8) yields equation (10) in section V.

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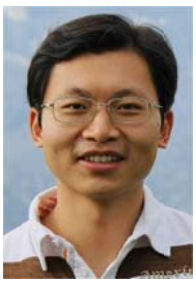

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