Spectral Analysis of Double-Sampling Switched-Capacitor Filters

J. J. F. Rijns and H. Wallinga, *Member, IEEE*

Abstract—**The double-sampling scheme (DSS) design technique is suitable for the realization of high-frequency switched-capacitor (SC) filters. This design technique effectively doubles the applicable frequency range of standard bi-phase SC filters. In practice, the particular nonideal properties of the double-sampling scheme result mainly in parasitic sidebands in the output spectrum. This paper describes the DSS design technique and gives a spectral analysis of double-sampling SC filters including the nonideal properties. With these results, the precise specifications for the pre- (anti-aliasing) and postfilter are derived. An excellent matching between the analytical description and experimental results is found for a bilinear fifth-order elliptic double-sampling SC low-pass filter, designed for video frequency applications.**

I. Introduction

SC filters are commonly used in voice and audio frequency communication circuits [1]. An extension of the signal bandwidth to the megahertz (video) range imposes severe requirements on the (active) filter components, since the bandwidths of the continuous-time subcircuits have to exceed the signal bandwidth largely for an accurate charge transfer between the switched-capacitors [2]. Many design techniques and synthesis methods that are suitable for SC filter applications up to the sub-megahertz frequency range have been published, e.g., [3]. The applicable frequency range of an SC design is particularly determined by the relation between the number of clock phases, the number of sampling phases, and the maximum available settling time for the charge transfer that is provided by the design technique.

A design technique for the realization of high-frequency SC filters has to be based on a minimal number of clock phases and a maximal number of sampling phases. The double-sampling scheme (DSS) [4] satisfies these conditions and has proven to be suitable for the design of SC video filters [5]–[7]. The combination of this design technique and an exact filter synthesis using the bilinear $s-z$ transform [8] makes an SC filter realization possible with a sample rate equal to twice the clock frequency and a very low ratio between the clock frequency and the filter cutoff frequency. In practice, the double-sampling scheme suffers from two nonideal properties, i.e., path gain errors and nonuniform sampling. This paper describes the influences of these nonidealities on the output spectrum of DSS SC filters. Accurate specifications for the analog pre- and postfilters are derived, based on the analytical results and the filter characteristic.

In Section II, it is explained that a double-sampling SC filter realization can be based on any standard bi-phase design. The double-sampling scheme is discussed and it is shown that this technique doubles the applicability frequency range of bi-phase SC filters by doubling of the effective settling time for the charge transfers. After the description of the ideal DSS, the practical nonideal properties, path gain errors and nonuniform sampling, are introduced.

Section III describes the effects of these properties of the double-sampling scheme on the output spectrum of SC filters in practice. The analysis is focused on the design of low-pass and bandpass SC filters with a low sensitivity to element variations. For the experiment verification of the analytical results of Section III, a bilinear fifth-order elliptic SC low-pass ladder filter, originally designed for video frequency applications [7], is chosen as vehicle. Additionally, a comparison of the experimental performance results of this video frequency SC filter in a single- and double-sampling implementation is given as an illustration of the DSS potentials. The last section of this paper comprises the conclusions.

II. Properties of the Double-Sampling Design Technique

SC circuits can operate on minimally two clock phases. At least one phase is required to precharge the capacitors and one phase is required for the charge transfer. Design techniques using more than two clock phases are not suitable for the realization of high-frequency SC filters, since the available settling time for the charge transfer is inversely proportional to the number of clock phases for a fixed clock frequency. For this reason and because of the need for stray insensitivity, the realization of high-frequency SC filters should be based on the use of stray-insensitive bi-phase SC integrators [9], shown in Fig. 1. Depending on the switch operation, an inverting and a noninverting integrator can be realized. Since only one

Manuscript received March 19, 1990. This work was supported by the Dutch Program for Innovative Research under Grant IOP IC-TEL 46.011. This paper was recommended by Associate Editor M. Ismail.

The authors are with the Department of IC-Technology and Electronics, MESA Institute, University of Twente, 7500 AE Enschede, The Netherlands.

IEEE Log Number 9102880.

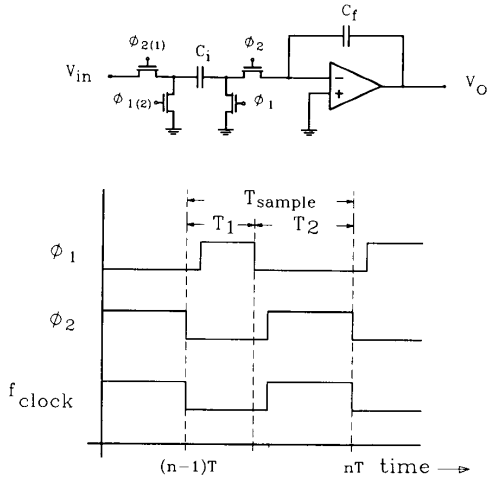

Fig. 1. Stray-insensitive SC integrator with bi-phase timing diagram.

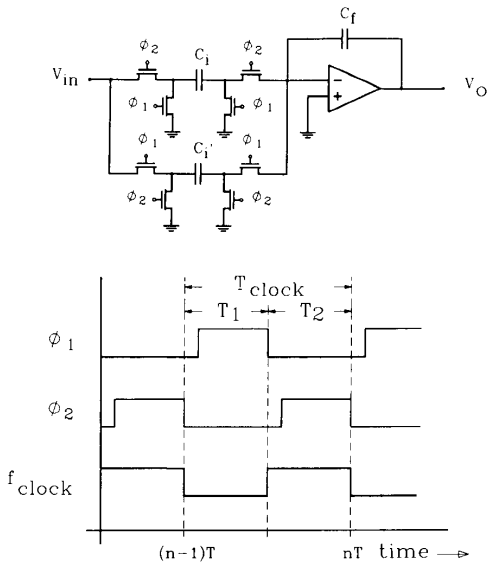

Fig. 2. DSS inverting SC integrator with bi-phase timing diagram.

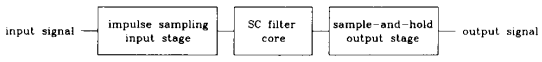

Fig. 3. System block diagram of an SC filter.

switch samples the input voltage, all signals in SC circuits built with these bi-phase integrators will have a uniform periodicity, independent of the equality of the delays T_1 and T_2 between two successive clock phases. Since the sample rate is equal to the clock frequency, incorporating the uniform sampling property, this design technique will be denoted as the single-sampling scheme (SSS). Inherent to the SSS design technique, all amplifiers that realize the high-impedance charge redistribution circuit nodes are active for signal processing during only one half of the clock period.

In SC filters using the double-sampling scheme (DSS), both clock phases are used as sampling phases. This operation can be implemented by a doubling of all SC (time-variant) branches of the single-sampling SC filter version and driving them by opposite clock phases. Fig. 2 shows the double-sampling implementation of the stray-insensitive inverting SC integrator with the timing diagram. The output signal of each filter stage is sampled at both clock phases, resulting in a sample frequency equal to twice the clock frequency for an ideal timing diagram ($T_1 = T_2$). The frequency response of the ideal double-sampling SC circuit can be obtained from the single-sampling version using the transformation $z \Rightarrow z^{1/2}$ with $z \equiv \exp(sT)$. The use of two-integrator loops consisting of a delay-free inverting integrator and a delaying noninverting integrator prevents a fully continuous-time coupling of all filter sections. Note that the operation of DSS SC circuits is not equal to a parallel operation of the single-sampling version as in N-path circuits [10].

If the sample rate and the capacitor ratios are chosen equal for a single-sampling and double-sampling SC filter design, both realizations have the same filter time constants. In this situation, the available settling time for the charge transfers by the (active) DSS filter components is doubled with respect to those of the SSS implementation, since the clock frequency of the DSS is half that of the SSS to obtain equal sample rates for both schemes. The price for the DSS is the doubling of all switched-capacitors and associated switches with respect to the SSS. Since all unswitched-capacitors and amplifiers are implemented singularly, the increase of the total chip area of the DSS will be much smaller than a factor two.

Until now, the ideal double-sampling scheme is described using a uniformly distributed sample sequence and an ideal matching between the capacitors of the two parallel charge transfer paths. In practice however, the equality of the charge transfers of both paths is affected by mismatches of the SC pairs. This effect will be denoted as "path gain errors," and it is described in detail in the next section. Moreover, the uniform sampling property will be violated by a difference in the delay (clock skew) between two successive sampling phases. This skew is unavoidable if the clock phases are generated from a clock signal with a frequency equal to half the ideal sampling frequency as indicated in Fig. 2, with $T_1 \neq T_2$. The nonuniform sampling sequence can be interpreted as the sum of two mutually time shifted uniform distributed sequences, both periodic with the clock period T.

In the next section, the influence of these particular nonideal properties on the DSS SC filter output spectrum will be analyzed using the general system block diagram of Fig. 3. This model allows us to study the effects of nonidealities of one of these SC filter function blocks on the performance of the total system by distinguishing between the sampling process and the filtering action.

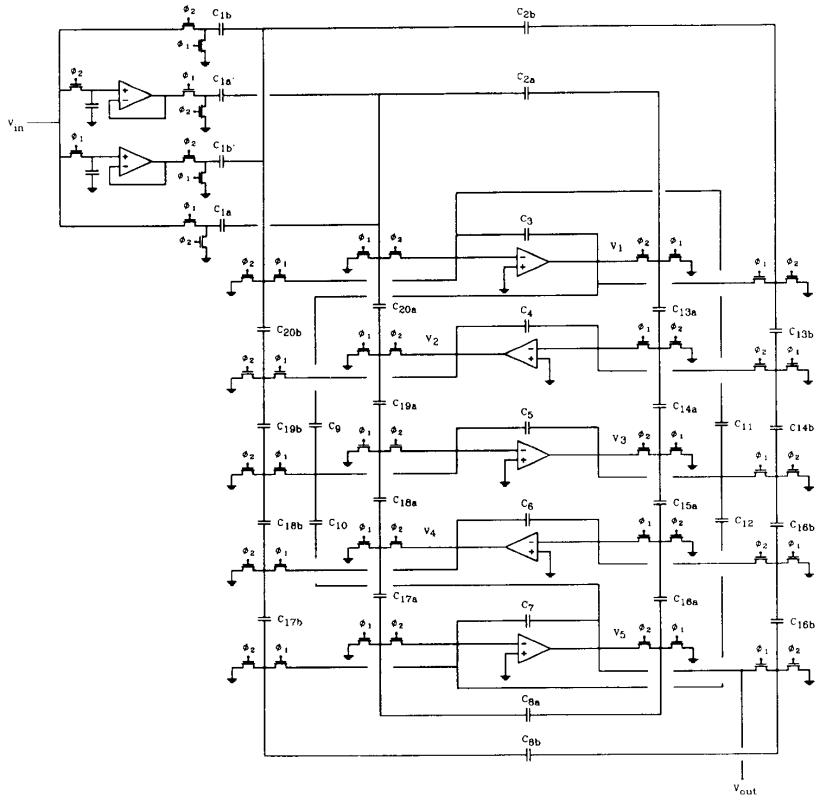

Fig. 4. Double-sampling bilinear fifth-order elliptic SC low-pass ladder filter.

The input stage transforms the analog input signal into an analog sampled-data signal with the use of one or more impulse sampling (SI) functions. The output spectrum of the SI input stage consists of replicas of the continuous-time input signal spectrum. The periodicity and shape of its output spectrum depends on the uniformity of the sampling sequence. The SC filter core can now be interpreted as a discrete-time calculator, constructing a new output signal sample out of current or previous output and/or input signal samples. The sample-and-hold (SH) output stage receives these output signal samples and transforms the sequence into a staircase signal. This transformation is mathematically modeled using the unit-step function. Notice that the hold times of the SH output signal are determined by the timing of the sampling sequence.

III. The Nonideal DSS

The accuracy of SC filter time constants is determined by the settling accuracy of the continuous-time subcircuits, the matching accuracy of the capacitors and the uniformity of the sampling sequence. The influence of deviations of the filter coefficients on the frequency response depends on the filter structure. The double-terminated LC ladder structure is commonly used in high-performance applications because of its low-sensitivity property [13]. In the next part of this paper, the analysis will therefore be focused on the design of SC ladder filters, although the results can be applied to all SC filter structures with a low sensitivity to element variations.

An independent spectral analysis will be given of the influence of path gain errors and a nonuniform sampling operation on double-sampling SC ladder filters. For the verification of the analytical results, a bilinear SC low-pass ladder filter is chosen as vehicle satisfying the following specifications, normalized on the sample frequency [7]

- maximum passband ripple A_P: -0.5 dB,
- minimum stopband attenuation A_S: -50 dB,
- passband: 0–0.1,
- stopband: 0.15–0.5. (1)

The SC filter is designed according to a standard filter synthesis method [8]. Both a single- and a double-sampling implementation has been realized. The double-sampling SC ladder filter implementation is shown in Fig. 4. All switched-capacitors indexed "b" with the associated switches are omitted in the standard SSS version. Both SC filters are designed for operation on a 25-MHz clock frequency, resulting in an effective sample frequency of

25 MHz for the SSS version and 50 MHz for the DSS version. For the verification of the analytical results of this section, however, the clock frequency is reduced to 1 MHz (passband 0–200 kHz) in order to exclude the finite bandwidths effects of the SC filter components and the duty cycle inaccuracy of the external master clock (HP 8112 generator with a duty cycle accuracy $\pm 5\%$ and ± 2 ns).

A. The Influence of Path Gain Errors on the Output Spectrum of DSS SC Ladder Filters

The filter coefficients of single-sampling integrator based SC filters are determined by the ratio of all input capacitors to the integrator capacitance. The accuracy of these capacitor ratios is limited by capacitor mismatches. Analogous is the accuracy of double-sampling SC filter coefficients determined by the ratio accuracy of the input capacitors of both charge transfer paths to the integrator capacitor. Under condition of a uniform sampling operation results a mismatch between the two parallel input capacitors of both paths, a path gain error, in two discrete-time charge flows with an unequal magnitude and a periodicity equal to the clock period. The capacitor matching of each separate path determines the accuracy of the filter coefficients. Since both path charge flows are periodic with the clock period, which is twice the ideal sample period, the path gain error causes parasitic sidebands in the filter output spectrum.

The sampling capacitors of the nonrecursive input branch of the SC filter have a special function on the filter characteristic, since they determine the maximum filter gain. Referring to the system block diagram of Fig. 3 and exploiting the low-sensitivity property of the SC filter core, the influence of capacitor mismatches on the output spectrum of SC ladder filters can be modeled by the nonideal functioning of the input stage. The number of capacitors and the frequency dependency of the transfer function of this branch depends on the applied synthesis method and the stray sensitivity of the input branch. The single-sampling bilinear synthesis of the resistive source impedance of the double-terminated ladder filter requires an input branch with a Z-domain voltage-charge transfer function $K(1+z^{-1})$. In a standard SSS stray-insensitive implementation, this input branch consists of one delay-free and one full period delay SC branch with capacitors C_{1a} and C_{1b} with nominally equal values, realizing a voltage-charge transfer function $\Delta Q(z)/V_{\text{in}}(z) = C_{1a} + C_{1b}z^{-1}$. A deviation from the ideal capacitor matching, i.e., $C_{1a} = C$, $C_{1b} = C(1-\delta)$, and $\delta \neq 0$, modifies $\Delta Q(z)/V_{\text{in}}(z)$ into $C(1+z^{-1}) - \delta C z^{-1}$, which corresponds to a transmission zero in the filter response at half the sample frequency with a finite Q-factor. The consequence of this capacitor mismatch for low-pass and bandpass filters with a stopband located around half the sample frequency is a minor, nearly frequency-independent gain error in the filter passband. For a single-sampling LDI synthesis of the resistive source impedance of the double-terminated LC ladder filter, a capacitor mismatch in the SC input branch with the voltage-charge transfer function $\Delta Q(z)/V_{\text{in}}(z) = K$ results in an exact frequency independent gain error. The neglect of the minor frequency dependency of the passband gain error of the SSS bilinear input stage makes the effects of capacitor mismatch on this input branch analogous to that of the SSS LDI input branch.

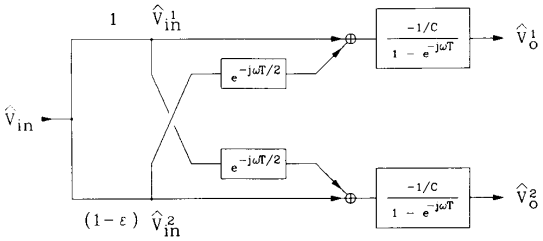

Fig. 5. Equivalent continuous-time system for the DSS integrator with path gain error ϵ.

Based on the previous discussion, the influence of path gain errors in double-sampling SC filters will be modeled as a gain error of the input stage, independent of the input branch structure with the use of two uniform sampling sequences, periodic with the clock frequency ω_T and mutually time shifted by half the clock period T. The uniform sampling property results in uniform hold times of the output signals which allows us to use an impulse sampling operation for the spectrum analysis of these path gain errors. The path gain error ϵ is defined as the capacitor mismatch between the parallel sampling capacitors of the two paths of the double-sampling input branch. Note that the effects of capacitor mismatch on all other filter capacitances will simply affect the accuracy of the filter poles and zeros.

The output spectrum of the inverting integrator of Fig. 2 will be derived for illustration. The path gain error ϵ, caused by a capacitor mismatch of the input capacitances C_i and C_i' is modeled by the capacitor values: $C_i = 1$, $C_i' = (1-\epsilon)$, $C_f = C$. The discrete-time signals $v_{\text{in}}^1(t)$, $v_{\text{in}}^2(t)$, $v_0^1(t)$, and $v_0^2(t)$ are given by

$$
\begin{aligned}
v_{\text{in}}^1(t) &= \hat{v}_{\text{in}}(t) \sum_{n=-\infty}^{n=+\infty} \delta(t-nT) \\
v_{\text{in}}^2(t) &= (1-\epsilon)\hat{v}_{\text{in}}(t) \sum_{n=-\infty}^{n=+\infty} \delta(t-nT-T/2) \\
v_0^1(t) &= \hat{v}_0^1(t) \sum_{n=-\infty}^{n=+\infty} \delta(t-nT) \\
v_0^2(t) &= \hat{v}_0^2(t) \sum_{n=-\infty}^{n=+\infty} \delta(t-nT-T/2). \qquad (2)
\end{aligned}
$$

The signals $v_{\text{in}}(t)$ and $v_0^i(t)$ are defined as discrete-time versions of respectively the continuous-time signals $\hat{v}_{\text{in}}(t)$ and $\hat{v}_0^i(t)$. The discrete-time frequency response can be derived using an equivalent continuous-time system [12]–[14] as illustrated in Fig. 5. The discrete-time output

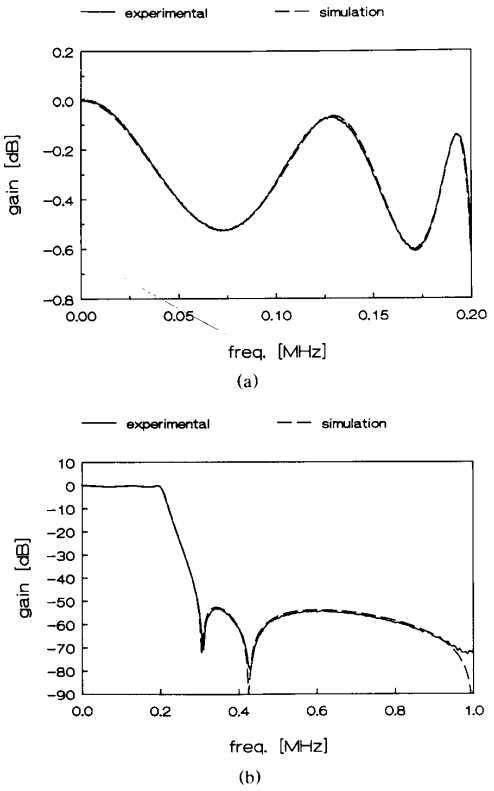

Fig. 6. Experimental and simulated frequency response of the DSS SC filter for a clock frequency of 1 MHz. (a) Passband. (b) Overall frequency response.

spectrum of the integrator can be written as [$\omega' = \omega - n\omega_T$, $\omega_T = 2\pi/T$, $v_0(t) = v_0^1(t) + v_0^2(t)$]:

$$V_0(\omega) = -\frac{\frac{1}{T}\sum_{n=-\infty}^{n=+\infty}\left[\hat{V}_{\text{in}}^1(\omega') + \hat{V}_{\text{in}}^2(\omega')e^{-j\omega' T/2} + \hat{V}_{\text{in}}^2(\omega') + \hat{V}_{\text{in}}^1(\omega')e^{-j\omega' T/2}\right]}{C\left[1 - e^{-j\omega' T}\right]}. \tag{3}$$

Rewriting of this equation gives

$$V_0(\omega) = -\frac{\frac{1}{T}\sum_{n=-\infty}^{n=+\infty}\hat{V}_{\text{in}}(\omega')}{C\left[1 - e^{-j\omega' T}\right]}\left\{\left[1 + (1-\epsilon)e^{-j\omega' T/2}\right] + \left[(1-\epsilon) + e^{-j\omega' T/2}\right]e^{-jn\pi}\right\}$$

$$= -\frac{\frac{2}{T}\sum_{n=-\infty}^{n=+\infty}\hat{V}_{\text{in}}(\omega - n\omega_T)}{C\left[1 - e^{-j(\omega - n\omega_T)T/2}\right]}K(n); \qquad \begin{aligned} &\text{with } K(n) = 1 - \epsilon/2 \quad \text{for } n \text{ even} \\ &\qquad\quad = \epsilon/2 \quad\quad\ \text{for } n \text{ odd.} \end{aligned} \tag{4}$$

For an analog input spectrum bandlimited to the Nyquist frequency (the clock frequency ω_T) of the ideal DSS uniform sampling sequence, the baseband of the output spectrum is found to have a frequency-independent amplitude shift of $1 - \epsilon/2$ and an alias component level of $\epsilon/2$. Using careful layout techniques, the path gain error ϵ can be limited to a few hundred ppm, resulting in an alias level of -50 to -70 dB. Fig. 6(a) and (b) show the experimental frequency response of the DSS SC filter for a 1-MHz clock frequency with an exact 50% duty cycle (2-MHz sample frequency). The experimental passband response shows an excellent matching with the ideal response. The effects of the path gain errors are only perceptible around at the end of the passband, confirming the theory. The first spurious sideband (4) is caused by both the capacitor mismatches between the two paths of the DSS bilinear input and by the capacitor mismatches in one of each paths, and results in a finite stopband attenuation at 1 MHz. The measurement results indicated a path gain error ϵ of approximately 500 ppm.

B. The Influence of Nonuniform Sampling on the Output Spectrum of SC Ladder Filters

As mentioned before, the nonuniform bi-phase sampling sequence can be described using two mutually time-shifted uniform sampling sequences, periodic with the clock frequency. This type of nonuniform sampling is known as bunched or recurrent sampling [15]–[17]. Due to the difference in the delay between two successive sampling instants, the applied $s - z$ transformation (based on the ideal double-sampling situation) is distorted and will cause deviations of the frequency response of the SC filter core (Fig. 3). The average delay between two successive sampling instants of half the clock period T makes these deviations negligible for frequencies far below the clock frequency. The relation between the sampling instants of the SI input stage and the hold times of the SH output stage results in the presence of parasitic sidebands in the output spectrum and a nonuniform SH sinc distortion in the filter baseband.

The output spectrum of the integrator of Fig. 2 will be derived for a nonuniform sampling sequence with a sample timing error $\alpha T/2$ and capacitor values: $C_i = C_i' = 1$, $C_f = C$. The nonuniform sampling operation can be modeled using the following discrete-time signals $v_{\text{in}}^1(t)$, $v_{\text{in}}^2(t)$,

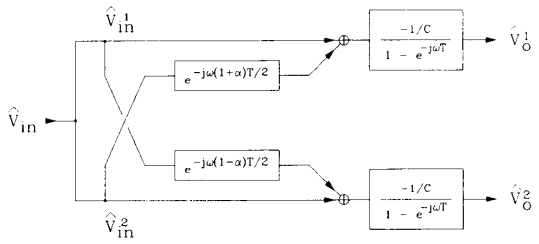

Fig. 7. Equivalent continuous-time system for the DSS integrator with a relative sample timing error α.

$v_0^1(t)$, and $v_0^2(t)$:

$$v_{in}^1(t) = \hat{v}_{in}(t) \sum_{n=-\infty}^{n=+\infty} \delta(t - nT)$$

$$v_{in}^2(t) = \hat{v}_{in}(t) \sum_{n=-\infty}^{n=+\infty} \delta(t - nT - (1-\alpha)T/2)$$

$$v_0^1(t) = \hat{v}_0^1(t) \sum_{n=-\infty}^{n=+\infty} \delta(t - nT)$$

$$v_0^2(t) = \hat{v}_0^2(t) \sum_{n=-\infty}^{n=+\infty} \delta(t - nT - (1-\alpha)T/2). \quad (5)$$

From the equivalent continuous-time system in Fig. 7, the SH output spectra of the integrator are obtained [$\omega' = \omega - n\omega_T$, $\omega_T = 2\pi/T$, $v_0(t) = v_0^1(t) + v_0^2(t)$]:

$$V_{0,SH}^1(\omega) = -\frac{\sum_{n=-\infty}^{n=+\infty} \left[\hat{V}_{in}^1(\omega') + \hat{V}_{in}^2(\omega') e^{-j\omega'(1+\alpha)T/2}\right]}{C[1 - e^{-j\omega' T}]} \cdot \frac{[1 - e^{-j\omega(1-\alpha)T/2}]}{j\omega T}$$

$$V_{0,SH}^2(\omega) = -\frac{\sum_{n=-\infty}^{n=+\infty} \left[\hat{V}_{in}^2(\omega') + \hat{V}_{in}^1(\omega') e^{-j\omega'(1-\alpha)T/2}\right]}{C[1 - e^{-j\omega' T}]} \cdot \frac{[1 - e^{-j\omega(1+\alpha)T/2}]}{j\omega T}. \quad (6)$$

This equation shows the effect of the sample timing error $\alpha T/2$ on both the discrete-time frequency response and on the SH distortion function. The total output spectrum of the integrator equals the sum of these two spectra. Using the approximation

$$[1 + e^{-j\omega'(1-\alpha)T/2}] \simeq [1 + e^{-j\omega'(1+\alpha)T/2}] \simeq [1 + e^{-j\omega' T/2}] \quad (7)$$

the influence of a small variation in the location of a transmission zero around the clock frequency on the SC circuit transfer function is neglected. Under this condition, the total SH output spectrum of the integrator can be written as the product of the ideal DSS integrator transfer function and the output spectrum of the combined SI input and SH output stage (Fig. 3):

$$V_{0,SH}(\omega) = -\frac{\sum_{n=-\infty}^{n=+\infty} \hat{V}_{in}(\omega')\{[1 - e^{-j\omega(1-\alpha)T/2}] + [1 - e^{-j\omega(1+\alpha)T/2}] e^{-jn\pi(1-\alpha)}\}}{C[1 - e^{-j\omega' T/2}] j\omega T}$$

$$= -\frac{\sum_{n=-\infty}^{n=+\infty} \hat{V}_{in}(\omega - n\omega_T)}{C[1 - e^{-j(\omega - n\omega_T)T/2}]} \mathrm{SH}(\omega, n). \quad (8)$$

As shown in the Appendix, the modulus of the modified SH sinc function SH(ω, n) can be approximated by

$$|\mathrm{SH}(\omega,n)| = |\sin((\omega - n\omega_T)T/4)\cos(\alpha\omega T/4)/(\omega T/4)|, \quad \text{for } n \text{ even}$$
$$= |\sin((\omega - n\omega_T)T/4)\sin(\alpha\omega T/4), (\omega T/4)|, \quad \text{for } n \text{ odd}. \quad (9)$$

Note that the SH output spectrum of the ideal double-sampling SC filter only has sidebands at the integer multiples of the sample frequency (the even integer numbers of the clock frequency), distorted by the ideal SH sinc function

$$|\sin((\omega - n\omega_T)T/4)/(\omega T/4)| = |\sin(\omega T/4)/(\omega T/4)|.$$

According to this analysis, the output spectrum of the SC filter with a nonuniform sampling operation can be approximated by the product of the ideal DSS periodical filter frequency response and (9). This is true for an analog input spectrum bandlimited to half the clock frequency, which is the Nyquist frequency of each of the two separate sampling functions. Fig. 8 shows the experimental amplitudes of the first parasitic filter sideband for $f_{clock} = 1$ MHz and input frequencies from dc to 200 kHz (the passband frequency range) for three values of the relative sample timing error α in combination with the analytical data according to (9). Even for the large values of α, an excellent matching of the measurements with the theory is observed.

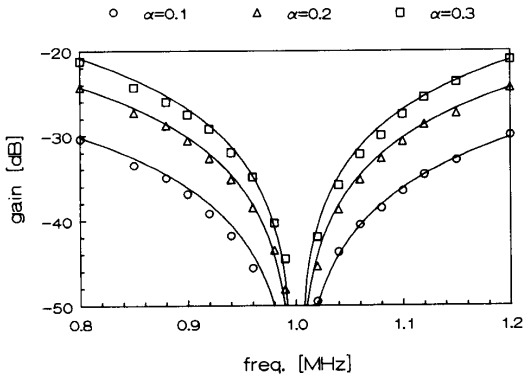

Fig. 8. Amplitudes of the first parasitic sideband of the DSS SC filter for $f_{clock} = 1$ MHz, input frequencies in the range $\langle 0, 0.2$ MHz$\rangle$ and $\alpha = 0.1$, 0.2, and 0.3. Markers are experimental values, solid curves are analytical data according to (9).

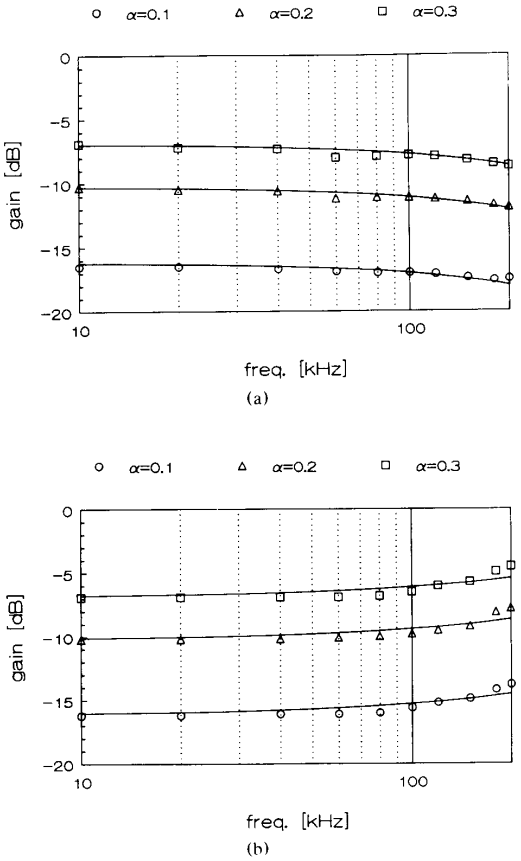

Fig. 9. Alias components in the baseband of the DSS SC filter for $f_{clock} = 1$ MHz and a relative sampling timing error $\alpha = 0.1$, 0.2, and 0.3. Markers are experimental values, solid curves are analytical data according to (11) for input frequencies (a) ⟨0.8 MHz, 1 MHz⟩ and (b) ⟨1.0 MHz, 1.2 MHz⟩.

In order to derive accurate specifications for the analog anti-aliasing (pre-) and postfilter, the spectrum deviations and alias components level have to be predicted for an input spectrum exceeding the Nyquist frequency of the two separate sampling functions.

Obviously, the frequency folding mechanisms for input frequencies around the first multiple of the clock frequency ($\omega_T/2 \leq \omega \leq 3\omega_T/2$) will determine these requirements. Based on (9), input frequencies $\omega_T \pm \omega$ with $\omega \leq \omega_T/2$ will cause alias components at ω with an amplitude

$$|A(\omega)| \simeq |\sin((\omega_T \pm \omega)\alpha T/4)\sin(\omega T/4)/(\omega T/4)| \tag{10}$$

or, neglecting the very small effect of the sinc distortion in the baseband

$$|A(\omega)| \simeq |\sin(\pi\alpha/2 \pm \alpha\omega T/4)|. \tag{11}$$

Fig. 9(a) and (b) show the experimental alias components

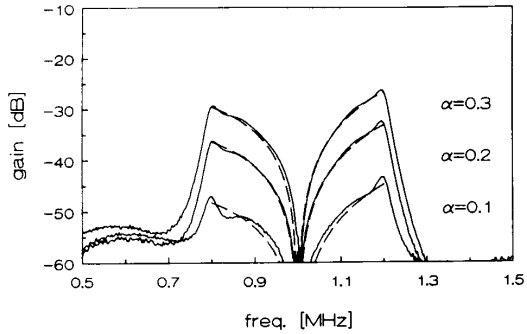

Fig. 10. Frequency response of the DSS SC filter for $f_{clock} = 1$ MHz and a relative sampling timing error α of 0.1, 0.2, and 0.3. Solid curves are experimental values, dashed curves are analytical results for the input frequency range ⟨0.8 MHz, 1.2 MHz⟩.

for input frequencies in the range 0.8 MHz to 1.2 MHz together with the analytical data according to (11) for a relative sample timing error α of 0.1, 0.2, and 0.3. This figure also shows a very close matching of the experimental results and the theory. Due to the frequency folding mechanism caused by the nonuniform sampling operation, input frequencies in the range ($\omega_T/2 \leq \omega \leq 3\omega_T/2$) appear as alias components in the baseband of the DSS SC filter output spectrum. These image frequencies are therefore located below the Nyquist frequency of the two sampling functions; see (5). As shown experimentally in Fig. 8, (9) describes the folding forward mechanism of these baseband frequencies accurately. The image frequencies of input frequencies in the range ($\omega_T/2 \leq \omega \leq 3\omega_T/2$) will therefore appear in the same frequency range with a theoretical amplitude given by the product of (9) and (11). Depending on the filter characteristic, these image frequency components may have larger amplitudes than the original frequency components, especially for low-pass and bandpass filters with a large stopband attenuation around the clock frequency. As an illustration, Fig. 10 gives the frequency response of the DSS SC filter for a clock frequency of 1 MHz and a relative sample timing error α of 0.1, 0.2, and 0.3. The solid curves represent the experimental values and dashed curves are the analytical results obtained from the product of the expressions in (9) and (11) for the input frequency range 0.8 MHz to 1.2 MHz. A very close matching of measurements and theory is again observed.

In this section, the use of the system block diagram of Fig. 3 allowed us to separate the influences of the nonideal DSS on the SC filter output spectrum in deviations of the SC filter transfer function due to deviations of the associated pole/zero pattern and in a modification of the output spectrum due to the nonideal sampling process. Depending on the filter sensitivity and the filter type (e.g., low-pass), the influence of the deviations of the filter transfer function may be neglected with respect to the deviations caused by the sampling process. This experimentally verified theory on the effects of nonideal DSS

TABLE I
AAF SPECIFICATIONS FOR DSS SC LOW-PASS FILTERS WITH A RELATIVE SAMPLE TIMING ERROR α

Frequency	Gain SCF	Gain AAF
dc	0	0
f_{pass}	A_{pass}	0
$f_{clock} - f_{pass}$	A_{stop}	$A_{stop} - 20\log(\sin(\pi\alpha/2 - \alpha\pi f_{pass}/2f_c))$
$2f_{clock} - f_{stop}$	A_{stop}	A_{stop}

SC filters will now be used to obtain accurate specification for the analog pre- and postfilter.

The anti-aliasing filter (AAF) is necessary to bandlimit the analog input spectrum in order to limit the alias component level in the SC filter baseband. Since the two sampling functions modeling the DSS sampling process have a periodicity equal to the clock period, a path gain error and an unequal mutual delay between the sample sequences will cause the aliasing of input frequencies above half the clock frequency in the DSS SC filter baseband. Equations (4) and (9) give an approximation of the amplitudes of the alias components as a function of respectively the path gain error ϵ and of the relative sample timing error α. In practice, the path gain errors ϵ will be limited to a few hundred parts per million. Consequently, the alias component level and the deviations of the DSS SC filter output spectrum will be dominated by the relative sample timing error α. The latter depends on the magnitude of the clock period and the systematic clock skew generated by the clock circuit. With the use of full-custom clock circuits, α can be limited to a few percent for clock frequencies up to 25 MHz [7].

The specifications for the AAF can now simply be obtained from the filter specifications and (9). The filter clock frequency is denoted by f_c, the filter cutoff frequency by f_{pass} and the stopband start frequency by f_{stop}. If the maximum alias component level is set to the minimum stopband attenuation, then the combination of (1) and (11) results in the AAF specifications of Table I. Both filter passband ripple A_{ripple} and stopband attenuation A_{stop} are assumed to be defined in decibels. For filters with a passband gain unequal to 0 dB, the stopband attenuation A_{stop} simply has to be defined as the difference between the filter passband and stopband gain. Analogously results in the combination of the filter specifications (1) and (9) in the specification of the analog postfilter (APF) as shown in Table II.

In the previous part of this section, the effects of practical nonidealities of double-sampling SC filter have been described analytically and verified with experimental results of a bilinear fifth-order elliptic double-sampling SC low-pass filter, designed for video frequency applications [7]. The basic theoretical advantage of the DSS design technique is the effectively doubling of the settling time of the amplifiers in comparison to the SSS implementation, operating at the same sampling rate. This is of course only of interest for very high (video) frequency applications. Therefore, the experimental results of the test filter in DSS and SSS implementation for video frequency operation are now summarized to illustrate the DSS potentials.

In the realizations, BiCMOS folded-cascode amplifiers are used with an experimental dc-gain of 68 dB and a unity-gain frequency of 98 MHz for a 3-pF capacitive load. The switches are CMOS transmission gates with effective dimensions $60/2$ μm, the unit capacitor value is 0.28 pF. Table III lists the capacitor values after a scaling operation based on a combined dynamic range and settling speed optimization. The four-phase nonoverlapping clock signals are generated on-chip using BiCMOS logic. The systematic clock skew is measured to be 1 ns ($\alpha = 25\%$ for a 25-MHz clock frequency), while the transient time is typically 2.8 ns. The experimental frequency response of the single-sampling SC filter is shown in Fig. 11 for a clock frequency of 10 and 25 MHz. The double-sampling frequency response is shown in Fig. 12 for a clock frequency of 12.5 and 25 MHz. The spurious sideband is clearly shown in Fig. 12(b) for the 12.5 MHz clock frequency. Table IV lists the major performance results of both filter realizations for different clock frequencies. The results of the 2.5-MHz cutoff frequency SSS and the 5.0-MHz DSS SC filter version are practically equal, both operating on a 25-MHz clock frequency. For equal bandwidths of the active components of the SSS and DSS SC filter, the effective doubling of the DSS sample rate with respect to the SSS version results in an effective doubling of the applicable signal frequency range.

IV. CONCLUSIONS

This paper describes the practical consequences of the use of the double-sampling design technique for SC ladder filters. It is shown that in practice, the timing accuracy of the sampling instants is a more critical design parameter than the matching accuracy of the SC pairs. The nonuniformity of the sampling sequence causes errors in the filter coefficients due to deviations in the applied $s - z$ transformation and leads to different hold times in the SH output signals.

Depending on the filter structure and filter type, the deviations of the SC filter core transfer function are found to be negligible to the deviations caused by the nonideal sampling process. In this case, the output spectrum can be described as the product of the modified output spectrum of the combined input and output sampling stage and the ideal transfer function of the DSS SC filter. Using minor approximations, very compact formulas are derived for the description of the parasitic sidebands and alias components of the filter SH output spectrum, which is used to derive accurate specifications for the analog pre- and post filters. The experimental results of a fifth-order bilinear low-pass ladder filter shows an excellent matching between the analytical and measured results for a large relative sample timing error, which legitimizes the approximations made in the analysis.

The theoretical results are based on signal reconstruction by the incorporated zero-order SH function. Since

TABLE II
APF SPECIFICATIONS FOR DSS SC LOW-PASS FILTERS WITH A RELATIVE SAMPLE TIMING ERROR α

Frequency	Gain SCF	Gain APF
dc	0	0
f_{pass}	A_{pass}	0
$f_{clock} - f_{pass}$	A_{stop}	$A_{stop} - 20\log\left[\sin(\pi f_{pass}/2f_c)\dfrac{\sin(\alpha\pi f/2f_c)}{\pi f/2f_c}\right]$
$2f_{clock} - f_{stop}$	A_{stop}	A_{stop}

TABLE III
CAPACITOR VALUES, SCALED FOR DYNAMIC RANGE AND SETTLING SPEED

$V_{1,max} = -2.53$ dB, $V_{2,max} = 2.97$ dB, $V_{3,max} = 0$ dB
$V_{4,max} = 2.97$ dB, $V_{5,max} = 0$ dB

Capacitor	Unit Value	Capacitor	Unit Value
C_1 (2x)	1.5697	C_{11}	1.0000
C_2	3.4181	C_{12}	1.3872
C_3	7.9026	C_{13}	1.3075
C_4	2.0456	C_{14}	1.0000
C_5	9.0099	C_{15}	1.6653
C_6	2.6929	C_{16}	1.0000
C_7	2.4335	C_{17}	1.9286
C_8	1.0000	C_{18}	2.3153
C_9	1.0000	C_{19}	2.3966
C_{10}	1.0000	C_{20}	3.1337

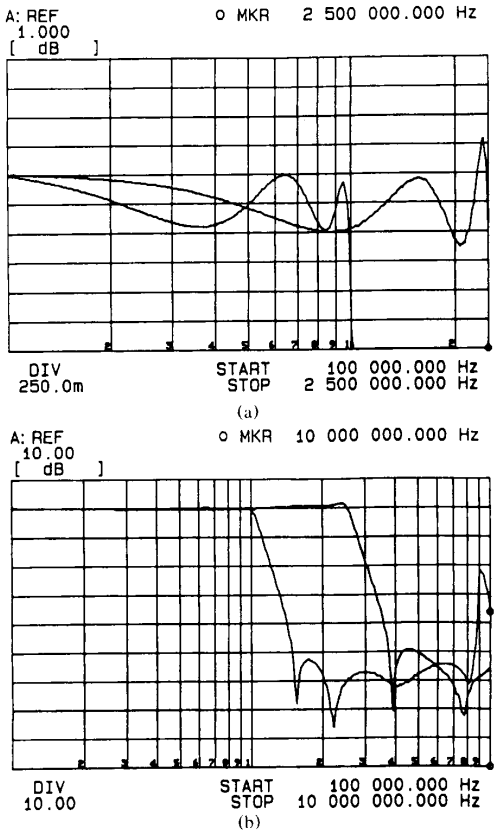

Fig. 11. Experimental SSS SC filter response for a clock frequency of 10 MHz and 25 MHz. (a) Passband frequency response 0.25 dB/div. (b) Overall frequency response 10 dB/div.

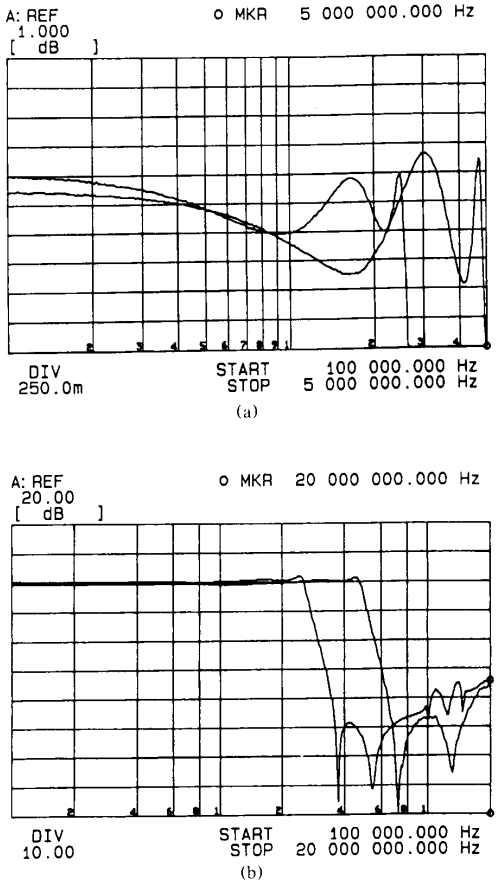

Fig. 12. Experimental DSS SC filter response for a clock frequency of 12.5 MHz and 25 MHz. (a) Passband frequency response 0.25 dB/div. (b) Overall frequency response 10 dB/div.

the deviations of the signal baseband caused by the sample timing error are negligible to the deviations caused by the sinc distortion of the zero-order SH function, no attempt has been made to design an improved signal reconstruction filter [15]–[17].

APPENDIX

The nonuniform sampling operation in bi-phase double-sampling SC circuits is modeled by two uniform distributed Dirac impulse sequences, which are periodic with the clock period T and mutually time shifted by

TABLE IV
EXPERIMENTAL RESULTS OF THE SSS AND DSS SC FILTER

Performance parameter		Single-Sampling		Double-Sampling	
clock frequency	(MHz)	10	25	12.5	25
cutoff frequency	(MHz)	1.0	2.5	2.5	5.0
passband ripple	(dB)	0.5	0.9	0.5	1.0
stopband attenuation	(dB)	53	49	48	46
noise level	($\mu V/\sqrt{Hz}$)	1.3	0.75	0.8	0.5
total inband noise	(mV)	1.3	1.2	1.3	1.2
dynamic range (THD = 1%)	(dB)	47	47	49	49
power supply voltage	(V)	±3.0	±3.0	±3.0	±3.0
power dissipation	(mW)	220	290	240	310

$(1-\alpha)T/2$, with α defined as the relative sample timing error. The construction of the sampled signal $f_S(t)$ from the two separate uniform distributed sample sequences of the continuous-time signal $f(t)$ with spectrum $F(\omega)$ results in

$$f_s(t) = \sum_{n=-\infty}^{n=+\infty} f(nT) + \sum_{n=-\infty}^{n=+\infty} f(nT+(1-\alpha)T/2) \quad \text{(A1)}$$

$$F_s(\omega) = \frac{1}{T}\sum_{n=-\infty}^{n=+\infty} F(\omega - n\omega_T)[1+e^{-jn\omega_T(1-\alpha)T/2}] \quad \text{(A2)}$$

with clock period T and $\omega_T = 2\pi/T$. In practice, the discrete-time signal $f_S(t)$ will have an SH nature. The SH signal $f_{S,\mathrm{SH}}(t)$ can be defined in the time-domain using the impulse sample sequence $f_S(t)$ in (A1) and the unit-step function $u(t)$

$$\begin{aligned} f_{S,\mathrm{SH}}(t) = &\sum_{n=-\infty}^{n=+\infty} f(nT)[u(t-nT) \\ &- u(t-nT-(1-\alpha)T/2)] \\ &+ \sum_{n=-\infty}^{n=+\infty} f(nT+(1-\alpha)T/2) \\ &\cdot [u(t-nT-(1-\alpha)T/2) - u(t-nT-T)]. \end{aligned} \quad \text{(A3)}$$

Using standard Fourier techniques, the spectrum $F_{S,\mathrm{SH}}(\omega)$ of $f_{S,\mathrm{SH}}(t)$ yields

$$F_{S,\mathrm{SH}}(\omega) = \sum_{n=-\infty}^{n=+\infty} F(\omega - n\omega_T)\mathrm{SH}(\omega,n) \text{ with}$$

$$\mathrm{SH}(\omega,n) = \frac{1-e^{-j\omega(1-\alpha)T/2}}{j\omega T} + \frac{1-e^{-j\omega(1+\alpha)T/2}}{j\omega T} e^{-jn\omega_T(1-\alpha)T/2}. \quad \text{(A4)}$$

The modulus of $\mathrm{SH}(\omega,n)$ yields

$$\begin{aligned} |\mathrm{SH}(\omega,n)| = \frac{1}{\omega T}\Big| &(e^{+j\omega(1-\alpha)T/4} + e^{-j\omega(1-\alpha)T/4}) \\ &+ (e^{+j\omega(1+\alpha)T/4} + e^{-j\omega(1+\alpha)T/4}) \\ &\cdot e^{-j(n\omega_T(1-\alpha)T/2+\omega T/2)}\Big| \end{aligned} \quad \text{(A5)}$$

or, using standard goniometry,

$$\begin{aligned} |\mathrm{SH}(\omega,n)| = &|\sin(\omega T/4)\cos(\alpha\omega T/4) \\ &\cdot\cos(n\pi/2+(\omega-n\omega_T)\alpha T/4) \\ &- j\cos(\omega T/4)\sin(\alpha\omega T/4) \\ &\cdot\sin(n\pi/2+(\omega-n\omega_T)\alpha T/4)|/(\omega T/4). \end{aligned} \quad \text{(A6)}$$

For even integer values of n, the second term of the right-hand part of (A6) is significantly smaller than the first term. For even n and $\omega = n\omega_T$ the term $|\sin(n\pi/2 + (\omega - n\omega_T)\alpha T/4)|$ is even zero and $|\cos(n\pi/2+(\omega - n\omega_T)\alpha T/4)|$ is equal to unity. For odd n, similar remarks can be made about the relative magnitudes of all terms in (A6). The first term of the right-hand part of (A6) is significantly smaller than the second term and for odd n and $\omega = n\omega_T$ the periodical terms $|\sin(n\pi/2+(\omega - n\omega_T)\alpha T/4)|$ and $|\cos(n\pi/2+(\omega - n\omega_T)\alpha T/4)|$ are respectively equal to unity and zero.

Based on this discussion, the modulus of $\mathrm{SH}(\omega,n)$ is approximated by

$$\begin{aligned} |\mathrm{SH}(\omega,n)| &= |\sin((\omega-n\omega_T)T/4)\cos(\alpha\omega T/4)| \\ &\qquad /(\omega T/4), \quad \text{for even } n \\ &= |\sin((\omega-n\omega_T)T/4)\sin(\alpha\omega T/4)| \\ &\qquad /(\omega T/4), \quad \text{for odd } n. \end{aligned} \quad \text{(A7)}$$

REFERENCES

[1] R. Gregorian, K. W. Martin, and G. C. Temes, "Switched-capacitor circuit design," *Proc. IEEE*, vol. 71, pp. 941–965, Aug. 1983.

[2] W. M. C. Sansen, H. Qiuting, and K. A. I. Halonen, "Transient analysis of charge transfer in SC filters—Gain error and distortion," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 268–276, Apr. 1987.

[3] M. S. Lee and C. Chang, "Switched-capacitor filters using the LDI and bilinear transformations," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 265–270, Apr. 1981.

[4] T. C. Choi and R. W. Brodersen, "Considerations for high-frequency switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 545–552, June 1980.

[5] M. S. Tawfik, P. Senn, and G. Mazare, "A 1-MHz cutoff frequency CMOS elliptic low-pass switched-capacitor ladder filter," in *Proc. ESSCIRC*, pp. 134–136, 1986.

[6] M. S. Tawfik and P. Senn, "A 3.6-MHz cutoff frequency CMOS elliptic low-pass switched-capacitor ladder filter for video communication," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 378–384, June 1987.

[7] J. J. F. Rijns, "Switched-capacitor filter design for video frequency applications," Ph.D. dissertation, Univ. Twente, The Netherlands, Mar. 1991.

[8] R. B. Datar and A. S. Sedra, "Exact design of strays-insensitive switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-30, pp. 888–897, Dec. 1983.

[9] K. Martin, "Improved circuits for the realization of switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 237–244, Apr. 1980.
[10] M. S. Lee and C. Chang, "Exact synthesis of N-path switched-capacitor filters," in *Proc. IEEE Symp. Circuits Systems*, vol. 1, pp. 166–169, Apr. 1981.
[11] Y. Tsividis, "Representation of sampled-data signals as functions of continuous time," *Proc. IEEE*, vol. 71, pp. 181–183, Jan. 1983.
[12] ___, "Principles of operation and analysis of switched-capacitor circuits," *Proc. IEEE*, vol. 71, pp. 926–940, Aug. 1983.
[13] G. C. Temes and H. J. Orchard, "First-order sensitivity and worst case analysis of doubly terminated reactance two-ports," *IEEE Trans. Circuits Syst.*, vol. CT-20, pp. 567–571, Sept. 1973.
[14] H. Freeman, *Discrete-Time Systems*. New York: Wiley, 1965.
[15] J. L. Yen, "On nonuniform sampling of bandwidth-limited signals," *IRE Trans. Circuit Theory*, pp. 251–257, Dec. 1956.
[16] A. J. Jerri, "The Shannon sampling theorem—Its various extensions and applications: A tutorial review," *Proc. IEEE*, vol. 65, pp. 1565–1596, Nov. 1977.
[17] A. Papoulis, "Generalized sampling expansion," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 652–654, Nov. 1977.

J. J. F. Rijns received the M.Sc. degree and the Ph.D. degree in electrical engineering from the University of Twente, The Netherlands, in 1987 and 1991, respectively.

During his Ph.D. research, he taught a course on switched-capacitor filter techniques. Since 1991, he has been with Philips Research Laboratories, Eindhoven, The Netherlands, involved with the design of analog CMOS circuits.

H. Wallinga (M'81) received the M.Sc. degree in physics from the State University of Utrecht, The Netherlands, and the Ph.D. degree in technical sciences from the University of Twente, The Netherlands.

He joined the University of Twente in 1967, where he was initially involved in device physics and device characterization of MOST devices and CCD's. He is now a professor in semiconductor devices and heads the department on IC Tecnology and Electronics in the Faculty of Electrical Engineering, University of Twente. His research activities include design and testing of sampled data and adaptive signal processing circiuts.