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SILC in MOS Capacitors with Poly-Si and Poly-$Si_{0.7}Ge_{0.3}$ Gate Material

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In this paper the DC-SILC characteristics of n^+ and p^+ poly-Si and poly-SiGe MOS capacitors are studied for substrate($+V_g$) and gate-injection($-V_g$) conditions. P^+ and n^+-gates with poly silicon (poly-Si) and poly Silicon-Germanium (poly $Si_{0.7}Ge_{0.3}$) were used to study the influence of the gate workfunction on gate current and SILC currents. For n^+ poly-SiGe, reduced poly depletion and no significant difference in SILC characteristics compared to n^+ poly-Si gate devices is observed. For p^+ gate devices asymmetric SILC and reduced SILC for poly-SiGe is observed.

1. Introduction

Stress Induced Leakage Current (SILC) limits the scaling of the gate oxide thickness for non-volatile memories. SILC was studied mainly for n-doped poly silicon (poly-Si) gate material up till now [1,2]. Recently, for p^+-gate devices a different conduction mechanism under gate injection conditions ($-V_g$) [3–5], asymmetric SILC (gate bias polarity) and reduced SILC for p^+ poly-$Si_{0.7}Ge_{0.3}$ was observed [5]. However, the impact of poly-$Si_{1-x}Ge_x$ on the SILC characteristics of n^+-gate devices has not been studied yet. In this paper the DC-SILC characteristics of n^+ and p^+ poly-Si and poly-SiGe MOS capacitors are studied for substrate($+V_g$) and gate-injection($-V_g$) conditions and a detailed comparison is made.

2. Experimental Procedures

PMOS and NMOS capacitors were fabricated on 10 Ω-cm n-type and p-type silicon substrates, respectively. A high quality gate oxide with 5.6 nm thickness (ellipsometric) was grown in diluted dry oxygen. Undoped poly-Si and poly-$Si_{0.7}Ge_{0.3}$ layers (200 nm thick) were deposited using a LPCVD system. Gate doping was done by a 20 keV, $2.5 \cdot 10^{15}$ cm^{-2} BF_2^+ or 40 keV, $5.0 \cdot 10^{15}$ cm^{-2} As^+ implant followed by an anneal at 850°C for 30 minutes (p^+-gate) or a rapid thermal anneal (RTA) at 1000°C for 20 seconds in N_2 ambient (n^+-gate). Electrical stress has been applied on $A=4.0 \cdot 10^{-4}$ cm^{-2} (p^+-gate) and $A=3.53 \cdot 10^{-3}$ cm^{-2} (n^+-gate) MOS capacitors using constant current stress conditions of $J_{stress}=\pm 0.1$ mA/cm^2. DC-SILC was measured in a similar way as in [1]. The oxide electric field was determined by integration of the quasi-static capacitance-voltage curves as in [5].

3. Experimental results

Quasi-Static C-V curves for capacitors with p^+-poly Si and poly-SiGe gate are shown in Fig. 1. A shift of the flatband voltage from 0.82V (poly-Si) to 0.60V (poly-SiGe) agrees well with previous data [3,6]. It is caused by a shift in valence band position [6]. Note that the gate depletion is acceptable for both devices. Fig. 2 shows the C-V curves for capacitors with n^+-poly Si and poly-SiGe gate material. Note that since for n^+ gate devices the workfunction difference is negligible between poly-Si and poly-SiGe, the flatband voltage is the same (-0.98V). Also it is evident that the gate depletion of the poly-SiGe devices is significantly reduced compared to the poly-Si reference devices, as was also found in [7].

Fig. 3 shows the J-E_{ox} characteristics of unstressed poly-Si and poly-SiGe capacitors for substrate- ($+V_g$) and gate-injection ($-V_g$) conditions. For n^+-gate devices the J-E_{ox} characteristics are symmetric with $-V_g$ and $+V_g$ injection conditions. However, for p^+-gate devices,

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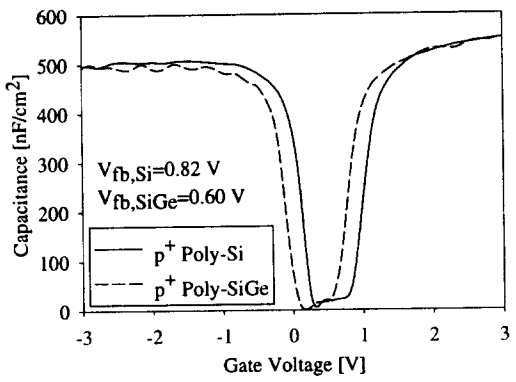

Figure 1. Quasi-static C-V curves for p^+-poly Si and p^+- poly SiGe MOS capacitors. Dashed line poly-SiGe, solid line poly-Si.

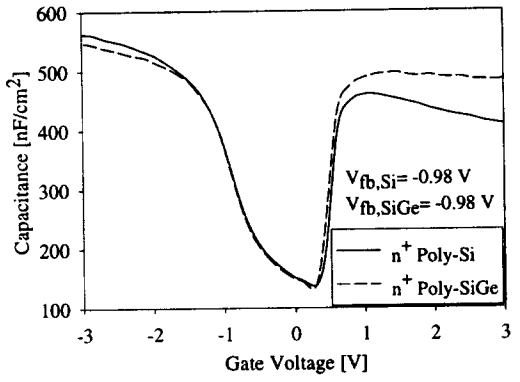

Figure 2. Quasi-static C-V curves for n^+-poly Si and n^+- poly SiGe MOS capacitors. Dashed line poly-SiGe, solid line poly-Si.

the onset of conduction for $-V_g$ occurs at significantly higher oxide field ($\approx 1.5\times$) than for $+V_g$ condition. Note the difference for p^+-gate devices between poly-Si and poly-SiGe at $-V_g$. For $+V_g$ the J-E_{ox} curve can be fitted with the standard Fowler-Nordheim (FN) expression with barrier height of 3.2 eV. For $-V_g$ a fit with a FN expression for p^+-gate devices can not be obtained, unless unphysical fit parameters are used. The gate, substrate and diode currents measured on gate-controlled diodes are shown in Fig. 4.

For $-V_g$ conditions the substrate and diode currents are larger than the gate current (right axis Fig 4, $I_{sub} > 2\times I_{gate}$). The larger substrate current indicates that an avalanche process is taking place. This is not expected when hole tunneling from the substrate dominates the gate current. It appears that gate current at $-V_g$ for p^+ gate devices is caused by electron injection from the gate. There are two possible mechanisms for electron injection from the gate. Firstly, tunneling of minority carriers(MCT) from the conduction band could occur for low active gate doping, since gate depletion increases the electron surface concentration. A second possibility is valence band tunneling (VBT). Gate currents are either influenced by the workfunction for valence band tunneling or the bandgap of the gate material for MCT mechanism. This will influence the SILC characteristics, stress experiments are discussed below.

In Fig. 5 the J-E_{ox} characteristics of n^+ poly-Si and poly-SiGe gate devices are shown for $-V_g$ and $+V_g$ after various stress intervals. From this it can be observed that no significant difference between n^+ poly-Si and poly-SiGe gate devices is observed for $+V_g$ and $-V_g$ injection conditions. Both SILC currents can be described well by a FN expression with an effective barrier of 0.9 eV [1,2].

In Fig. 6 the J-E_{ox} characteristics of p^+ poly-Si and poly-SiGe gate devices are shown after various stress intervals. For $-V_g$ injection the SILC becomes apparent at much higher E_{ox}, furthermore the field dependence is different from that at $+V_g$. At comparable oxide field the SILC is orders of magnitude smaller for $-V_g$ stress than for $+V_g$ stress. Hence there is a strong asymmetry of the SILC currents for p^+ gate devices with stress polarity. This is different from n^+-poly gate devices where SILC is almost symmetric with gate polarity. For $+V_g$ the SILC current after stress follows a FN dependence with effective barrier height of 0.9 eV, which is similar to the n^+-poly devices. For gate injection SILC can not be described by an FN expression with fixed bar-

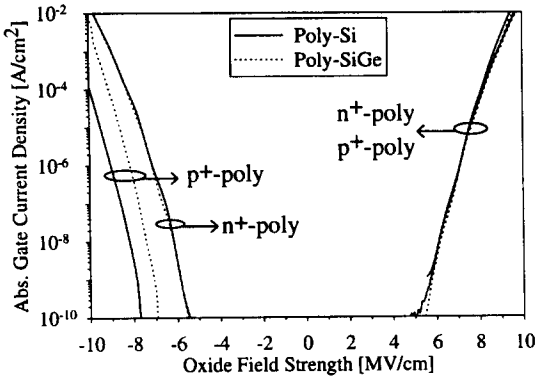

Figure 3. J-E_{ox} measurements of unstressed poly-Si and poly-SiGe gate MOS capacitors. Dashed line poly-SiGe, solid line poly-Si.

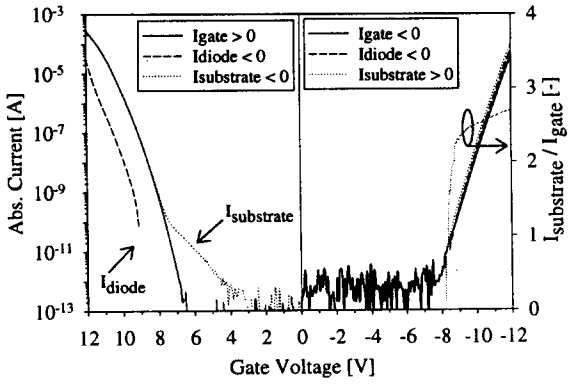

Figure 4. Gate, substrate and diode currents of p^+-poly Si gate-controlled diodes with 7nm oxide thickness as a function of gate voltage.

rier height, variations in shape occur with stress time. An (unphysical) FN fit of the SILC current results in a barrier height around 2 eV indicating a much stronger field dependence. It has been observed that SILC is proportional to the neutral trap density created during stress [1,2] and models based on inelastic trap-assisted-tunneling (TAT) are used to describe SILC [8]. The observed bias asymmetry in SILC for p^+-gate devices could be related to a larger tunneling barrier height for TAT or different position of the traps for $-V_g$ stress conditions. For $+V_g$ conditions the SILC current for p^+ poly-SiGe gates is strongly reduced compared to the p^+ poly-Si reference devices. The reduced SILC of poly-SiGe devices for $+V_g$ stress could be the result of a reduced Boron incorporation in the gate oxide. A larger solid solubility and smaller diffusivety of Boron in poly-SiGe lead to a reduced incorporation of Boron in the dielectric [3]. Hence a lower neutral trap density and reduced SILC for poly-SiGe gates is expected [1,2,9].

4. Conclusions

In summary, the DC-SILC characteristics of n^+ and p^+ poly-Si and poly-SiGe MOS capacitors were studied under substrate($+V_g$) and gate-injection($-V_g$) conditions. For n^+ poly-SiGe no significant difference in SILC characteristics compared to n^+ poly-Si is observed. For p^+ gate devices, both the workfunction of the gate material and Boron penetration into the gate oxide strongly influence the SILC effect. Boron-doped poly-SiGe may be a very interesting gate material due to low SILC at $+V_g$ and better gate oxide quality.

REFERENCES

1. J. De Blauwe *et al.* "A new quantitative model to predict SILC-related disturb characteristics in Flash E^2PROM devices", IEDM Tech.Digest, 1996 pp. 343-346.
2. D. J. DiMaria *et al.*, "Mechanism for stress-induced leakage currents in thin silicon dioxide films", J. Appl. Phys., no. 6(78) 1995 pp. 3883-3894.
3. C. Salm *et al.* "Gate Current and Oxide Reliability in p^+ Poly MOS Capacitors with Poly-Si and Poly-$Ge_{0.3}Si_{0.7}$ Gate Material", Electron Dev. Lett. vol 19(7) 1998 pp. 213-215.
4. J. -L. Ogier *et al.* "On the Polarity Dependence of Oxide Breakdown in MOS-Devices with n^+ and p^+ Polysilicon Gate", Proc. ESSDERC'96, 1996 pp. 763-766.

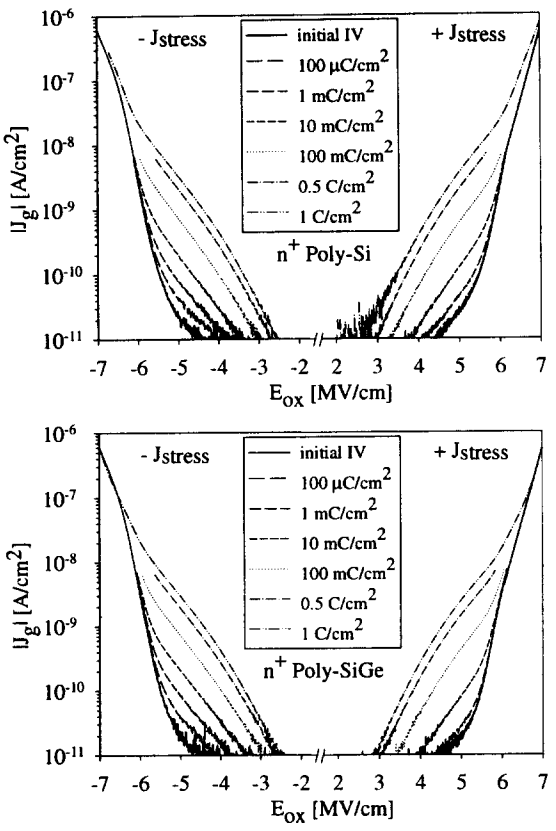

Figure 5. J-E_{ox} curves before and after stress ($100\mu C/cm^2$ to $1C/cm^2$) for n^+ poly-Si and poly-SiGe gate material

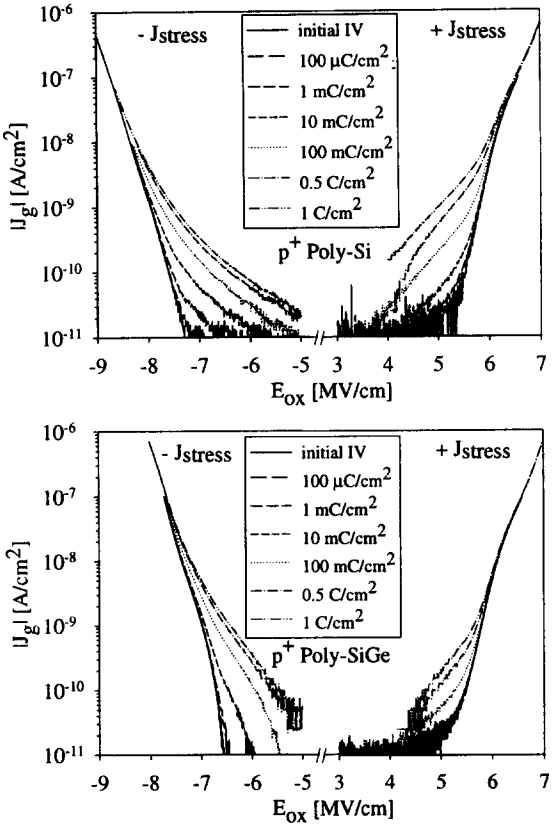

Figure 6. J-E_{ox} curves before and after stress ($100\mu C/cm^2$ to $1C/cm^2$) for p^+ poly-Si and poly-SiGe gate material

5. V.E. Houtsma *et al.* "Stress-Induced Leakage Current in p^+ Poly MOS Capacitors with Poly-Si and Poly-$Si_{0.7}Ge_{0.3}$ Gate Material", accepted for publication in Electron Dev. Lett.
6. T. -J. King *et al.* "A Polycrystalline-$Si_{1-x}Ge_x$-Gate CMOS Technology", IEDM Tech.Digest, 1990 pp. 253-256.
7. W. -C. Lee *et al.* "Observation of Reduced Poly-Gate Depletion Effect for Poly-$Si_{0.8}Ge_{0.2}$-Gated NMOS Devices", Elec. and Solid-State Lett. vol 1(1) 1998 pp. 558-59.
8. A. I. Chou *et al.* "Modeling of stress-induced leakage current in ultrathin oxides with the trap-assisted tunneling mechanism", Appl. Phys. Lett vol 70(25) 1997 pp. 3407-3409.
9. C. Jahan *et al.* "Investigation of Stress-Induced Leakage Current in CMOS Structures with Ultra-Thin Gate Dielectrics", Microelec. Reliab. vol 37(10/11) 1997 pp. 1529-1532.