Modeling a Verification Test System for Mixed-Signal Circuits

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Modeling a commercial verification test system enables simulated tests to be performed before actual testing with instruments and enhances communication between designers and test engineers.

IN CONTRAST TO the large number of logic gates and storage circuits encountered in digital networks, purely analog networks usually have relatively few circuit primitives (operational amplifiers and so on). The complexity lies not in the number of building blocks but in the complexity of each block and the need to test a range of parameters—for example, gain, bandwidth, and signal-to-noise ratio. Degraded circuit performance as well as nonfunctional operation must be checked. Thus, circuit complexity rather than volume complexity is the dominant problem in analog test, and testing mixed-signal circuits entails more difficulties than testing purely digital circuits.

In IC manufacturing, circuits traditionally move from design to test with little thought about how each department's activities affect those of the other. This lack of foresight almost always results in iteration cycles between design and test to realize a testable design that also satisfies the specification. We need a bridge between design and test phases to enable a smooth transition. An integrated approach whereby both teams understand each other's requirements is a big step in the right direction. Interaction between design and test databases significantly increases the degree to which design and test development can operate as concurrent processes; some work has already been done in this area.[1-3]

Our goal was to build Spice models for the instruments incorporated in the IntegraTest system[4] so that we could simulate the tests this system conducts during design. The models are based on manufacturer specifications, and control parameters used in the models are as close as possible to those in the instruments. To make changes in the models transparent to users, entering of parameters is isolated from the models' internal construction. After building the models, we compared the results of the simulated tests with results from actual tests performed with real instruments.

The IntegraTest system

The IntegraTest system is a hardware and software platform for VXI (VME extension for instrumentation) -based measurement subsystems developed by Microlex Systems and Integrated Measurement Systems (IMS). The basic hardware architecture consists of three main blocks: the test controller, the VXI modules, and the high-speed tester.

The test controller is typically a Unix-based workstation, but any computer with support for

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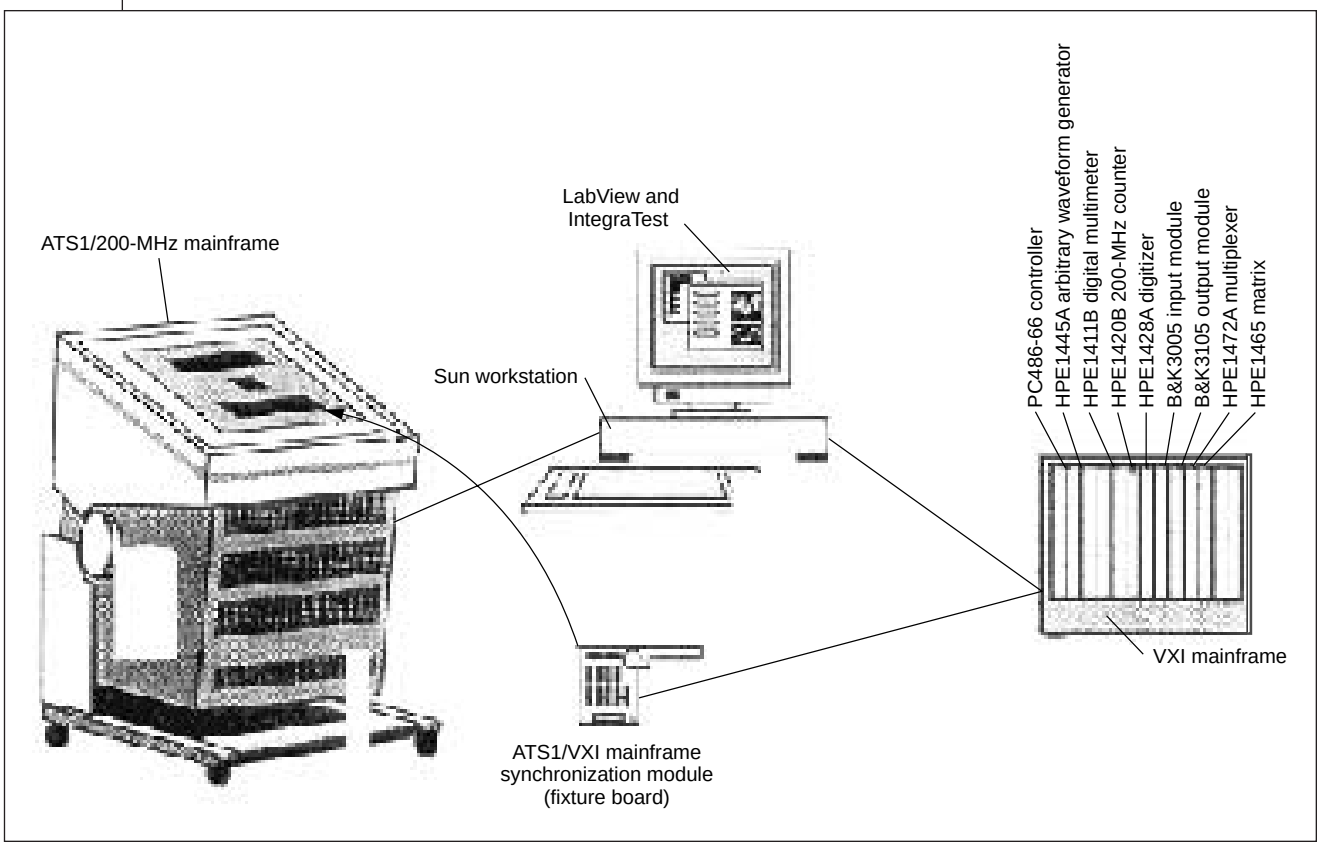

Figure 1. Implementation of the IntegraTest system.

programming GPIB (general-purpose interface bus) and VXI instruments can be used. It includes the software needed to perform the tests—that is, a program to generate and visualize waveforms, the testing programming environment, and the drivers for the instruments.

The VXI modules within the VXI mainframe include all the hardware instruments plus the so-called slot 0 controller. This controller has such special system resources as backplane clocks, configuration signals, and trigger signals, and it also houses the VXI mainframe host. The hardware instruments divide roughly into two categories: routing modules and instrument modules. The routing modules are the HPE1465 switch matrix module and the HPE1472A RF multiplexer. The instrument modules are the B&K3105 output module, the B&K3005 input module, the HPE1445A arbitrary waveform generator, the HPE1428A digitizer, the HPE1420B universal counter, and the HPE1411B digital multimeter. (All instruments referred to as HPExxxx are manufactured by Hewlett-Packard, and all instruments referred to as B&Kxxxx are manufactured by Denmark-based Bruel & Kjær.)

The last part of the system is the ATS1 system.[5] It is a 200-MHz high-speed tester consisting of the ATS mainframe, a controller module, a timing module, slots for up to 14 data modules, a fixture board, and several socket cards. The fixture board covers the top of the ATS mainframe and extends the I/O channels of the inserted modules to external terminals. A socket used to fix the device under test (DUT) and connect it to the modules can be mounted on the fixture board.

Figure 1 shows the actual IntegraTest system implementation, including the interface between the VXI and the test mainframes. A GPIB handles the data exchange between the test controller and the VXI mainframe, and an Ethernet connection handles communication between the test controller and the ATS mainframe. The VXI bus[6] controls and manages communication with the modules.

Modeling the instruments

Our first goal was to build functional models of the instruments in the test system. We decided to develop simple models first, then check their validity and determine whether there were any obstacles to achieving the best results. Also, we wanted to establish an easy way to build the files used in the test simulations so that subsequent changes in the models wouldn't affect the simulation files already written.

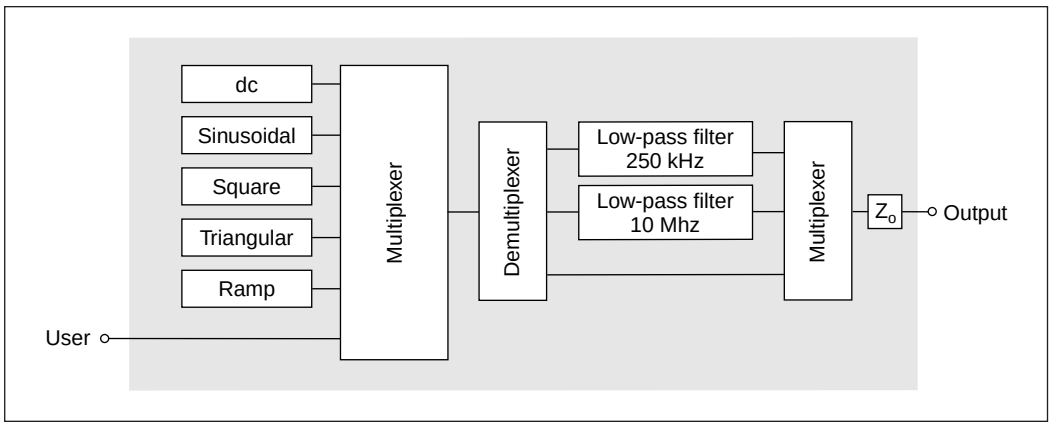

Figure 2. The TRAN model for the HPE1445A waveform generator.

We chose to work with Spice because of its widespread use in the field of analog and mixed-signal design. We used Avant!'s (formerly Meta's) hSpice implementation to make the models and the simulations.[7]

The instruments modeled are the waveform generators and the digitizers, as well as the routing system. The counter and the multimeter use complex DSP (digital signal processing) algorithms to calculate their results, and we chose not to model them because a Spice implementation would be excessively complex.

Waveform generators

Modeling the signal generators in Spice didn't present any special difficulty. The main characteristics chosen for modeling the arbitrary waveform generators were the types of signals they generate (dc, sinusoidal, square, triangular, ramp, and so on), the reconstruction filters, and the output impedance.

The HPE1445A waveform generator includes two low-pass reconstruction filters, one with a bandwidth of 250 kHz and the other with a bandwidth of 10 MHz (the maximum frequency allowed for a signal from the HPE1445A). Fortunately, the data sheet for the instrument[8] describes the type of filter used in each case. Both are Bessel-Thompson filters; the 250-kHz filter is of the fifth order, and the 10-MHz filter is of the seventh order. This makes modeling the filters quite straightforward.

Modeling the B&K3105, however, is not so straightforward. Its manual[9] indicates that the instrument has a low-pass reconstruction filter with a bandwidth of 30 kHz but gives no clue about the order or the approximation used to build the filter. We solved this problem by measuring the filter's frequency response and trying to build an appropriate model that matched the measurements. Both the B&K3105 and the B&K3005 have the same low-pass reconstruction filter. This let us use two different setups to measure the filter response. We can measure the filter in the B&K3105 generator with the HPE1428A digitizer or use the HPE1445A waveform generator to measure the filter in the B&K3005 digitizer. Because the B&K3005 digitizer can measure with higher precision than the HPE1428A, we decided to measure the frequency response of the filter in the B&K3005. From this measurement we found that the filter's cut-off frequency is actually 33 kHz, not 30 kHz.

While developing the first versions of the models, we experienced a problem when trying to find the frequency response of a circuit with either of the two generators. The model has been designed to work in transient-time simulations (TRAN in Spice). Hence, if we want to make a frequency sweep, the appropriate waveform must be externally produced and entered through the user input node provided in our model. This approach proved to be very inefficient because the simulation time increased dramatically. Our solution was to use the frequency sweep simulation (ac) in Spice. To do

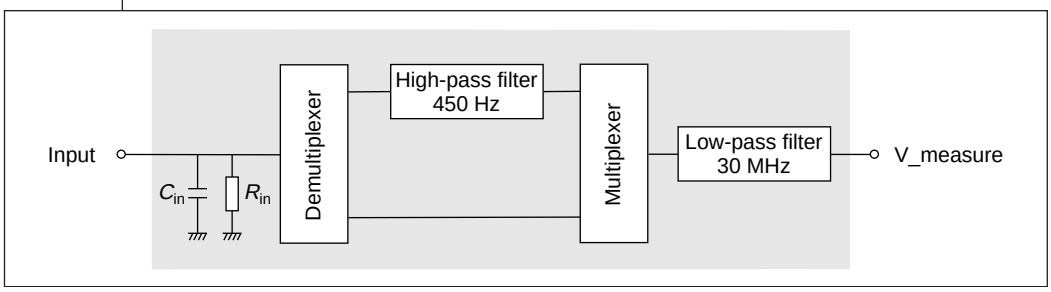

Figure 3. The model for the HPE1428A digitizer.

this, we devised an additional (and simpler) version of the model for the HPE1445A to be used in ac simulations. This new model has only two generators, one for the frequency sweep and a dc generator for offset inclusion. Figure 2 represents the model used for the HPE1445A waveform generator and transient-time analysis.

Digitizers

The characteristics used to model the HPE1428A and the B&K3005 digitizers are the input impedance and capacitance, the high-pass filters used for ac coupling, and the output low-pass filter. The input impedance and the input capacitance appear in the manuals of both modules, so this part presented no difficulty.

Specifications for the HPE1428A module provide no data regarding the order or the approximation used to build the high-pass filter; only the cut-off frequency (450 Hz) is mentioned.[10] Also, it proved impossible to measure the filter's frequency response because of problems with the software driver for the low-frequency-measurement instrument.

The B&K3005 digitizer's high-pass filter has a cut-off frequency of 10 Hz.[11] As with the HPE1428A, the instrument specifications provide no data regarding the approximation used to build the filter. However, unlike the HPE1428A, measuring the filter's frequency response presented no problems. The model that best fit the measurements was a first-order Butterworth high-pass filter.

The HPE1428A includes a low-pass filter with a 30-MHz cut-off frequency at its output. The instrument's specifications give no additional data on the order and approximation used to build the filter. Additionally, neither of the generators in the system let us measure the filter's frequency response, so we used a Bessel-Thompson approximation because of its linear-phase characteristics. The low-pass filter used in the B&K3005 is the same as that used in the B&K3105, as mentioned earlier.

Figure 3 represents the model used for the HPE1428A digitizer. The model for the B&K3005 is similar; the only differences are the high-pass and low-pass filters.

Routing system

The key factor in the IntegraTest system is the routing system. It comprises the HPE1465 matrix module, the HPE1472A RF multiplexer module, and the cables connecting them to the instruments and the DUT.

Instead of trying to model the two routing modules separately, we combined them with the cables in a generic routing model. The IMS system has 16 channels that can be used as either inputs to or outputs from the DUT.[4] To keep a correspondence between the model and the actual system, we made sure that the routing model also consists of 16 channels. It follows the same connection scheme as the actual system: channels 1 to 14 are routed through the matrix, and channels 15 and 16 are routed through the multiplexer. In the model, every channel implements the following signal path. First there's the input cable (from the instruments' or the DUT's outputs to the routing system). Then, depending on the channel number, there's a model of the signal path through the matrix or the multiplexer. Finally, we have the output cable (from the routing system to the instruments' or the DUT's inputs).

The cables used in the IntegraTest system to connect the instruments and the DUT to the routing modules are 1-meter-long coaxial cables of the RG-174/U type. We used the lossy transmission line model included in hSpice to model the cable, employing the parameters for the specific cable model.

The HPE1465 matrix module specifications

give little useful data for modeling the signal path through the module. The module's data sheet indicates that the switches in the matrix are latched armatures; however, no data regarding the physical construction of the armatures is available. So the main characteristics used to model the matrix are the 10-MHz bandwidth and the transmission line's characteristic impedance. The very low series resistance value and the very high insulation resistance value[12] did not affect the simulations. For simplicity, we decided to eliminate them from the model.

The problem encountered when modeling the matrix surfaced again when we tried to model the multiplexer: insufficient data from the manufacturer. The switches in the multiplexer are nonlatched armatures, but there is no data about their electrical characteristics or how they are constructed. The multiplexer also has a series and an insulation resistance, and a bandwidth of 1.3 GHz. Its bandwidth is much higher than the maximum bandwidth of any instrument in the IntegraTest system (250 MHz for the HPE1428A digitizer), so we decided not to model it. The only characteristics modeled for the multiplexer were the series and the insulation resistance.

```
    TEST THE DUT: measuring the STEP RESPONSE
    *GENERATOR:hpe1445aawg
    *DIGITIZER:hpe1428adig
    *DUT:comb_two_stage
    *routing: includes cables

    * Subcircuits
    .INCLUDE '../lib/filters.spi'
    .INCLUDE '../lib/cables.spi'
    .INCLUDE '../lib/comparator.spi'
    .INCLUDE '../lib/mxers.spi'
    * The instruments
    .INCLUDE '../lib/hpe1428adig.spi'
    .INCLUDE '../lib/hpe1445aawg.spi'
    .INCLUDE '../lib/routingwc.spi'
    * The DUT
    .INCLUDE '../DUT/simple_excitation.spi'

    * The routing system
    Xrout 0 0 0 0 0 0 0 0 0 0 0 0 0 0 test_out_opamp v_gen
    + oma1 oma2 oma3 oma4 oma5 oma6 oma7 oma8 oma9 oma10 oma11 oma12 oma13
       oma14
    + v_dut_out test_in_opamp
    + routing
    * The 1445 AWG
    X1445 0 v_gen hpe1445awg signal=3 amplit=1 offset=2.5 freq=2.5k infinity_load=1
    * The 1428 digitizer
    X1411 v_dut_out v_meas hpe1428dig

    * Calculations and post-processing
    .OPTION POST=1
    .TRAN 2n 300u
    .PROBE TRAN V(v_gen) V(v_meas)
.END
```

Figure 4. Example Spice simulation file using several instrument models.

Verifying the models

The next step was to determine whether the models could accurately simulate the results obtained from a real test made with the actual instruments. First we show how the simulation files were constructed, then we compare the simulation results with the test results.

One goal of the project was to allow easy generation using software of the simulation files that use the instrument models. Hence, the designer need not construct the test simulation files. This makes the models suitable for inclusion in systems such as the Cadence Design Framework or Mismatch.[13]

Figure 4 shows an example of a typical Spice simulation file, including the routing system, the HPE1445A waveform generator, and the HPE1428A digitizer. The file is divided into three parts (following the comments). The first part includes the necessary circuit files, such as the models for the instruments used and the Spice description of the circuit to be simulated. The modules and their parameters appear in the second part. Finally, in the third part, we can see the calculation and postprocessing options. In this way, creation of the file for simulating the measurement system can be easily automated from an existing description of the test circuit and the test to be carried out.

For the first tests we measured the frequency and step responses of direct connections between the generator and digitizer pairs (HPE1445A–HPE1428A and B&K3105–B&K3005). These direct connections were made first without the routing system, then through the matrix, and finally through the multiplexer. In the second round of tests we measured the frequency and step response of a simple RC (resistance-capaci-

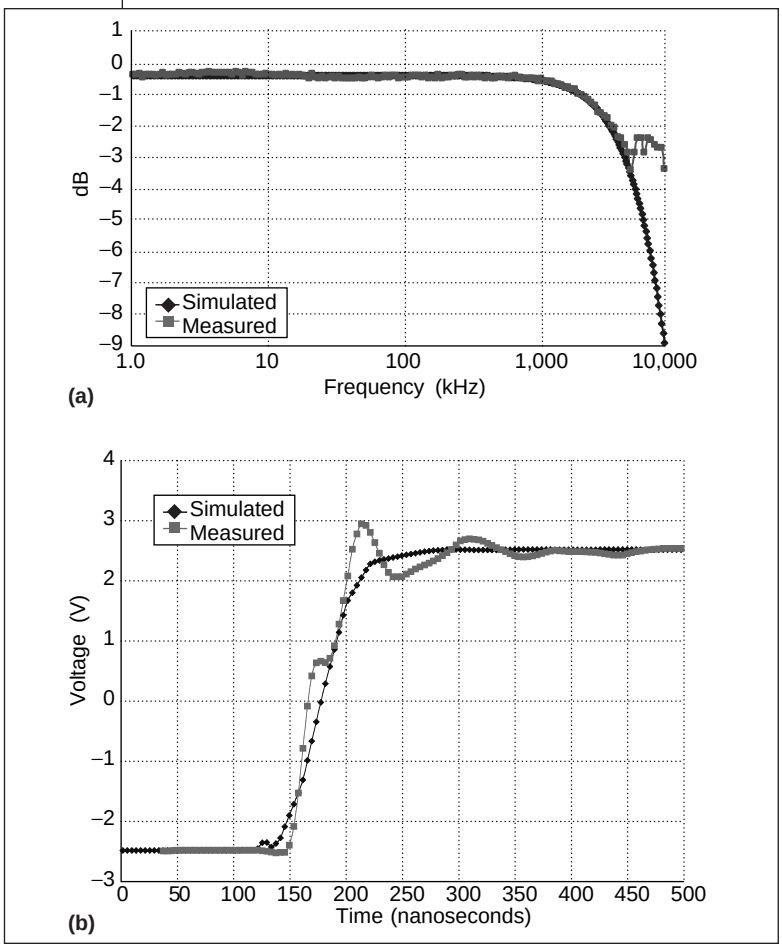

Figure 5. Frequency (a) and step (b) response of the connection through the matrix between the HPE1445A and the HPE1428A.

tance) low-pass filter. Finally, we measured the frequency and pulse responses of two circuits, including two different commercially available operational amplifiers, the LM324 and the OP27. All the programs (virtual instruments) necessary to perform the tests with the IntegraTest system were created in the LabView environment.

Measurements made without the routing system closely resembled those achieved with the simulated tests. The only difference found in the frequency response was some noise. In the case of the HPE1445A–HPE1428A pair, we also found a difference of about 1 decibel (dB) at the highest frequencies. Figure 5 shows the simulation and test results using the matrix as the routing module. At the highest frequencies, a lot of noise is present. The simulated test for the step response (Figure 5b) doesn't include the voltage overshoot found in the test results. Its absence results from the matrix model's simplicity. Only one reactive element is present in the model, making it impossible to oscillate. The real matrix, however, presents some parasitic inductances and capacitances.

Figure 6 shows the results of simulating and measuring the connection through the matrix of the B&K3105 and the B&K3005. The routing system doesn't affect the measurements with the low-frequency modules, and the results are the same whether the matrix and the multiplexer are used or not. The simulation results

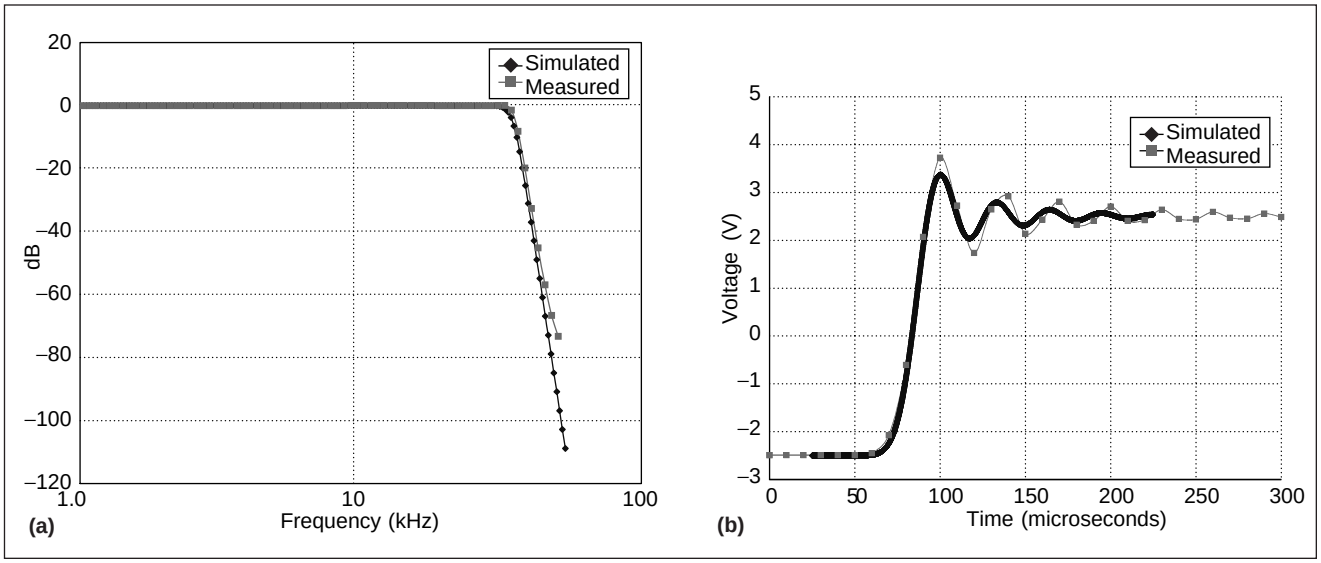

Figure 6. Frequency (a) and step (b) response of the connection through the matrix between the B&K3105 and B&K3005.

follow the real test results with great accuracy. The only difference appears at the highest frequencies, but the signal levels are very low (less than –60 dB). Step response (Figure 6b) revealed only a small difference in the oscillation frequency. In this case, as opposed to Figure 5, the test simulation presents some overshoot, owing to the nature of the low-pass filter.

Figure 7 shows the results of tests made putting a simple RC filter between the instruments and routing the signals through the matrix.

When using the multiplexer to route the signals, we expected the analysis results to be very similar to those involving no routing. However, this was not the case. The results of different tests performed with the same configuration at different times, or after changing a connection, show a random pattern, appearing in Figure 8. We found no plausible reason for this strange behavior.

The last batch of tests involved two different commercially available operational amplifiers in two different configurations, and here we faced a practical problem. Although the HPE1445A waveform generator allows amplitudes as low as 0.163 V,[8] the software driver for the instrument reported errors if we tried to output a signal with less than 0.5 V of amplitude (1 V peak to peak). This kept us from doing a small-signal analysis.

The simulation results agree with the small-signal characteristics as presented in the data sheets for the amplifiers.[14,15] The test results, however, don't. This is because the input to the amplifier was actually a large signal, owing to the problems with the software driver for the waveform generator. Looking at the large-signal frequency response in the amplifiers' data sheets, we could see that the measurement results were as predicted by the manufacturer. The difference in results is a consequence of the Spice model for the amplifiers. These models are not the actual amplifier implementations but functional descriptions of them. This simplification assumes a small signal, so the effects of large signals are not taken into account. Fixing the software problem so that small signals could be used for the measurements or having better models for the devices that allow large signals to be used as input to the circuit model would solve this problem.

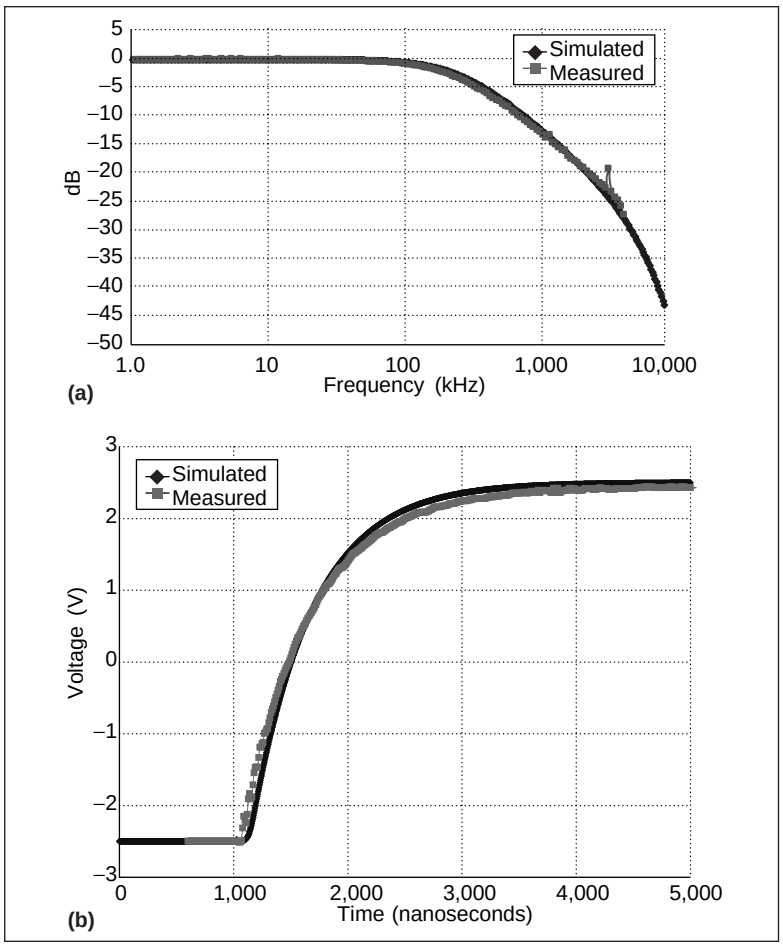

Figure 7. Frequency (a) and step (b) response of the RC filter routing the signals through the matrix, measured using the HPE1445A and the HPE1428A.

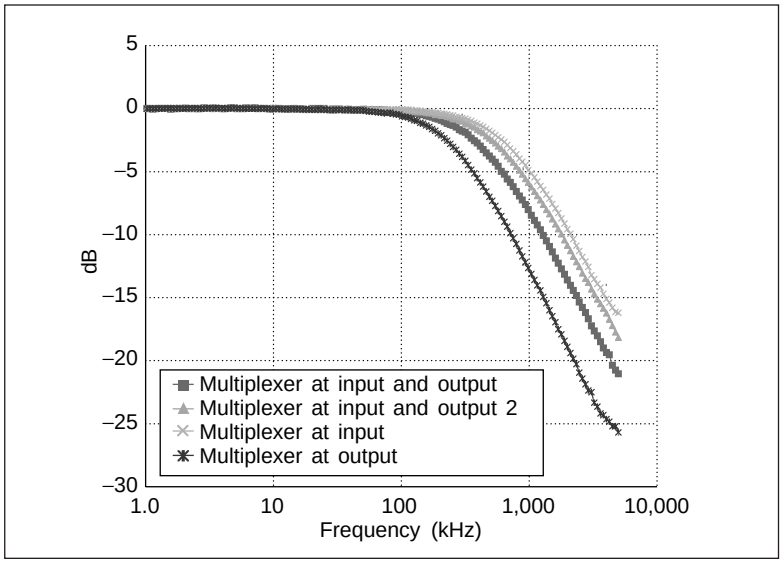

Figure 8. Frequency response of the RC filter for different multiplexer configurations.

While the models for the instruments were very simple, the results obtained from the simulations nearly equaled the test results in almost all the tests made. The only differences appeared when testing the operational amplifiers and when testing the RC filter using the multiplexer for the routing. In the first case, the simulations failed because the software driver for the HPE1445A generator didn't work according to the instrument specifications. In the second case, the difference between the simulation and the measurement is due to the multiplexer model's simplicity. No data was available regarding the characteristics of the switches in the matrix and the multiplexer. However, the results of the simulations with the matrix model were very accurate, with only second-order effects not being simulated.

We have shown that it is possible to build Spice models of test instruments and use those models to simulate the tests. The results of these simulations can mimic those of the real tests. Also, the files used for the simulations are built in a highly structured fashion. This allows test simulations to be easily automated from either the test or the simulation environment.

Future improvements depend on data availability to model the switches in both the matrix and the multiplexer routing modules. Also, second-level models of the other instruments can be made, including the analog-to-digital and digital-to-analog blocks that can be found in all the instruments (which include analog-to-digital converters or digital-to-analog converters and amplifiers and attenuators). Inclusion of these models in higher level systems (such as Mismatch or Cadence's Design Framework) is also an important future possibility. Building the simulation files is easy, and they are transparent to the user.

As noted earlier, during the experiments we discovered quite a difference between the data sheet provided for the VXI module and its actual behavior. Much of the information in the data sheet is based on the VXI module's hardware capabilities. In some cases, however, because of limitations in the driver software, performance falls below what the data sheet specifies, so the data sheet could not serve as a performance reference. VXI instrument manufacturers should at least make sure the data sheet specifications pertain to the actual working environment and thus ensure that the modules' performance is not limited by the driver software. ■

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