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Design of analog-to-digital converters for energy-sensitive hybrid pixel detectors

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Abstract

An important feature of hybrid semiconductor pixel detectors is the fact that detector and readout electronics are manufactured separately, allowing the use of industrial state-of-the-art CMOS processes to manufacture the readout electronics. As the feature size of these processes decreases, faster and more complex electronics can be designed and manufactured. Furthermore, most new CMOS processes are optimised for use with digital circuits, making the design of precise analog electronics a difficult task. Hence, the sooner the data is converted to the digital domain, the better the technology can be used. We have studied the possibility of adding energy sensitivity to the single photon counting capability of pixel detectors. To know not only the number of X-ray photons but also their energies (or wavelenghts), will increase the information content of the resulting image, given the same X-ray dose. In order to do this, a small and low power ADC is added to each pixel. We have studied different types of analog-to-digital converters that can be implemented inside the pixel electronics of a pixel detector.

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Keywords: Pixel detectors; VLSI; Energy sensitivity; Analog-to-digital converters

1. Introduction

Semiconductor pixel detectors are now used in almost all major high energy physics experiments (see, for example, [1,2]). Their application as photon counting devices for X-ray and gamma-ray detection has also been demonstrated [3,4]. In this case, the advantages of pixel detectors over other types of imaging devices are their high sensitivity, low noise, linear behaviour and wide dynamic range.

In the so-called hybrid pixel detectors, the detector and the readout electronics are manufactured independently. They are connected afterwards using flip-chip bonding techniques. This allows for separate optimisation of the detector and the readout electronics. In order to take advantage of the fast developments taking place in the semiconductor industry, the readout electronics are usually manufactured using industrial CMOS processes.

New CMOS processes offer smaller feature sizes and lower supply voltages. Those two characteristics allow, in principle, smaller or more complex

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pixel electronics with little increase in power consumption. However, new CMOS processes are primarily optimised for manufacturing digital ICs. This means that analog circuits (which are the crucial part of the pixel electronics) become more cumbersome to design [5].

To design energy-sensitive pixel electronics, the analog data coming from the detector should be converted into digital form as soon as possible, in time (as soon as the event occurs) as well as in space (as close to the connection to the detector as possible). This conversion can be performed using analog-to-digital converters (ADC) in the pixel electronics. The use of ADCs at the pixel level can also improve the spatial resolution in particle detection applications [6].

In the following we will show several approaches to obtain energy-sensitive pixel electronics using analog-to-digital converters in every pixel. In Section 2 we mention a first approach to energy sensitivity already used in some photon counting pixel detectors not requiring the use of analog-to-digital converters. In Section 3 we explain four different ADC architectures we are exploring, showing our simulation results. We will end with conclusions from the work so far and future work to be done.

2. Multi-comparator

The output signal from a charge sensitive amplifier in the pixel readout electronics is directly proportional to the energy of the incident photon. In single photon counting detectors, this signal is compared against a threshold, and if the signal exceeds the threshold, a counter is incremented. It is easy to see that by using $N+1$ comparators and N counters, N different regions in the energy spectrum can be selected. If the regions are equally spaced, this approach is similar to a flash ADC [7]. By using only two comparators and one counter [8] or two counters [4], and allowing the thresholds to be programmed independently, a simple form of *energy windowing* can be achieved.

One possible application is to implement the differential imaging system of Ref. [9] to acquire images containing energy information in just one acquisition, eliminating the need for energy filtering and multiple exposures. This system requires a minimum of four comparators and three counters, which is perfectly feasible with current CMOS technologies. The biggest advantage of such a system is its reliance upon already proven front-end and readout electronics. The different thresholds can be programmed via on-chip DACs, allowing for its use in multiple applications.

3. Pixel-level ADC

One problem is that the more energy channels we want, the more comparators and counters are needed, increasing the pixel area and power consumption. If we want to have a large number of regularly spaced energy channels, the use of generic ADCs must be considered.

We have chosen to put the ADCs inside the pixel electronics and not in the periphery for various reasons. One important reason is the need to minimise the area occupied by peripheral electronics. Most applications need an imaging area that exceeds the typical $2\,cm^2$ of a single chip. This means that several chips must be butted together and the peripheral circuits, which cause a dead area between chips, must be kept to a minimum.

Another important reason is that, by having an ADC in every pixel, all the ADCs work in parallel and so the need for high-speed operation moves to the readout digital chain, and we can take advantage of the fact mentioned earlier that CMOS processes are optimised for fast digital functionality.

In most pixel readout chips there is a clear distinction between the image acquisition and the data readout. In our case, however, the digital readout has to be working while an image is being acquired, as we do not intend to provide means for storing more than one hit in the pixel. This means that an event by event readout is needed for this kind of circuit.

A flash analog-to-digital converter has the highest speed, but its cost in area and power consumption can be too high for resolutions of 3 bits or higher. Given that in a typical pixel detector we want to keep the pixel size as small as

possible and the power consumption low, this leads us to consider other ADC types that can achieve the desired resolution while minimising the occupied area as well as the consumed power. The downfall of this approach is the decrease in the conversion speed compared with the flash ADC solution. For most applications, however, this decrease can be tolerable.

The energy resolution we can achieve with a hybrid pixel detector is ultimately limited by the noise of the electronics and by the energy resolution of the detector. We chose to make our designs with a resolution of 4 bits. This corresponds approximately to the best resolution that can be achieved with a room temperature GaAs detector [10], and we assume to a first approximation that the electronics noise will not deteriorate this resolution. We aim at a pixel size of the order of 100 μm by 100 μm, and a power consumption below 50 μW per pixel (including ADC, amplifier and readout).

The basic pixel electronics that we will consider for our designs is shown in Fig. 1. The first block amplifies and integrates the signal from the detector and gives two signals to the ADC. One of them is the analog input to the ADC, and is proportional to the charge deposited in the detector. This signal can be expressed as a current or as a voltage, depending on the type of converter. The second signal is a digital pulse that tells the ADC that a photon has hit the pixel and the conversion can start.

The readout unit is located after the converter. This circuit stores the digital value and interacts with the periphery of the chip to send the digital data out of the pixel.

The reasons for studying different designs are the trade-offs that each one offers, in terms of area, power and conversion speed.

3.1. Slope ADC

The operating principle of the slope ADC is shown in Fig. 2. The signal is stored as a voltage on a capacitor C. At a given moment, this capacitor starts being discharged by the current source, and at the same time the counter starts to count. When the voltage stored in the capacitor goes below the threshold of the comparator, the counter is stopped. The counter then contains a digital representation of the input signal. This conversion technique is sometimes referred to as Time-Over-Threshold.

Its main advantage is the simplicity of the components needed: one comparator, one N-bit counter (with N being the number of bits of the converter) and one current source.

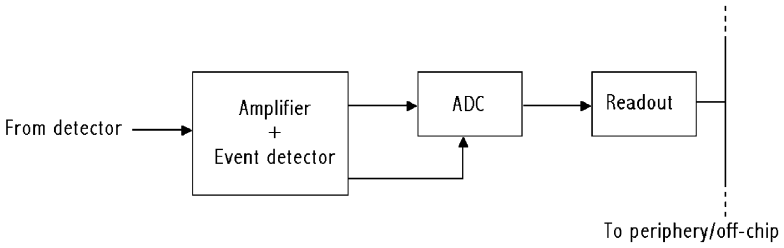

Fig. 1. Block diagram of the pixel electronics.

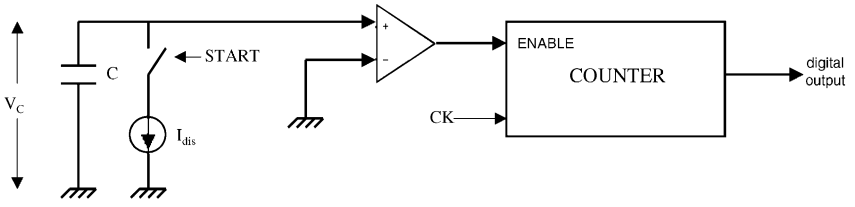

Fig. 2. Block diagram of the slope ADC.

3.2. Successive approximation ADC

The slope ADC is equivalent to a linear search: we need of the order of 2^N clock periods to obtain the final value with an accuracy of N bits. A much better approach is to use a binary search, where only N clock periods are needed to realise the conversion. This can be implemented via a so-called successive approximation ADC. Fig. 3 shows the block diagram of such an analog-to-digital converter.

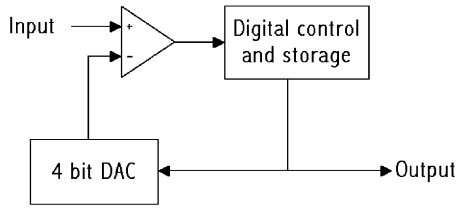

Fig. 3. Block diagram of the successive approximation ADC.

Fig. 4 shows the waveforms of the inputs to the comparator (the DAC output and the signal to be converted) as well as of the clock, in a simulation of our system.

First, the digital block sets to logic level 1 the MSB of the DAC at the rising edge of clock. If the comparator output does not switch state before the next clock cycle, it means that the value of the DAC is lower than the input, and hence the bit is kept as 1. If the comparator output switches, the value of the DAC is higher than the input, and so the bit is switched back to 0. This is repeated for all N bits.

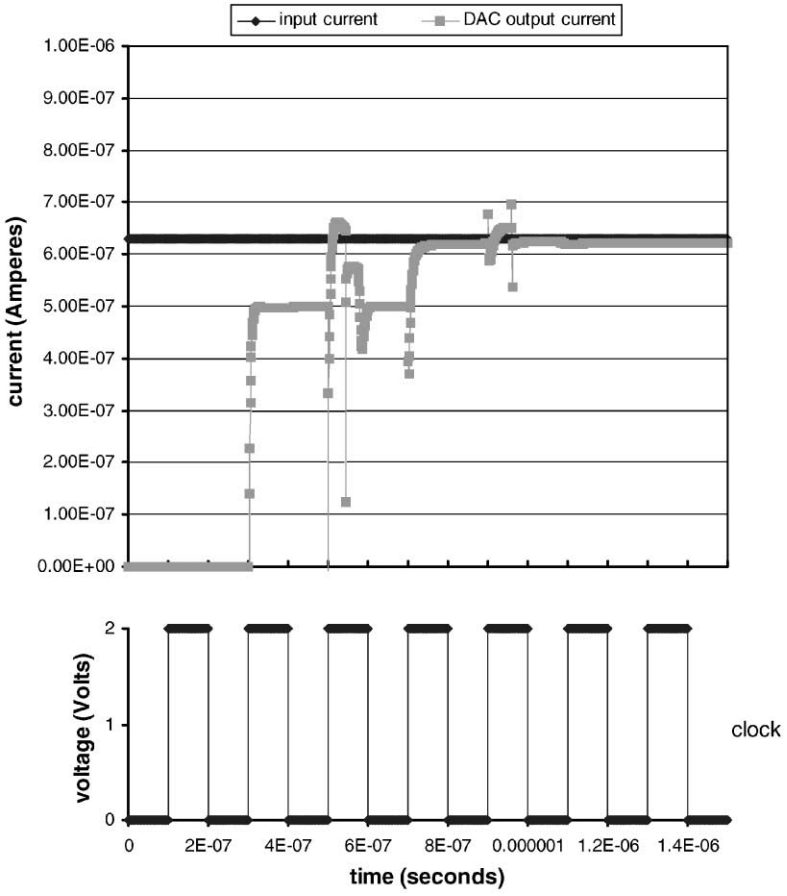

Fig. 4. Waveforms of the input signal and the output of the DAC in a successive approximation ADC.

Fig. 5 shows the input–output characteristic of the converter, simulated at a 1 μA full scale and with a clock frequency of 5 MHz (1.25 Msamples/s).

In this design, the input signal is expressed in the form of an electrical current. This eases the design of the comparator [11] as well as of the DAC.

It is possible to increase the speed while keeping the same input–output characteristic by increasing the full-scale current. This is due to the fact that the speed of a comparator depends on the difference between the two signals at its inputs. This increase in full-scale current, obviously, will lead to an increase of the power consumption.

3.3. Algorithmic ADC

The term algorithmic refers to the basic building block [12], shown in Fig. 6. The basic principle of this block can be summarised as follows. The input value is expressed as an electrical current, as this eases the design of the different components. The input signal is multiplied by 2 and compared with a reference value equal to the full-scale current of the converter. If the reference is higher, the analog output is set equal to the input multiplied by two, and the digital output is set low. If the reference is lower, the analog output is set equal to the input multiplied by two minus the reference, and the digital output is set high.

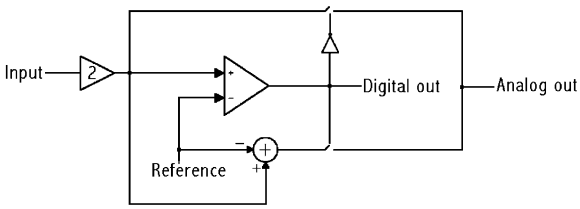

Fig. 6. Block diagram of the basic block in the algorithmic ADC.

A first ADC that uses this basic block [12] can be seen in Fig. 7. Our design is a slightly modified version, in order to decrease the static power consumption. One could call this a "pipelined" algorithmic ADC. The advantage of this design is

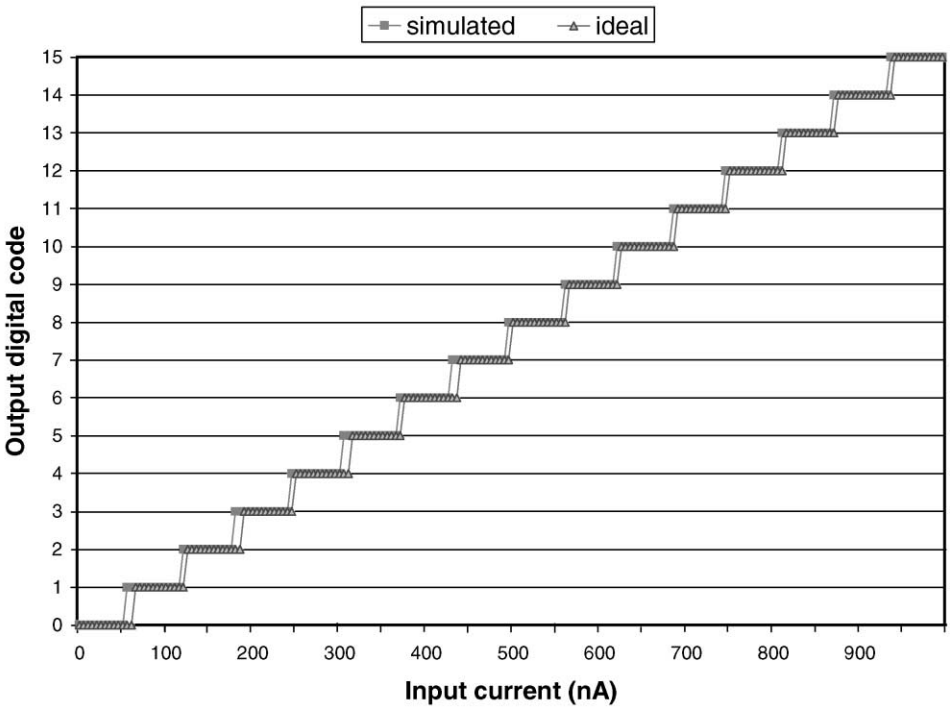

Fig. 5. Simulated input/output characteristic of the successive approximation ADC.

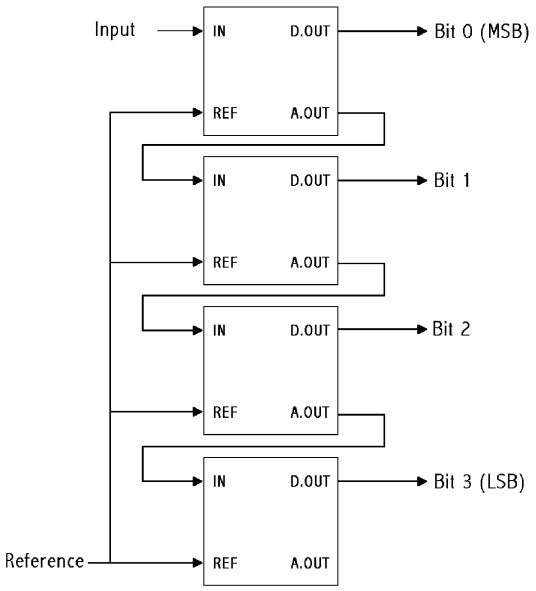

Fig. 7. Block diagram of the pipelined algorithmic ADC.

its simplicity: no digital circuitry is needed, and also no clock signal has to be distributed to the cells. It is also faster than the successive approximation ADC. The disadvantage is that it uses N basic blocks, which means N times the area and the power of one basic block. Fig. 8 shows the input–output characteristic of such an ADC with 1 μA full-scale current.

Another possibility is to use the same building block in a sequential way as Fig. 9 shows. It again needs N clock cycles to perform the conversion, so its speed is the same as that of the successive approximation ADC. The complexity of the digital circuitry is also similar to the successive approximation case, as one needs to generate the control signals in the pixel. The complexity in the analog part is in the design of the sample and hold block. If we use current to express the input value, its design can be simplified by using a circuit as the one described in Ref. [13].

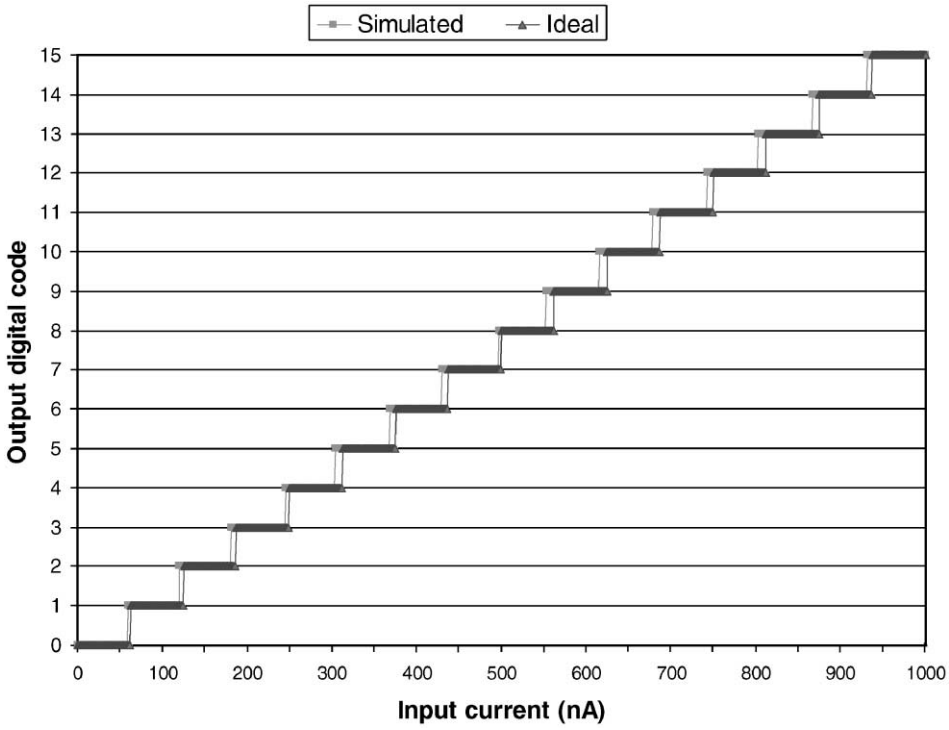

Fig. 8. Simulated input/output characteristic of the pipelined algorithmic ADC.

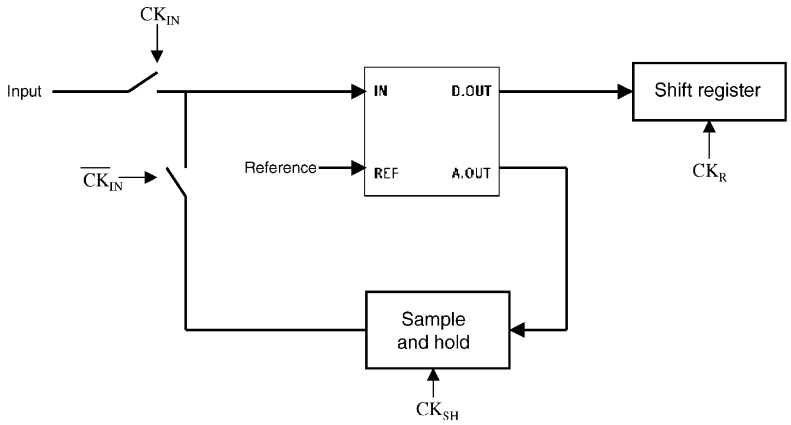

Fig. 9. Block diagram of the sequential algorithmic ADC.

4. Testing the ADC

It is a general trend in the microelectronics industry to put more functionality in new chips as soon as new technologies with smaller feature sizes become available. This, however, creates the problem of how to test this increased functionality close to the operating conditions. This is further complicated by the increase in operating speed of the circuits. Expensive test-equipment is needed to verify these circuits. As a way to reduce the complexity of testing, new methods are developed that add some of the test equipment/circuitry inside the chip. One of such techniques is the so-called Built-In-Self-Test (BIST).

As we have seen, the complexity of a pixel readout chip with energy sensitivity electronics is high, compared to previous chips. Thus, we decided to study the possibility of including some kind of BIST functionality. We must keep in mind that the area occupied by the additional circuitry must remain minimal.

We have designed a circuit that checks for missing codes and evaluates the differential and the integral linearity in all the ADCs located in an array of N by M [14]. In terms of extra circuitry, it only needs one DAC, three counters and very simple digital logic. The DAC could even be one of the DACs used to bias the analog front-end, minimising the need for extra circuitry. It only needs four extra I/O pads, which can also be shared with some of the pads used in the normal operation of the chip.

5. Conclusions

In order to add energy sensing capabilities to pixel detectors, analog-to-digital converters can be added to the pixel electronics. We are studying the possibility of using analog-to-digital conversion techniques different from flash conversion. Compared with a flash ADC, our circuits suffer from a reduction in conversion speed, but at the same time, the power consumption and the area occupied by the electronics are decreased.

An important implication of the use of pixel-level ADCs is the need for an architecture capable of reading-out data event by event.

We plan to submit a test chip with arrays of the ADC structures we are studying in order to measure their performance. We are also investigating ways to speed up and simplify the readout of the data from the pixels, as well as new ways to implement the amplifier–integrator stage before the ADC.

Acknowledgements

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References

[1] ATLAS collaboration, ATLAS Pixel Detector: Technical Design Report, CERN-LHCC-98-013, 31 May 1998.
[2] ALICE collaboration, ALICE: Technical Design Report of the Inner Tracking System (ITS), CERN-LHCC-99-012, 18 June 1999.
[3] M. Campbell, E.H.M. Heijne, G. Meddeler, E. Pernigotti, W. Snoeys, IEEE Trans. Nucl. Sci. NS-45 (3) (1998) 751.
[4] M. Lindner, Nucl. Instr. and Meth. A 466 (2001) 63, these proceedings.
[5] A.-J. Annema, IEEE Trans. Circuits Systems-II: Analog Digital Signal Process. 46 (6) (1999) 711.
[6] D.C. Christian, J.A. Appel, G. Cancelo, S. Kwan, J. Höff, A. Mekkaoui, J. Srage, R. Yarema, S. Zimmermann, Nucl. Instr. and Meth. A 435 (1999) 144.
[7] S. Cadeddu, C. Caligiore, M. Caria, A. Lai, D. Lo Presti, S. Panebianco, C. Petta, P. Porcu, N. Randazzo, P. Randaccio, S. Reito, G.V. Russo, Nucl. Instr. and Meth. A 419 (1998) 270.
[8] http://medipix.web.cern.ch/MEDIPIX/.
[9] C.A. Mistretta, Kelcz, US patent No. 3974386, August 1976.
[10] E. Bertolucci, M. Conti, G. Mettivier, P. Russo, A. Cola, F. Quaranta, L. Vasanelli, M.G. Bisogni, U. Bottigli, M.E. Fantacci, A. Stefanini, Nucl. Instr. and Meth. A 422 (1999) 247.
[11] H. Träff, Electron. Lett. 28 (3) (1992) 310.
[12] D.G. Nairn, A.T. Salana, IEEE J. Solid-State Circuits 25 (4) (1990) 997.
[13] G. Wegmann, E.A. Vittoz, IEEE J. Solid State Circuits 25 (3) (1990) 699.
[14] D. San Segundo Bello, E. Wolthuis, A BIST system for an array of static analog-to-digital converters, University of Twente, February 2000, available for download from http://www.nikhef.nl/user/dbello/stuff/reportbist.pdf.