Fast Thermal Cycling-Enhanced Electromigration in Power Metallization

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Invited Paper

***Abstract*—Multilevel interconnects used in power ICs are susceptible to short circuit failure due to a combination of fast thermal cycling and electromigration stresses. In this paper, we present a study of electromigration-induced extrusion short-circuit failure in a standard two level metallization currently used in power ICs and in particular the effect of fast thermal cycling on the subsequent electromigration lifetime. A special test chip was designed, in which the electromigration test structure is integrated with a heating element and a diode as temperature sensor in order to generate fast temperature swings and to monitor them. Experimental results showed that with the introduction of fast thermal cycling as a preconditioning, the electromigration lifetime is significantly reduced. We observed that the reduction of the electromigration lifetime depends on the stress time, temperature range and the minimum temperature. Electromigration simulations using a two-dimensional simulator confirm the extrusion short circuit as failure mechanism.**

***Index Terms*—Electromigration, extrusion, fast thermal cycling, interlayer dielectric, short circuits.**

I. Introduction

ELECTROMIGRATION (EM) is a phenomenon that occurs when an electrical current leads to mass transport of metal atoms within the integrated circuit (IC) metallization [1]. EM-induced failure of interconnects can be either voids growing over the entire line width that cause breaking or resistance increase of the line or extrusions that cause short circuits to neighboring lines. Many extensive studies have reported about the EM-induced open circuits as well as the resistance increase failure mode in submicron line metallization. However, the EM-induced extrusion short circuit, which has been already reported in an earlier study [2], can become a reliability concern in modern integrated circuits, where multilevel metallization schemes with faster, smaller and higher performance are required. This means that the multilevel interconnect dimensions, linewidth, linespacing, and junction depth are shrunk to accommodate a higher density of metal lines and low-k dielectric materials are introduced to increase the speed. As published data shows, low-k dielectrics have a lower fracture resistance compared to conventional dielectrics [3]. Metallization schemes using low-k materials as an interlayer dielectric (ILD) can cause a reliability problem because of an increased chance of cracking of the low-k dielectric due to a compressive stress induced by the EM driving force [4]. In these cases, use of design rules based solely on the open circuit failure mode could result in a less reliable product. It has been recognized that the extrusion short circuit failures induced by EM results in the cracking of the ILD (or passivation) not only depend on the metallization properties but also on the ILD properties. For instance, if a lower elastic modulus ILD is used, it could flex and relieve some of the EM-induced compressive stress in the metal line resulting in a delay of the extrusion. Thermal and mechanical stresses are generated in both the ILD and the metal layers due to the thermal mismatch among metallic, dielectrics and silicon substrate. It is clear that thermal and mechanical stresses can degrade the metal line (induce voids) as well as the ILD (induce micro-crack) and can be considered a particularly important aspect to the EM-induced extrusion failure mechanism.

In power IC metallization schemes, there is a coupling between thermal and electromigration stresses due to large ac signals. Therefore, a combined stress of EM and thermal cycling may induce early extrusion failures in the metallization, which would be a major reliability concern in power ICs. There are quite some studies about the effect of thermal cycling on the electromigration performance [5], [6]. In these studies, the thermal cycling is done slowly using an environmental chamber. The typical temperature cycle time for this method is quarters of an hour or more. This possibly masks the mechanism of more realistic fast thermal cycling (FTC) on the EM performance. As far as we know the effects of the FTC on the EM performance is still unknown, and a full understanding the effect of the FTC stress on the EM performance is necessary to adjust the EM design rules for a better reliability of multilevel interconnects used in power ICs.

In this paper, we characterize the EM-induced extrusion short circuit failure mode of a standard two level metallization currently used in power ICs. A no-cracking condition together

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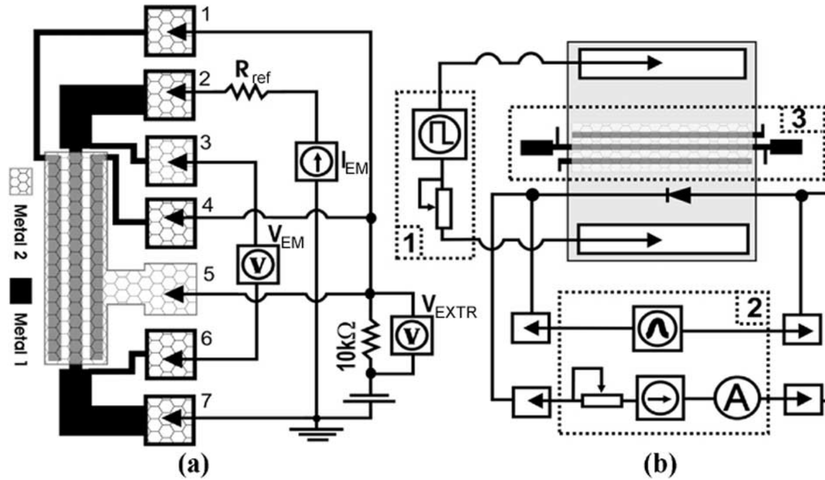

Fig. 1. Experimental setup. (a) Top view diagram of the electromigration test structure together with the electromigration test circuit; pads (2), (3), (6), and (7) are $I^{+}_{\rm EM}$, $V^{+}_{\rm EM}$, $V^{-}_{\rm EM}$, and $I^{-}_{\rm EM}$, respectively, and (1), (4), and (5) are extrusion monitors. (b) Setup for fast thermal cycling preconditioning, (1) is a pulsed current source, (2) is the temperature measurement module (consists of a digital oscilloscope and a dc current source), and (3) is the EM device under test.

TABLE I
TEST STRUCTURE LAYER DETAILS

Layers	Materials	Thickness [µm]
Passivation	Si_3N_4	1
Metal 2	Al-Si(1%)-Cu(0.5%)	2.5
Interlayer Dielectric	Si_3N_4	0.9
Metal 1	Al-Si(1%)-Cu(0.5%)	1
Oxide	SiO_2	1

with simulations of the EM-induced compressive stress and the thermal expansion is used to demonstrate the failure mechanism. In particular, the influence of FTC, induced by the on chip micro-chuck, on the EM performance is investigated. Different FTC conditions are employed to carry out a preconditioning step to distinguish between the effects of the FTC temperature range (ΔT) and the FTC minimum temperature $(T_{\min})$ on the EM lifetime.

II. EXPERIMENTAL DETAILS

A. Description of the Test Chip

The test chip was manufactured in a two-level metallization process used for the fabrication of power ICs. Both metal 1 and metal 2 are AlCu(1%)Si(0.5%). No barrier layers were used. The thicknesses of metal 1 and 2 are 1.0 and 2.5 μm, respectively. The passivation and the interlayer dielectric are both silicon nitride with a thickness of 1.0 and 0.9 μm, respectively. Table I summarizes the material information.

The 1000-μm-long test line (metal 1) has Kelvin contacts to accurately measure the resistance. Next to the meandering stressed test line there are additional tracks at both sides to monitor lateral extrusion in metal 1 and a large metal 2 plate, covering the entire structure, to monitor interlayer metal extrusions during the EM testing. The metal 2 plate is only used as an extrusion monitor and there are no vias between metal 1 and metal 2. The line length of 1000 μm exceeds the Blech length significantly and is even longer that the standard NIST EM structures. On both sides the EM test line ends in wide NIST-like feeds which act like reservoirs.

The line width of the test line and the extrusion monitors, as well as the spaces between the stressed line and the extrusion monitor tracks, is 3.5 μm.

To carry out the FTC as preconditioning for the EM tests, besides the standard EM test element, the test chip was designed with two more important on-chip elements. First, a large n^{+}-Si resistor just below the die surface that can be used as a micro-chuck. Second, an integrated diode in the middle of the chip used as a temperature sensor. The resistor is used to generate fast temperature swings by forcing a pulsed current through it and the diode is used to monitor the temperature swings.

The test chips were encapsulated in standard 17 pins power packages (DPS-17-P). Two different packages referred to as type A and B were used in this study. The essential differences between type A and B are the moulding compound and the die-attachment materials. In the package type A, a polymer die attachment has been used to glue the silicon die to the lead frame. In the package type B, a lower stress moulding compound and solder die attachment has been used.

B. Experimental Setup

To perform the EM tests, a commercial setup (DESTIN EM system with specified temperature stability of 0.02 °C and current stability of 250 ppm) has been used. The basic EM test circuit schematic used in this work can be seen in Fig. 1(a) (it is mounted with the EM test structure). A constant current is passed through the metal line and the voltage across the metal line is monitored. The three extrusion monitors are connected via 10-kΩ resistors. During EM testing, the resistance of the stressed line and the extrusion voltage across on the 10-kΩ resistor are continuously monitored. By connecting the 10-kΩ resistor and the extrusion monitors in series, the current through the stressed line remains the same even after the first extrusion is formed. To carry out a pre-stress with the FTC, the experimental technique for the FTC test, which was described in detail in a previous paper [7], was employed. The setup that is used to

TABLE II
ELECTROMIGRATION TEST CONDITIONS

Name	**J**[MA/cm^2]	**T**[^{o}C]
E1	2.5	125
E2	2.5	150
E3	1.5	125
E4	1.5	150
E5	2.5	175

generate and measure the temperature swings during the FTC stressing is shown in Fig. 1(b).

C. Sample Size

For each stress condition a sample size of 16 devices was used. Each set of 16 devices contained dies from all test wafers to compensate for possible wafer-to-wafer or batch-to-batch variations. The sets for both package types were made from different wafers so here the wafer-to-wafer difference is only accounted for when comparing test conditions per package.

III. RESULTS AND DISCUSSIONS

A. Electromigration-Induced Extrusion Failure Mode

Conventional EM tests were carried out to examine the EM performance of metal 1. Fresh devices encapsulated with the package type A were tested with condition E1, E2, E3, E4, and E5 as shown in Table II. The samples were stressed more than 1500 hrs. Fig. 2(a) and (b) shows typical plots of the resistance of the stressed line measured as a function of time for EM tests with conditions E2 and E4, respectively. The resistances drop due to an extrusion was observed for condition E2 but not for condition E4. No gradual increase in the resistance was observed for any of the stress conditions in Table II, so this is not a failure criterion for these samples. This is due to the low acceleration of the EM test conditions. Also, alloying of the aluminum with solutes of Cu and Si can play a role. Except for the low stress conditions E3 and E4, we observe that devices fail due to extrusions. As we will explain later a few devices show an open circuit at the end of the stress time.

Typically, the extrusions happen before the open circuit as shown in Fig. 3(a). After the extrusion the stress continued. Sometimes a second extrusion can occur and sometimes an open circuit can be created due to voiding. The open circuit did not always occur because sometimes the current in the stressed line is reduced too much due to the extrusions. In Fig. 3(b), a zoom-in shows more visible simultaneous variations of resistance in a stressed line and voltage in an extrusion monitor. It can be seen that when the first extrusion was formed the resistance of the stressed line did not change. This means that the stressed line can still carry the current, and the test is continued until another extrusion or open circuit is formed. When the second extrusion forms, which can be observed from the measurement of extrusion voltage [see Fig. 3(b)], the resistance of the stressed line drops because a portion of the stressed line is shorted out by the two extrusions. It can be also seen in Fig. 3(b) that before the second extrusion there is a slight increase of the resistance of the stressed line as well as the extrusion voltage due to the larger extrusions. With a long stress time, the resistance of the stressed line could drop steeply [see Fig. 3(b)]. As demonstrated in Fig. 1, the extrusion monitor pads were connected together during the EM testing for the extrusion monitor. To distinguish between a sideways extrusion (the extrusion of stressed line to sideways tracks) and interlayer extrusion (the extrusion of the stressed line to metal 2), separated sequential extrusion monitors of the sideways and the interlayer extrusions were carried out on the failed devices. Only in very few cases the sideways extrusions were observed, implying that the interlayer extrusion (the extrusion between metal 1 and metal 2) is the main failure mechanism in these samples. This is due to the difference in dimensions, the tracks are separated by 3.5 μm and the thickness of the ILD is 0.9 μm.

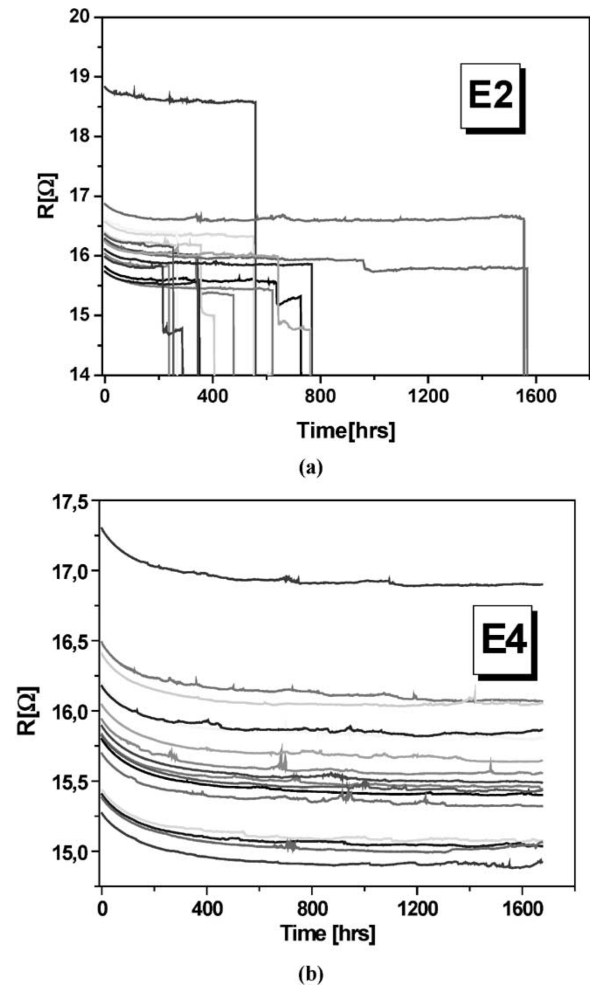

Fig. 2. Resistance evolution of metal lines stressed with condition. (a) E2, extrusion failures are observed. (b) E4, no failure is observed.

In order to confirm these observations, the devices with extrusion short circuit and void-open circuit failure identified by the electrical measurement were selected for failure analysis. The structure used in this work has a very thick metal 2 layer covering over the stressed line and the extrusions are normally very small. Therefore, locating the extrusion is a very difficult task. Several techniques to locate the extrusion such as liquid crystal hot spot detection and optical beam induced resistance change (OBIRCH) have been tried but without success so far, the later technique seems to be promising but more studies are needed. To overcome this problem, a focused ion beam (FIB) was used

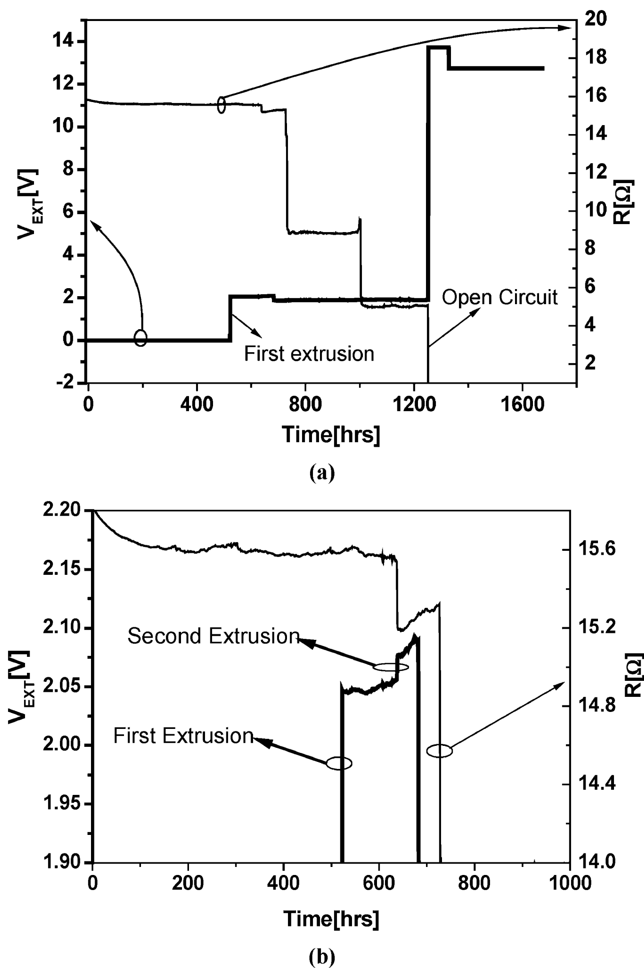

Fig. 3. Monitor results of metal line resistance and extrusion voltage. (a) Typical extrusion and resistance measurement of a sample for the whole electromigration period. (b) Zoom-in of the first extrusion to show in detail the extrusion and resistance measurement.

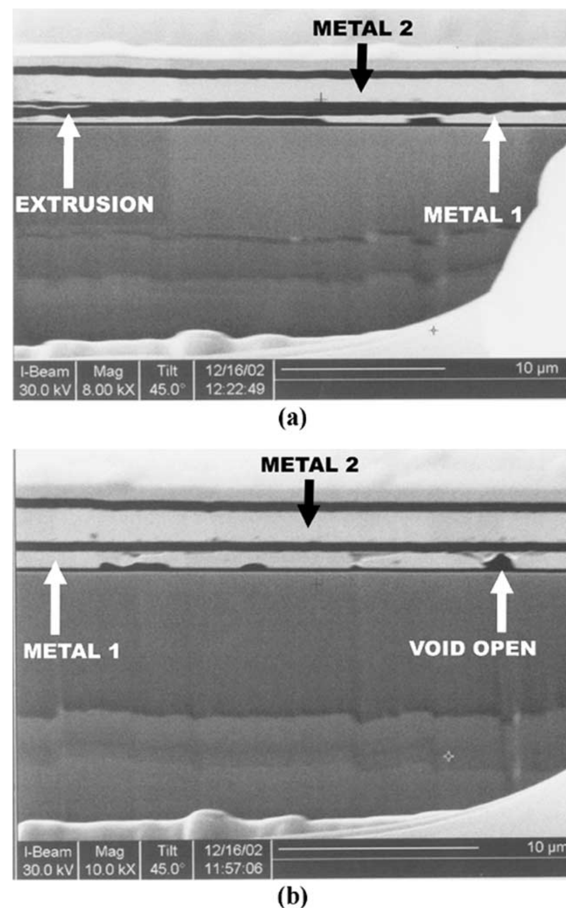

Fig. 4. FIB cross-section showing (a) the extrusion-short and (b) void-open circuit.

to make cross-sections in search of extrusions and opens on the stressed line. To do so, very long cross-sections were made parallel with the stressed line, which is a time consuming and costly task. After making several cross-sections, we finally observed a typical extrusion and void as respectively shown in Fig. 4(a) and (b). Please note that the extrusion as shown in Fig. 4(a) did not show clearly the extrusion short circuit between metal 1 and metal 2, which is very difficult to obtain by making cross-sections because the extrusions are very small. Despite the fact that Fig. 4(a) shows the metal only extruded through the ILD halfway to metal 2, it does clearly show how the extrusion has been formed.

To analyze the EM lifetime in this work, the extrusions short-circuit as mentioned above is used as the failure criterion to estimate the time to failure. This means that a device was considered to have failed when a significant extrusion voltage (larger than 0.1 V) had appeared on the extrusion monitor. Note that the time to failure is determined by the time to form the first extrusion. In fact, a competition takes place between many locations (micro-cracks or defects in the ILD) where metal can extrude and cause the short circuit fail. This resembles a weakest link mode. Therefore, the times to failure distributions of the EM tests with conditions, E1, E2, and E5 (see Table II) were plotted in a Weibull graph, shown in Fig. 5. It can be seen that the distributions are relatively well behaved with comparable slopes. This would imply that the same failure mechanism has occurred for the three test conditions. Fig. 6 shows the resulting mean time to failure (MTF) as a function of reciprocal temperature. The temperature rise due to the Joule heating of about 10 °C was added to the stage temperature to more accurately represent the stressed line temperature during testing. The activation energy for this failure mode is extracted to be 0.67 eV. This value is in good accordance with the value of 0.7 eV obtained from the original EM process qualification. Here different test structures were used with a relative resistance increase as failure criteria. An activation energy of ~0.7 eV is typical for electromigration-induced failures and is consistent with Al-alloy grain boundary diffusion. The similarity in activation energy for resistance increase and extrusion-short failure modes implies that the fundamental mechanism does not change in EM-induced extrusion short circuit. The EM-induced extrusion failures as well as the EM-induced resistance increase are driven by the transport of mass induced by the stressing current. However, the actual failure is caused by the accumulation and depletion of mass at certain places that is affected by the microstructure of the metal line. The movement of Al atoms in the direction of the electron current causes mechanical stresses to build up in the metal line due to atomic flux divergence at grain boundaries, at the anode and the at cathode. Tensile and compressive stresses are

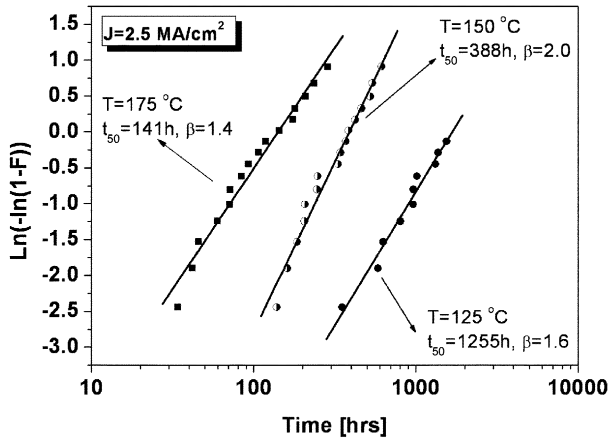

Fig. 5. Failure probability plots for electromigration with $J = 2.5$ MA/cm^2 and $T = 175\,^\circ$C, 150 °C and 125 °C.

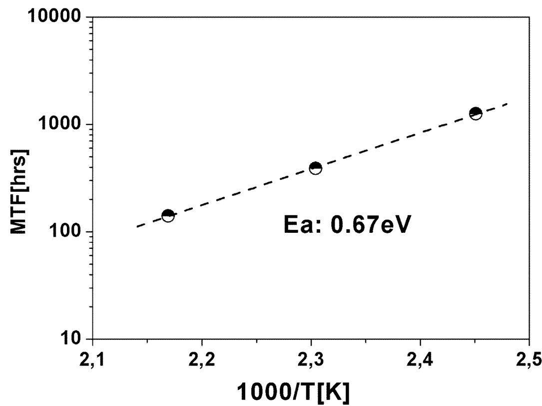

Fig. 6. Arrhenius plot of short circuit failure for three temperatures at $J = 2.5$ MA/cm^2.

generated in regions of mass depletion and of mass accumulation respectively. When the compressive forces generated in the lines cannot be relieved, they will build up to a point where the dielectric cracks and metal extrudes through the opening. It can be argued that the EM-induced extrusion failure can be assisted by local increase in temperature and the presence of initial voids. Because local heating can cause a micro-crack in the ILD due to the different thermal expansion of the layers where the metal easily pumps through the ILD by the EM stress, and an initial void can cause the current density to increase in the vicinity around itself because of the reduction of cross-section area of the conductor.

Recently, Suo [8] has proposed a no-cracking condition for small objects, using fracture mechanics as an energy criterion that can be used for the EM case as follows:

$$\beta P_{\max}\sqrt{W} < K_c \quad (1)$$

where $P_{\max}$ is maximum hydrostatic pressure in the metal line, β is a dimensionless geometric parameter, W is a characteristic dimension of the interconnect cross-section, chosen to be the linewidth. K_c is the fracture resistance of the layer overlaying the metal line.

Suo has predicted that if the stress build-up at the anode about 1.5 GPa, the no-cracking condition will no longer be satisfied, resulting in the cracking of the SiO_2 passivation. Chiras

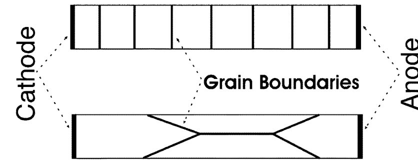

Fig. 7. Simulation structures with different microstructures: bamboo (top) and near bamboo (bottom).

and Clarke have presented an extensive study of applying the Suo model for the metal line with Si_3N_4 passivation [9]. They have reported that the stress induced by electromigration is only about 1 GPa. The thermal stress due to the thermal expansion mismatch between aluminum and Si_3N_4 at the EM test temperature must be included into the no-cracking condition. The difference in prediction of maximum compressive stress (Suo: 1.5 GPa and Chiras: 1 GPa) to induce the cracking of the passivation is caused by the fact that they have used different passivation materials (SiO_2 and Si_3N_4), and the fracture toughness of SiO_2 which is almost twice as that of Si_3N_4 [10]. Suo and Chiras have measured the stress at the anode and taken that as the maximum stress in the line to verify the no-cracking condition.

However, we have carried out failure analysis on many failed devices and did not find any extrusions or cracking of the ILD at the area near anode, but extrusions were found in the stressed line quite far away from anode. The explanation is the presence of reservoir areas at the ends of the line so that metal diffusion is not stopped at the line end. This implies that the extrusions that were observed are not due to the accumulation of materials at the anode but at a position in the line far away form the anode. Depending on the microstructure of the metal line, the compressive stress can build up at different levels to be large enough to crack the ILD layer.

To verify this issue, we have used a two-dimensional (2-D) EM simulator to study the mechanical stress evolution in time of the stressed line with stressed condition E2 ($J = 2.5$ MA/cm^2 and $T = 150\,^\circ$C) for different microstructures in the metal line. Details about this simulator can be found elsewhere [11]. We have compared two simulation structures with different microstructures, which are bamboo and near-bamboo (triple point) grain boundaries in the metal line as shown in Fig. 7. The activation energies for aluminum diffusion in bulk ${E_a}^{\mathrm{bulk}} = 1.4$ eV and at grain boundaries ${E_a}^{gb} = 0.6$ eV were, respectively, higher and lower than experimentally obtained activation energy $({E_a}^{\exp} = 0.7\,\mathrm{eV})$. Apparently the activation energy found from the experiment depends on a combination of grain boundary as well as bulk diffusion and possibly even surface diffusion. The aim of these simulations is not a quantitative comparison, but they are used to explain the failure mechanism. Results of mechanical stress distributions of the metal lines stressed with condition, E2 for 500 hrs are shown in Fig. 8(a) and (b) for the bamboo and near-bamboo microstructures of Fig. 7, respectively. As expected, the maximum stress in the near-bamboo line is significantly larger. It can be seen that the stress builds up very fast at the triple point. Hence, these triple points are the weakest point, i.e., the point where the cracking of the ILD and the subsequent extruding of metal can cause a short circuit between

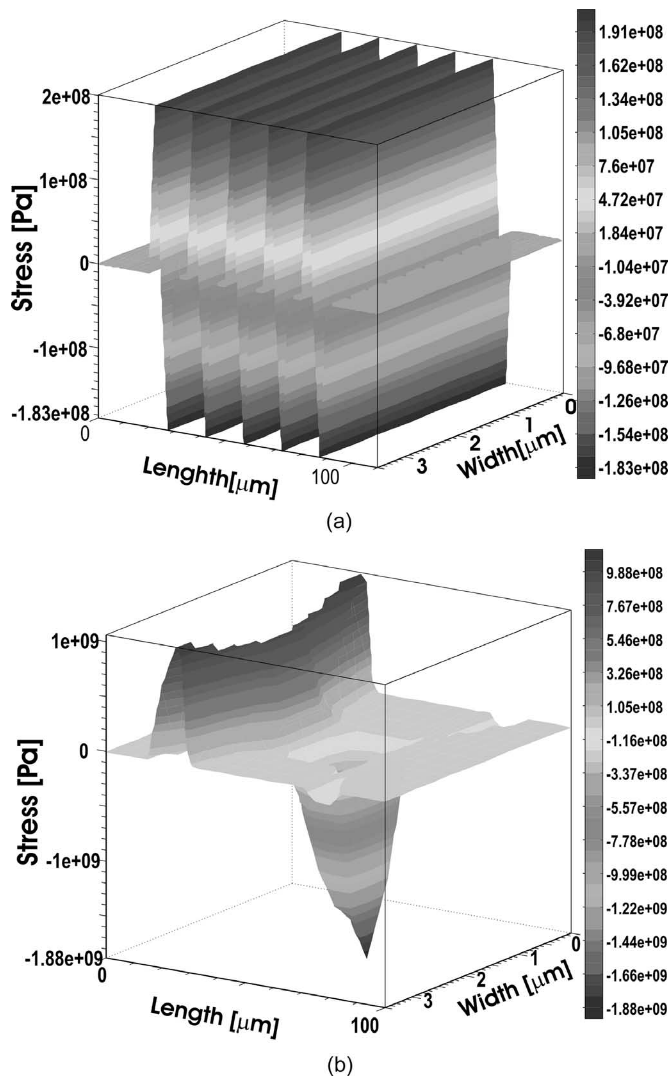

Fig. 8. Simulation of stress build-up in metal lines after 500 hrs of EM stress ($J = 2.5$ MA/cm^2 and $T = 150$ °C). (a) For the bamboo grain boundary. (b) For the near bamboo grain boundary (see Fig. 7).

metal 1 and metal 2. The maximum of compressive stress at the triple point is 1 GPa.

As mentioned above, the thermal stress at the EM test temperature needs to be added to the no-cracking condition. This is a compressive stress in the metal line because Al has a larger thermal expansion coefficient than both the dielectric and the substrate. As seen in published data [12], [13], the thermal stress depends on the aspect ratio of the line, the geometry of the interconnect structure, the mechanical properties of the dielectric and the temperature. Its magnitude can be more than 100 MPa. To estimate the thermal stress of our sample at the temperature of EM test, a semiconductor process simulator (SILVACO) has been used to simulate the processing of the test structure and thermal stress at different temperatures [14]. First the simulation test structure was built up following the experimental process steps, and the result of simulation is shown in Fig. 9(a). Its geometry is quite comparable with a cross-section of the test structure that will be shown in the next section (Fig. 13). Then, the thermal stress build-up due to the thermal mismatch among the layers was simulated for an increase in temperature from room temperature (23 °C) to the EM test temperature (150 °C). It should be mentioned that the thermal stress of the package (due to the thermal mismatch between package substrate and silicon die) was not included in this simulation. Fig. 9(b) shows the thermal stress build up in the ILD (Si_3N_4) and metal 1 (M1) at the position near the left edge of the metal line. The maximum compressive stress in the metal line is about 225 MPa, and this stress can be larger when the thermal stress of package is included. Therefore, the thermal stress cannot be neglected in the no-cracking condition. To verify the no-cracking condition for our case, the representative values $\beta = 0.3$, $K_c = 0.5$ MPa $\cdot\, \mu$m$^{1/2}$, and $W = 3.5\ \mu$m were taken [9]. Substituting these values into (1) yields that there will be no cracking of the passivation layer if $P_{\max}$ is lower than 0.9 GPa. This value is much lower than the total stress of 1.2 GPa, induced by the 500-hrs EM stress (1 GPa) and the thermal stress at the EM test temperature (0.2 GPa), so cracking of the Si_3N_4 layer will take place.

If the metal line were assumed to fail due to the increase of the resistance only, it might pass the reliability qualifications. It is clear the cracking of the ILD followed by extruding metal during EM stress should be included in the reliability analysis. The extrusion failure mode can be affected by different factors, such as the initial void density in the metal line, thermal stress, packaging-process-induced stresses, plastic deformation characteristics of the Al (determined by the microstructure and the impurity concentration in the Al film), properties of the ILD material (fracture resistance), etc. Thermal stresses are inherently present in power ICs, so for these processes analysis of extrusion failures should be included. In the next section, we will discuss the impact of fast temperature swings on the EM lifetime tested by fast temperature cycling induced by the on-chip micro-chuck.

B. *Influence of Fast Thermal Cycling*

In power ICs, the FTC and the EM stresses always occur simultaneously. The dominant failure can be due to either FTC or EM or a combination of the two mechanisms, depending on the operating conditions. In this work, we study the interaction of the two stresses by applying sequentially FTC and EM stresses. The failure mechanism induced by FTC stress, without an EM stress current, has been found to be a short circuit due to the cracking of the ILD [7] and the dominant failure induced by EM tests in this study is also a short circuit but due to an extrusion. Therefore, one expects that the FTC stress affects the EM lifetime.

The devices were first subjected to FTC stress as preconditioning and subsequently to an EM test with test condition E2 ($J = 2.5$ MA/cm^2, $T = 150$ °C). The selected FTC stress conditions assure that none of the samples in the test population would fail due to the FTC preconditioning.

Table III summarizes the FTC stress conditions. Virgin devices were also subjected to the same EM test for comparison. Only the extrusion failure mode was monitored. Devices with package type B were subjected to pre-stressing with all the conditions shown in Table III. For comparison, package type A received only a subset of these. The frequency of 10 Hz and duty

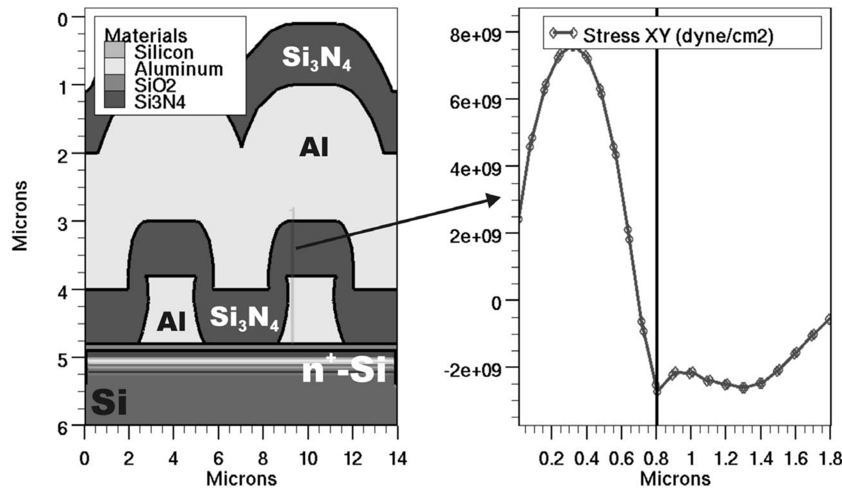

Fig. 9. Thermal stress due to thermal expansion mismatch due to an increase from room temperature to the EM test temperature of 150 °C.

TABLE III
FTC STRESS CONDITIONS

Name	**t**[hrs]	**T**[°C]	$\mathbf{T_{min}}$[°C]
Fresh	-	-	-
F1	16	160	46
F1’	16	160	65
F2	32	160	46
F3	4	200	46
F4	8	200	46

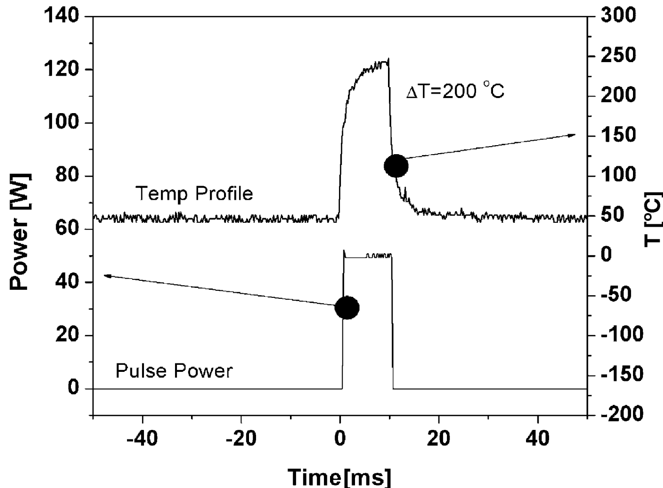

Fig. 10. Temperature cycling profile in case of temperature range of 200 °C. Only one cycle is shown.

cycle of 10% was used for all the FTC conditions as shown in Fig. 10. The amplitude was chosen such to obtain a temperature cycle profile with $\Delta T = 200\,^{\circ}\mathrm{C}$ and $T_{\min} = 46\,^{\circ}\mathrm{C}$.

Fig. 11 shows the reduction of the EM lifetime as a function of the pre-stress time (length of FTC pre-stressing) for two pre-stress conditions with a different temperature swing. The larger EM-lifetime reduction is observed with a longer FTC pre-stress time as well as with a larger temperature swing. As reported previously [7], an FTC stress with a large ΔT can result in an early failure due to the cracking of the ILD. To avoid failure of a part of the test population as a result of the FTC-pre-stressing,

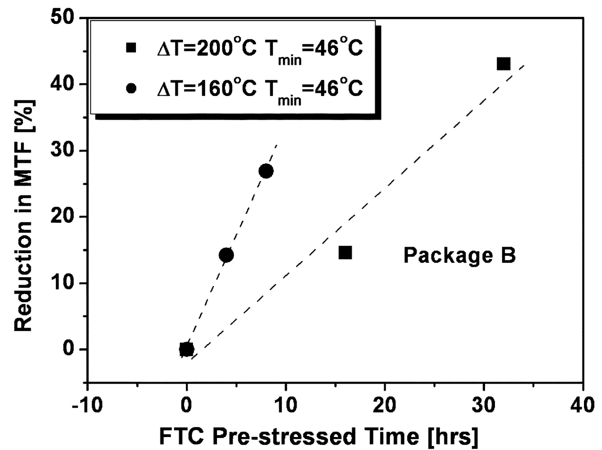

Fig. 11. The reduction in the EM lifetime as a function of the pre-stress time for two FTC temperature swings. EM test conditions: $J = 2.5$ MA/cm^2, $T = 150\,^{\circ}\mathrm{C}$.

the press-stress conditions should be carefully chosen. FTC pre-stressing with low ΔT and long time is recommended.

Mechanical stress and strain from the plastic package can cause parametric shifts and physical damage to passivation and metallization layers. Edward *et al.* have extensively studied the generation of mechanical stress from plastic packages in detail [15]. They have shown that the moulding compounds as well as die attach materials play an important role in the generation of the mechanical stress. The moulding compounds and die attach materials can cause a compressive stress and a stress gradient on the silicon die, respectively. These stresses can cause cracks in passivation layers or be transferred to the metal layers. A significant amount of experimental data has been collected in this area [15]–[17]. The effect of mechanical stresses on the EM lifetime already reported in literature [18].

Fig. 12 shows the EM results with condition E2 on virgin devices encapsulated in packages type A and type B. The MTF and slope (β) were extracted (see Table IV). It can be seen that the MTF of the package type B is larger that that of the package type A. The slope is only slightly different so that the failure mechanism is supposed to be the same. Considering the sample size and the sample selection procedure (see Section II), we cannot

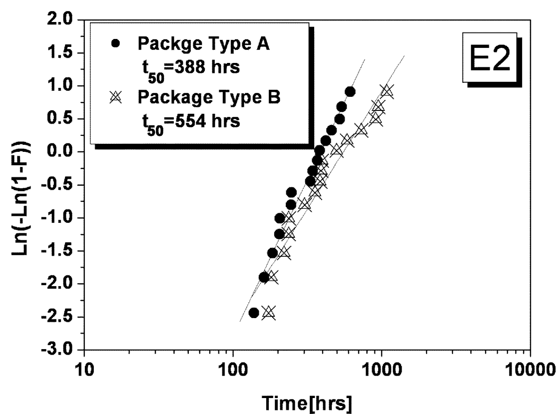

Fig. 12. Failure probability plots for electromigration tests at $J = 2.5$ MA/cm^2 and $T = 150\,^\circ$C for packages type A and B.

TABLE IV
EM RESULTS WITH FTC AS PRE-STRESS

FTC Pre-stress	EM Test	Package B MTF [hours]	Package B β	Package A MTF [hours]	Package A β
Fresh	E2	554	1.6	388	1.8
F1	E2	473	2.3	326	1.9
F1'	E2	428	1.5	275	1.5
F2	E2	315	2.2	*	*
F3	E2	475	1.5	*	*
F4	E2	405	1.2	*	*

* Experiments were not necessary for the comparison of the two package types

conclude whether the difference in MTF should be attributed to the package properties or is a result of wafer-to-wafer variations. However, in view of the possible differences per package as mentioned above, it is clear that the effect of the FTC on the EM lifetime should be characterized using one type of plastic package.

The results of the EM tests with FTC pre-stressing are summarized in Table IV. The EM lifetime is significantly reduced when an FTC pre-stress is applied for both package types. Apparently, FTC damages the stressed line by inducing voids and/or degrades the ILD by inducing micro-cracks or outgrowth of existing cracks. Voids in the metal line result in a local high current density that enhances the EM. Cracks result in a decrease of the facture resistance of the ILD, shortening the time for the stress induced by the EM to exceed its fracture resistance. Consequently, the EM lifetime is reduced. Note that, like other temperature treatments FTC will also affect other metallization properties such as Cu dissolution, diffusion and precipitation and Al crystal defect annealing. Therefore, the EM lifetime could also be enhanced after the preconditioning. We did not observe any increases of the EM lifetime in our experiments. Apparently the currently employed annealing in the fabrication process already result in maximum EM strength.

Like the conventional thermal cycling stress, FTC can also induce voids in the metal line as shown in Fig. 13(b). The voids were observed on the cross-section of the metal line after a few hours with FTC stress. The cross-section of the virgin metal line shows no voids [see Fig. 13(a)]. The introduction of voids by the thermal cycling has been extensively studied in literature [19],

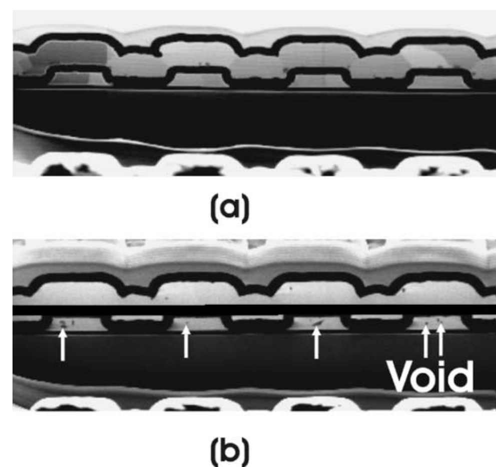

Fig. 13. FIB cross-section of test structures. (a) Fresh device showing no void on the metal line. (b) The metal line after a few hours of fast thermal cycling stress showing voids.

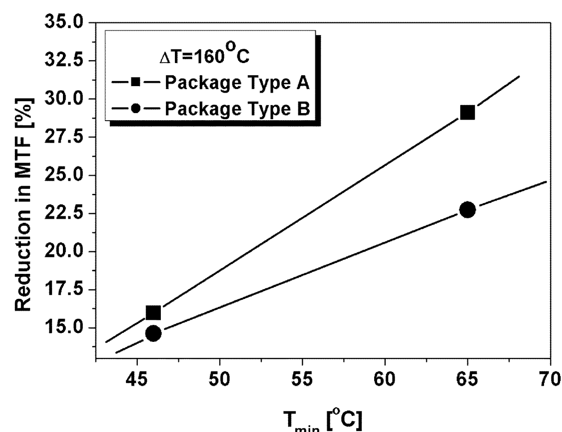

Fig. 14. Reduction in the EM lifetime as function of the $T_{\min}$ of the FTC.

[20]. They showed that the voids nucleation rate depends on the thermal cycling condition such as temperature range, number of cycles, and cycling frequency. This can imply that the reduction of the EM lifetime strongly depends on the FTC conditions. We have already shown the dependence of EM-lifetime reduction on the pre-stress time and the temperature swing in Fig. 11. An additional experiment was performed keeping the temperature swing constant at $\Delta T = 160\,^\circ$C but changing the value of the minimum and maximum temperature. Fig. 14 compares the EM lifetimes of devices pre-stressed with conditions F1 ($T_{\min} = 46\,^\circ$C, $t = 16$ hrs) and F1$'$ ($T_{\min} = 65\,^\circ$C, $t = 16$ hrs). From Fig. 14 it is clear that the reduction in the EM lifetime depends on the $T_{\min}$ and $T_{\max}$. An increase in $T_{\min}$ results in an increased reduction in the EM lifetime. This was observed for both package types. As discussed above, the FTC can accelerate the EM by inducing: 1) stress voiding in the metal line and 2) cracks (micro-cracks) in the ILD.

Our previous reliability tests with the FTC only, showed that the FTC stress with the same ΔT and higher $T_{\min}$ result in a longer FTC lifetime [7]. In this case the failure mechanism is the cracking of the ILD. This indicates that fewer or smaller cracks (or micro-cracks) are induced during an FTC stress with a higher $T_{\min}$. Fig. 14 shows enhanced EM when applying an FTC pre-

stress at higher $T_{\min}$. When $T_{\min}$ increases the average temperature increases. This may result in an increased void density, resulting in an enhanced EM. Apparently, the stress-voiding manner is dominant in the acceleration of the EM, probably because the ΔT is too small to cause the crack or micro-crack in the ILD.

IV. Conclusion

This work has demonstrated a potential failure mode in multilevel interconnects where a combination of fast thermal cycling and electromigration can result in early failures due to extrusion induced short circuits. This problem can be especially severe for power ICs. An EM-lifetime reduction as a result of fast thermal cycling pre-stress has been shown. The reduction in the electromigration lifetime increases for larger temperature swings as well as for increased minimum temperature.

Two-dimensional EM simulations in combination with a no-cracking condition analysis predict that the extrusions mostly happen away from the anode. This is confirmed by the results of failure analysis.

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