A 2.5–10-GHz Clock Multiplier Unit With 0.22-ps RMS Jitter in Standard 0.18-μm CMOS

Remco C. H. van de Beek, *Member, IEEE*, Cicero S. Vaucher, *Senior Member, IEEE*, Domine M. W. Leenaerts, *Senior Member, IEEE*, Eric A. M. Klumperink, *Member, IEEE*, and Bram Nauta, *Member, IEEE*

***Abstract*—This paper demonstrates a low-jitter clock multiplier unit that generates a 10-GHz output clock from a 2.5-GHz reference clock. An integrated 10-GHz *LC* oscillator is locked to the input clock, using a simple and fast phase detector circuit that overcomes the speed limitation of a conventional tri-state phase frequency detector due to the lack of an internal feedback loop. A frequency detector guarantees PLL locking without degenerating jitter performance. The clock multiplier is implemented in a standard 0.18-μm CMOS process and achieves a jitter generation of 0.22 ps while consuming 100 mW power from a 1.8-V supply.**

***Index Terms*—Charge pump, clock multiplication, clock generation, clock multiplier unit (CMU), CMOS, frequency detector, frequency multiplication, frequency synthesizer, high speed, low jitter, low noise, phase frequency detector (PFD), phase detector, phase locked loops (PLL), phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

THE rapid increase in bandwidth of optical networks, such as SONET/SDH, presents a challenge for circuits operating at the interface between the electrical and optical domain. In a complete SONET serializer-deserializer (SerDes) system the received optical datastream is converted from high-speed serial to low-speed parallel. After processing, it is converted to high-speed serial for transmission. For this purpose, several phase-locked loops (PLLs) are used to perform clock and data recovery at the input, clock clean-up, and clock generation for the high-speed output stream. The complete system has to comply with a combination of jitter specifications: jitter tolerance, jitter transfer, and jitter generation. In this paper, we focus only on the data serializer that multiplexes several data streams into one high-speed serial bitstream. Consequently, jitter generation is the main performance indicator for our IC. Multiplexing requires a high-speed low-jitter clock multiplier unit (CMU) to generate accurate timing of the outgoing high-speed bitstream (see Fig. 1). State-of-the-art CMUs implemented in a standard CMOS technology operate with an input signal of 622 MHz and output a signal with a frequency of 10 GHz [1].

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R. C. H. van de Beek was with the University of Twente, 7500 AE Enschede, The Netherlands. He is now with Philips Research Laboratories, 5656AA Eindhoven, The Netherlands (e-mail: remco.van.de.beek@philips.com).

C. S. Vaucher and D. M. W. Leenaerts are with Philips Research Laboratories, 5656AA Eindhoven, The Netherlands.

E. A. M. Klumperink and B. Nauta are with the University of Twente, MESA+ Research Institute, 7500 AE Enschede, The Netherlands.

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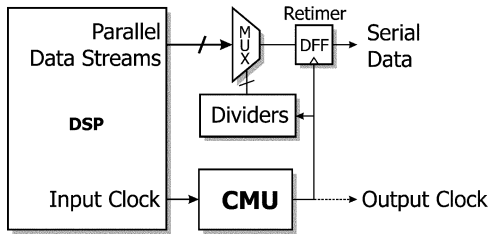


Fig. 1. General multiplexing transmitter architecture.

The conventional implementation of a CMU uses an integer-N phase-locked loop (PLL), where the output clock is generated by a voltage-controlled oscillator (VCO) which is locked to the parallel-input clock via a frequency divider. A different approach is seen in recent papers and uses a frequency multiplying delay-locked loop (DLL) [2]–[4]. However, for high output frequencies, the edge combiner used in these designs is hard to design and will consume a significant amount of power. Locking an *LC* oscillator to the reference clock enables lower power usage and low output jitter [5]. Also, the area consumed by the integrated inductor becomes less of a problem with increasing output frequencies.

Using a conventional tri-state phase frequency detector (PFD) to control the PLL can be problematic in high-frequency clock converters because of the inherently slow local feedback loop present in PFD circuits [6]. To enable high reference frequencies we propose a faster phase detector (PD) design [7], [8] that generates output signals comparable to those produced by a conventional PFD. This PD design lacks a feedback loop, which is possible by using the readily available in-phase and quadrature-phase (I and Q) signals from the PLL frequency divider.

This paper exploits the proposed PD in a low-power low-jitter clock multiplier unit capable of running at an input frequency of 2.5 GHz [8] and generating a 10-GHz output. In order to prove the concept of the fast PD, we chose to use this 2.5-GHz reference instead of the conventional 622 MHz in a 10-Gb/s SONET system. Although this is not according to the SONET standard, our focus was to make faster circuits in a given IC technology, therewith deviating from an industrial standard. However, applications of a faster PD can be also be found outside SONET standards. Using 2.5 GHz as reference enables serializing high-speed data streams without pre-dividing the reference clock which would lead to jitter degradation.

Apart from low close-in phase noise, which is due to the high-speed PD used, employing a high-quality *LC* oscillator led

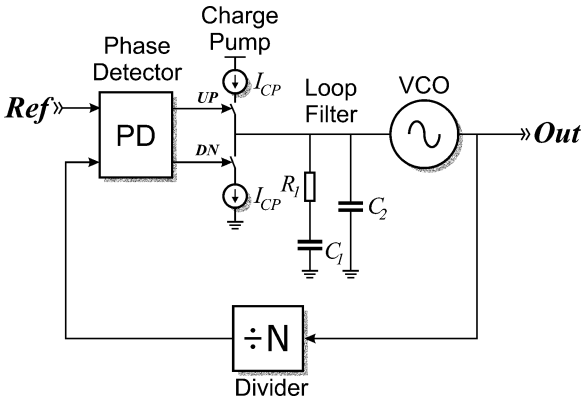


Fig. 2. Charge pump integer-N phase-locked loop.

to low phase noise further from the 10-GHz carrier, resulting in a low total integrated rms jitter.

The contents of this paper are as follows. Section II of this paper motivates the use of a high-speed phase detector on the grounds of the low jitter requirement of optical transmitters, followed by a description and detailed analysis of the proposed PD circuit. Section III then describes the complete CMU design that was integrated in a standard 0.18-μm CMOS technology. The experimental results of this CMU are presented in Section IV, followed by the conclusions in Section V.

II. High-Speed Phase Detection

To guarantee low bit-error rates at the receiver side, an optical transmitter has very strict specifications concerning its clock multiplier's output jitter, which is proportional to the integral of the phase noise power spectral density [9]. In an integer-N PLL clock multiplier architecture (see Fig. 2), the output jitter is caused by both the VCO phase noise (which can be kept low by using a high-quality *LC* oscillator) and the noise of the other PLL components, as well as jitter present on the reference signal. These last jitter contributions appear at offset frequencies below the PLL bandwidth (and are referred to as in-band phase noise here) and generally result in at least 50% of the total jitter [10]. Low in-band phase noise is therefore an important issue.

The in-band phase noise of the CMU can be shown to depend heavily on the ratio of the output frequency and the reference frequency at the input of the PLL [10]. The low-frequency jitter component that is influenced most by this ratio is the jitter due to the charge pump (CP) noise, which is the dominant source of in-band phase noise in most high-frequency transmit PLLs. The transfer of charge pump noise current to PLL output phase noise can be described analytically using PLL building block parameters [10]:

$$S_{\phi_{\rm CP}} = S_{i_{\rm CP}} \left| \frac{\frac{Z(j\omega)\frac{K_{\rm VCO}}{j\omega}}{1+\underbrace{\frac{I_{\rm CP}}{2\pi}Z(j\omega)\frac{K_{\rm VCO}}{j\omega}\frac{1}{N}}_{\text{PLL open-loop gain}}}}{} \right|^2 \quad [\text{rad}^2/\text{Hz}] \qquad (1)$$

where the phase noise offset frequency is given by ω, $S_{i_{\rm CP}}$ is the charge pump noise current spectrum in A^2/Hz, $I_{\rm CP}$ the charge pump current, $Z(j\omega)$ the loop filter impedance, $K_{\rm VCO}$ the VCO gain, and N the frequency ratio of the output signal and the PLL reference clock.

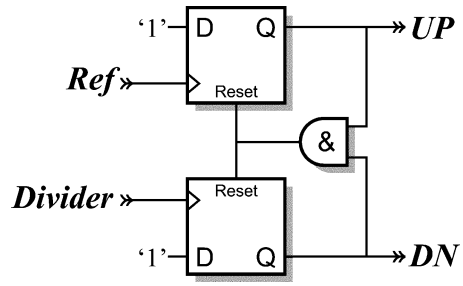


Fig. 3. Common tri-state PFD implementation.

The in-band phase noise spectrum resulting from the CP can be calculated by realizing that the PLL open-loop gain is much higher than 1 for offset frequencies smaller than the PLL bandwidth, yielding the following approximation:

$$S_{\phi_{\rm CP,in-band}} \simeq S_{i_{\rm CP}} \frac{4\pi^2 N^2}{I_{\rm CP}^2} \ [\text{rad}^2/\text{Hz}] \qquad (2)$$

showing a quadratic dependency of the in-band phase noise power density on the loop multiplication ratio N.

Now it is apparent that the loop multiplication ratio N should be kept as low as possible, as this number directly affects the generated CMU output jitter. To keep N as low as possible, the 2.5-GHz reference clock should be applied to the input of the PLL directly, without using a reference divider. Doing this results in a low in-band phase noise level, which in turn yields low jitter generation by the CMU.

Apart from low jitter, a low in-band phase noise level will also lead to a high optimized PLL loop bandwidth [10], resulting in smaller loop filter capacitor dimensions than when using a reference divider. This in turn opens the way to a fully integrated PLL implementation.

A. Conventional Phase Frequency Detector

Standard integer-N PLL architectures often incorporate a tri-state PFD, such as depicted in Fig. 3, to detect the phase difference between the divided output signal and the reference signal. The PFD offers the ability to control a charge pump that will have little activity when the loop has achieved lock, resulting in low in-band phase noise and low reference breakthrough. It also provides frequency-error detection and thus a large PLL capture range. Another advantage of the PFD is that it is edge triggered, which makes the phase detection performance independent of the duty cycle and amplitude of the signals on the detector inputs.

On the other hand, the conventional PFD has an important operation speed limitation, due to the feedback loop that is present to reset the PFD to its neutral state, where neither the *UP* nor the *DN* signal are active [6]. The consequence of this speed limitation is a limitation of the reference frequency that is supplied to the PLL. For correct operation of the PFD, the PLL comparison frequency must not be higher than $1/(2T_r)$, where T_r is the time needed to reset the PFD [6]. This time includes the delay of the AND gate and the propagation time inside the D-flip-flops.

If the reference frequency exceeds the maximum PFD operation frequency, a trivial solution is to use a reference divider preceding the PLL to decrease the comparison frequency at the PFD input. However, (2) predicts this will lead to increased in-band phase noise. Another possible disadvantage is that decreasing the comparison frequency decreases the maximum achievable PLL loop bandwidth [11].

One could also opt to use a faster PD structure, preferably a simple design without the need for internal feedback. A well-known option is the XOR gate. Using an XOR also has some disadvantages. The loop will not lock to a phase difference of zero degrees, which will cause a much higher reference breakthrough, and thus higher output spurs. Also, the XOR PD has duty-cycle dependent behavior [12], which is usually a problem. Finally, the XOR gate does not provide a frequency detection means and thus has a limited lock-in range.

B. Proposed Phase Detector

Having established that the main speed limitation of the PFD is the relatively slow reset path led to investigate the possibility of removing the PFD reset loop altogether, while preserving the most important property of the PFD: the generation of concurrent *UP* and *DN* pulses. The latter is desirable because of the ability to control a charge pump with no net activity in lock.

Observing the basic functionality of the PFD building block reveals that the reset signal is needed to put the detector in its *neutral* state. In the case of phase lock, this signal will always go high a small amount of time after the rising edge of both PFD input signals. When using a static divide-by-two frequency divider in the PLL, which inherently generates *I* and *Q* signals, we see that the quadrature divider signal has a transition some time after the rising edge of the in-phase divider signal. To avoid generation of the reset signal in a feedback loop, the possibility of using the quadrature divider signal as a reset signal was examined.

We can derive a set of simple rules for a fast PD able to control a charge pump, using the quadrature divider output signal as reset signal.

1) The *UP* signal will go high after a rising edge of the reference clock *Ref*.
2) The *DN* signal will go high after a rising edge of the in-phase divider signal *DivI*.
3) Both *UP* and *DN* signals will be reset after the next falling edge of the quadrature divider signal *DivQ*.

The effect of these rules are shown graphically in Fig. 4(a), for the case that the PLL is close to lock. Observing the PD input and output signals, we conclude that the simplest implementation of this behavior can be described as:

$$UP = Ref \text{ AND } DivQ$$
$$DN = DivI \text{ AND } DivQ$$

with AND being the Boolean AND operation. The phase detector circuit implementing this behavior is shown in Fig. 4(b). In [7], this two-AND phase detector type has been proposed for a CMU for purposes of increased jitter tolerance and handling missing input clock pulses.

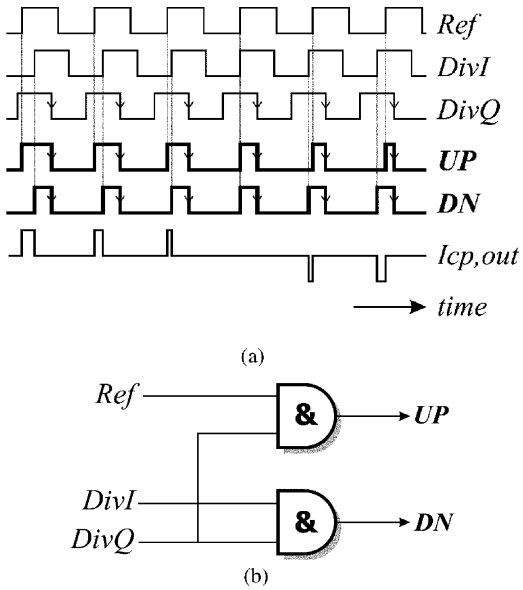


Fig. 4. PD response and implementation. (a) Desired PD response; (b) PD circuit implementation.

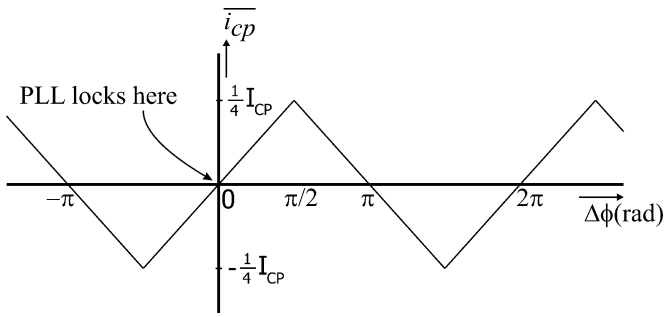


Fig. 5. Mean CP current as a function of the phase error.

Note that the width of the *UP* pulse responds *linearly* to the time overlap of *DivQ* and *Ref*. The width of the *DN* pulse depends on the time overlap of *DivQ* and *DivI*. In lock, with coinciding rising edges of *Ref* and *DivI*, the *UP* pulse has the same width as the *DN* pulse.

When the *UP* and *DN* signals are supplied to a charge pump, the net charge pumped in the PLL loop filter is linearly dependent on the phase difference detected, for phase differences close to zero degrees. This can be concluded from Fig. 5, where the mean charge pump current is plotted as a function of the PLL input phase difference. Note that this graph applies to infinitely fast AND gates and an ideal CP transfer. Fig. 5 shows that the gain of the PD/CP combination is $I_{\mathrm{CP}}/2\pi$, where I_{CP} is the maximum charge pump current. Because of the integrating action of the CP and the loop filter, the PLL will lock to a phase error of 0 degrees, as indicated in Fig. 5. Because the *UP* and *DN* pulses and the corresponding charge pump currents will cancel in lock, the reference breakthrough will be small resulting in low spurious peaks, similar to the case in which a conventional PFD is used.

In Fig. 6, the dependence of the PD/CP response on the 90° quadrature quality is shown. Although the range in which the PD stays linear is affected by the phase angle between *DivI* and

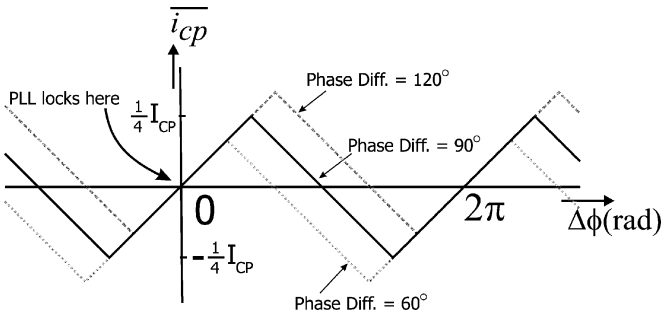


Fig. 6. Influence of imperfect quadrature on PD response.

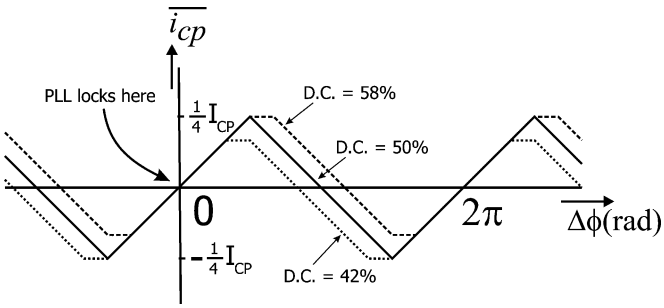


Fig. 7. Influence of reference duty cycle on PD response.

DivQ, the PD gain is unaffected, as is the locking point of the PLL. The linear region ranges from $\Delta\phi_q - \pi < \Delta\phi < \Delta\phi_q$, where $\Delta\phi_q$ is the phase difference between *DivI* and *DivQ* and $\Delta\phi$ is the phase error of the PLL. In the case of ideal quadrature (when the phase difference between *DivI* and *DivQ* is $\pi/2$), the linear range is between $-\pi/2$ and $\pi/2$.

Fig. 7 shows that the gain and the PLL phase error in lock also do not depend on the duty cycle of the reference. The same holds for the dependence on the duty cycles of *DivI* and *DivQ* (not plotted here). The linear region is again affected by duty cycle deviations. For a reference duty cycle lower than 50%, the linear region is between $-\pi/2 < \Delta\phi < 2\pi(\mathrm{DC} - 1/4)$, with DC being the reference duty cycle. If DC $> 50\%$, the linear region is between $-2\pi(3/4 - \mathrm{DC}) < \Delta\phi < \pi/2$. Note that for correct operation of the PD, the reference duty cycle can vary amply between 25% and 75%. In the case where the duty cycle is 50% the linear range is between $-\pi/2$ and $\pi/2$.

The plots shown so far all apply to infinitely fast AND gates and charge pump circuitry. Fig. 8 shows the simulated transfer of the PD/CP combination as implemented in the clock multiplier chip, discussed later in this paper. The figure shows the simulated mean charge pump output current as a function of the phase difference between the reference and the *DivI* signal, at 2.5-GHz input frequencies (the charge pump current I_{CP} is 100 μA). There is a nearly flat response around input phase differences of about $-\pi/2$, due to the fact that the time overlap of the reference and the *DivQ* signal becomes very small here. As the PLL will not lock in this region, this effect will not cause any problem. One can see that there is no gain degradation around zero degrees phase error, showing that the PD/CP combination does not have a dead-zone problem.

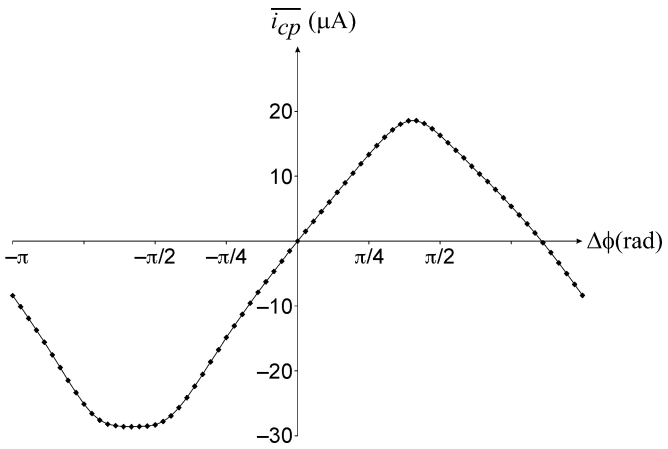


Fig. 8. Simulated PD/CP response as function of phase error.

Note that in [13], a PD is used that at first sight looks similar in design to the proposed PD. However, in [13], three-input AND gates are used, which are generally slower than two-input AND gates, as used in the proposed PD. More importantly, in that work, the lengths of the *UP* and *DN* pulses approach zero when the PLL is in lock. Because neither the output voltages of the AND gates nor the current sources of the CP are infinitely fast, the structure proposed there will have a dead-zone problem. This means that the gain of the PD/CP combination will drop significantly as the phase difference approaches zero. The PD we propose does not suffer from this problem as the *UP* and *DN* signals maintain a duty cycle of about 25% when the PLL is locked, because there is an overlap between the input signals of the AND gates.

Besides the basic two-AND solution, [7] proposes some additional digital circuitry to reduce the width of the *UP* and *DN* pulses, without creating a dead zone. At lower operating frequencies, this technique could have been used in a CMU to reduce unwanted side effects of both charge pump current sources being on simultaneously, such as extra noise injection into the loop filter or mismatch-induced reference feed-through. However, because the PD has to operate at 2.5 GHz, the *UP* and *DN* pulse widths could not be reduced. Simulations showed that reducing the pulse width significantly would lead to incomplete switching of the CP current sources, resulting in a PD gain degradation (dead zone).

III. CMU Design

Fig. 9 shows the top-level block diagram of the CMU. The block diagram shows the use of the novel phase detector design in combination with a frequency detector (FD), the need for which will be demonstrated shortly. Both detectors control a separate charge pump. The VCO output signal of about 10 GHz is passed through two static divide-by-2 circuits to generate the 2.5-GHz signal that is locked to the CMU reference clock. The second divide-by-two stage delivers the *I* and *Q* signals needed by the PD and FD. Note that for the loop around the FD, a zero is unnecessary because the VCO is merely a gain element in the frequency domain; this explains the direct connection of the

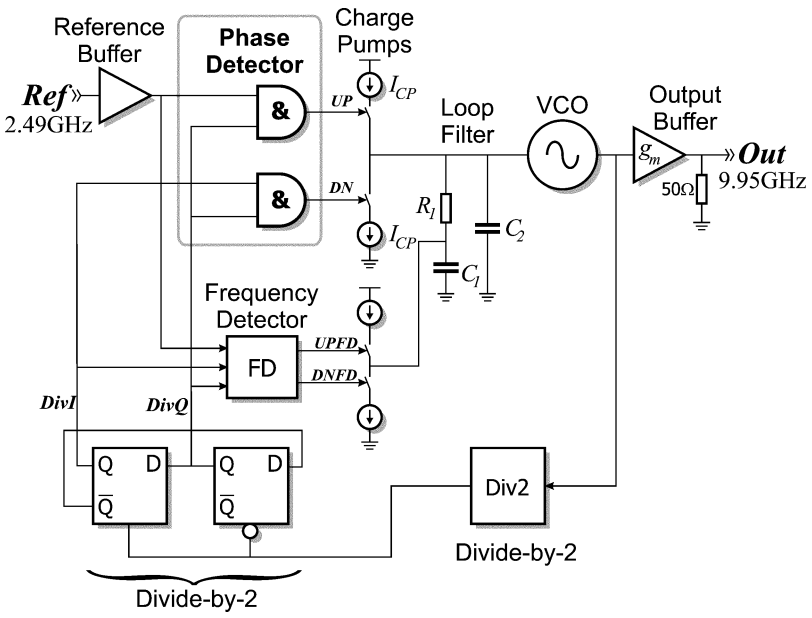


Fig. 9. Architecture of the clock multiplier unit.

FD controlled charge pump in Fig. 9 to the largest loop filter capacitor.

A. Lock Behavior

High-level simulations using Simulink (a graphical MatLab shell) were performed with the presented CMU structure. The goal of these simulations was to study the lock behavior of a PLL with the proposed PD, with and without FD.

Before frequency lock is achieved, the phase difference between the reference and the *DivI* signal varies almost linearly with time. This means that the mean charge pump current of the CP that is controlled by the PD will be the mean value of the PD/CP transfer curve (such as shown in Fig. 8). For an ideal PD/CP combination, the mean current will be equal to 0 A. In practice, however, the mean CP output current will be nonzero. Because of the integration of this current by the loop filter, the VCO frequency will drift, possibly away from lock.

To ensure correct locking of the loop, a frequency detector should be added that drives the VCO frequency toward the reference clock frequency. The mean output current of the CP that is controlled by this FD should be higher than the before mentioned drift current. In this case, the net current will always bring the PLL toward lock.

Simulation results of the high-level implementation of the CMU are shown in Fig. 10. The PLL parameters were chosen equal to those used in the final CMU design. The results clearly show the need for the FD. Without the FD, the drifting effect discussed before drives the PLL away from lock. With the FD enabled, the absolute value of the output current of the CP controlled by the FD is higher than that of the drifting current, driving the average VCO control voltage toward lock.

B. Frequency Detector

The FD implementation is shown in Fig. 11. It is similar to that presented in [14], however, two AND gates were added to generate signals that can directly control a second charge pump.

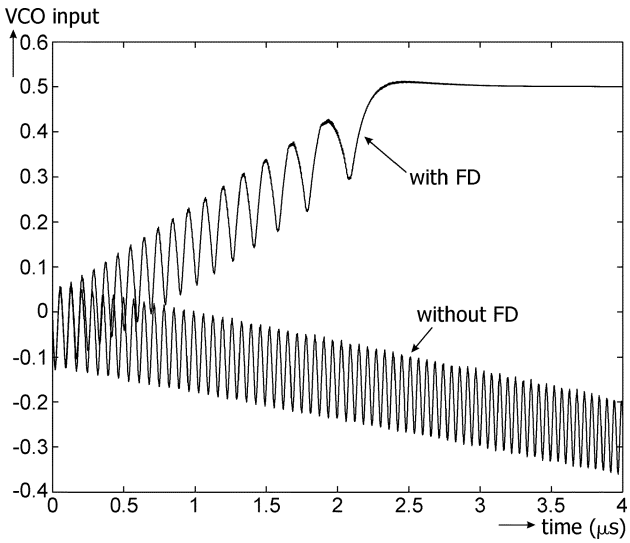


Fig. 10. High-level PLL simulation results.

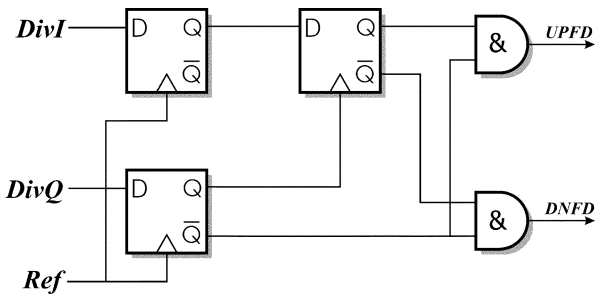
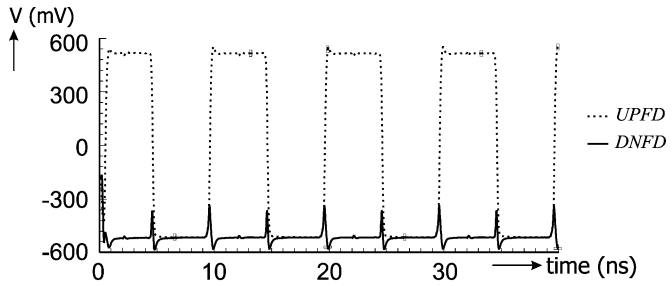
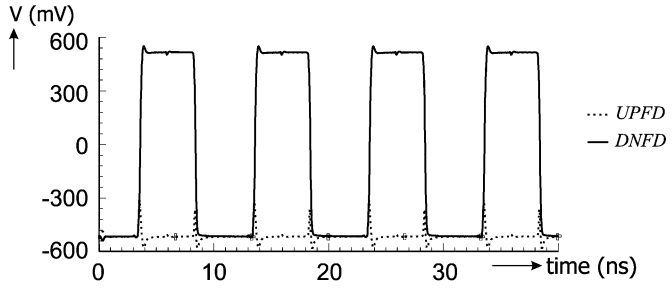


Fig. 11. Frequency detector design.

A strong point of this detector is that as soon as phase lock has been achieved, it will not generate output signals that may disrupt the normal behavior of the loop. This means two things. First, and most importantly, the frequency detector will not contribute in the clock multiplier output jitter. Second, there is no



(a) Divider output freq. = 2.4 GHz



(b) Divider output freq. = 2.6 GHz

Fig. 12. FD response for 2.5-GHz reference signal. (a) Divider output freq. = 2.4 GHz; (b) Divider output freq. = 2.6 GHz.

need to switch off the frequency detector after start-up. When the loop loses lock (e.g., due to a strong disturbance), the FD will automatically become active and bring the loop back in lock. So there is no need for a lock detector circuit.

The reason that the D-flip-flops used in this detector can operate at a higher reference frequency than the D-flip-flops used in a conventional PFD architecture is that the flip-flops in this frequency detector have an output frequency that is equal to the difference between the reference frequency and the frequency of *DivI* and *DivQ*. Also, the flip-flops do not need to be reset asynchronously, which makes their design easier and faster.

The frequency detector can in principle also be used as a phase detector, as described in [14]. However, the gain of this phase detector is not well defined; it depends on the speed of operation and of the waveform of the incoming signals, making stability and loop behavior not as well defined as with the proposed phase detector. Using a separate PD simplifies designing the D-flip-flops because their internal loop gain need not be close to 1, as is needed in [14] to create a sample-and-hold circuit.

Fig. 12 shows simulated output signals of the FD for a reference frequency of 2.5 GHz. The FD was implemented in current-mode logic (CML); an output voltage of $+0.5$ V means that the corresponding charge pump current source is on, -0.5 V means off. The upper graph represents a divider output frequency of 2.4 GHz, resulting in *UPFD* pulses. The lower graph resulted from a divider frequency of 2.6 GHz, in which case the *DNFD* pulses become active. Note that when the FD is active, its output signals have a duty cycle of 50%. This means that the charge pump current source values should be at least twice the drift current discussed earlier (Section III-A) to guarantee locking.

The theoretical input range of the FD is $\pm 25\%$ of the desired VCO frequency. This is high enough in this CMU design, where an *LC* oscillator is used of which the tuning range plus the expected process spread plus temperature variations are expected to be well below that.

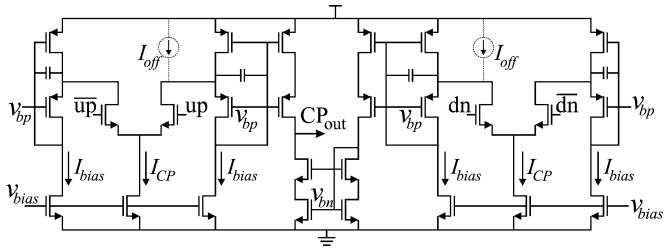


Fig. 13. Charge pump circuitry.

C. Charge Pumps

The charge pump controlled by the PD should be able to process the *UP* and *DN* signals at the speed of the reference signal (2.5 GHz). Because of the relatively high duty cycle of the PD signals, low-noise operation is an important issue.

Fig. 13 shows the CP circuit that is used, based on [15]. Both the *UP* and the *DN* signals are processed by an NMOS differential pair. This ensures input symmetry and high speed. The tail current source transistors have a high overdrive voltage to decrease their white-noise contribution. The transistors are large enough to ensure a negligible $1/f$-noise contribution to the CMU's output jitter.

The resulting *UP* and *DN* currents are processed by current mirrors. Although the shape of the output current of these mirrors is different from the input current shape due to the mirror poles, it can be shown that the total *charge* put into the mirror is copied to the output accurately [15]. As long as the mirror pole frequencies are much higher than the PLL loop bandwidth, the mirror poles will not disrupt loop behavior.

Low-voltage PMOS mirrors were used to ensure correct operation of the NMOS differential pairs. Simple two-transistor PMOS mirrors would drive the NMOS transistors of the input stages out of saturation because of the high-voltage drop the input PMOS transistor would require. The NMOS transistor being in triode means that either the differential output swing of the PD or the NMOS widths have to be increased to fully switch the tail current. Both methods decrease the maximum operation speed of the PD/CP combination. A third method of solving the problem would be to use level-shifters to connect the PD to the CP, also decreasing performance.

Another advantage of using low-voltage mirrors is the high output impedance obtained by cascoding. This increases the *UP* and *DN* current matching, as the CP output current is less sensitive to the VCO control voltage than without a cascoded CP output stage.

The capacitors in the PMOS mirrors are necessary to provide a fast feed-forward path from the input of the PMOS mirror to the gates of the upper mirror transistors. Without the capacitor, the high-frequency input impedance of the PMOS mirror would be high. This would cause a voltage drop on the input node every time the NMOS differential pair receives an input pulse, causing the NMOS transistor to go out of saturation. The capacitor also

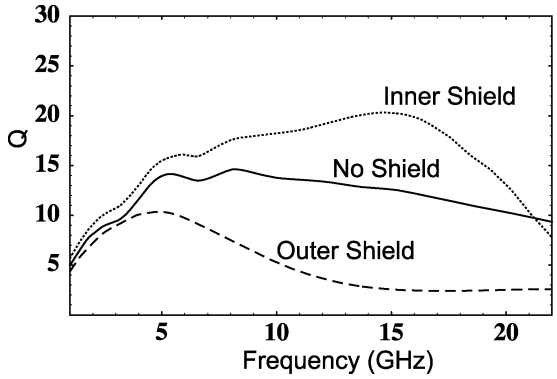


Fig. 14. Measured influence of shielding on the quality factor of the inductor.

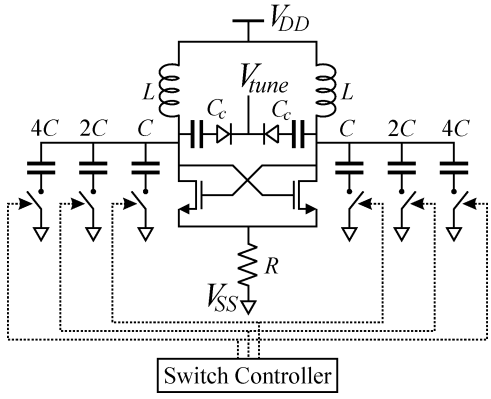


Fig. 15. Overall VCO schematic.

provides frequency compensation of the feedback loop present in the PMOS mirror to prevent ringing.

A disadvantage of the use of low-voltage mirrors is the need of an extra bias current, thus increasing the CP noise. However, because this bias current is just a fraction of the CP current, this was not a problem.

For the frequency detector CP, two pull-up current sources were added (shown dashed in Fig. 13) to completely switch off the CP output current when in lock, in order to decrease the noise contribution of this CP when the PLL is in lock (and no FD output pulses are generated), which would otherwise be caused by the mirroring of the bias currents.

D. VCO

The *LC* VCO has to operate at 10 GHz at a low phase noise level, demanding several careful design considerations. An important issue is the design of a monolithic planar inductor. Shielding the inductor toward the substrate reduces noise coupling from the substrate and increases the inductor's quality factor. Normally, the shield is patterned in order to prevent circular currents from flowing. The pattern is made with grounded poly-silicon bars. This grounding can be done from the outerside or innerside of the bars. Measurements reveal that inner grounding is the best option to get the maximum quality factor at high frequencies (see Fig. 14).

In recent work, the relation between the inductance value and the phase noise in the voltage-limited and current-limited region of the VCO is established [16]. The value of the inductor (0.3 nH) is chosen so that the oscillator operates at the edge of the voltage-limited region. The geometry of the inductor is a single turn circle, realized in metal layers 3, 4, and 5.

The varactor used is a differential PMOS p+ drain/source diffusion in an n-well. The quality factor is approximately 6, making it the limiting element in this design. The $C_{\max}/C_{\min}$ ratio is in the order of 1.2. To increase the tuning range, digital tuning by means of MOS capacitors has been applied. The digital tuning can cope with fabrication spread, without increasing the gain of the VCO. The overall schematic of the VCO can be seen in Fig. 15. Fig. 16 shows the phase noise spectrum of the free-running VCO, measured with a dedicated HP3048A phase noise measurement system.

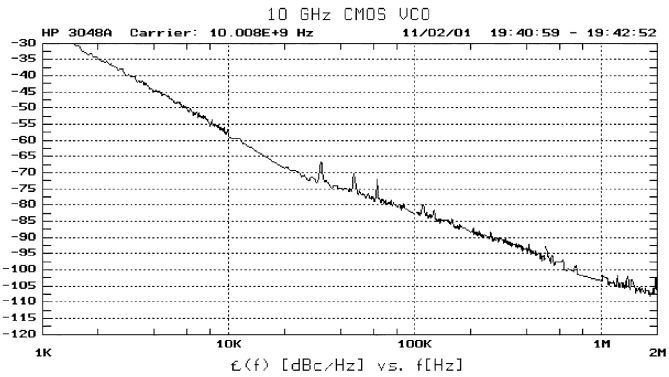


Fig. 16. Measured phase noise spectrum of free-running VCO.

E. Phase Noise Optimization

To determine the optimal PLL loop bandwidth (the bandwidth for which the total jitter caused by the VCO and by other loop components is minimal), we used the assumption that the in-band phase noise would be dominated by the CP noise. The CP noise spectrum was estimated by using steady-state ac noise analyses. The effect of the CP noise on the PLL output phase noise is calculated using (2):

$$\mathcal{L}_{\rm CP} \equiv \frac{1}{2} S_{\phi_{\rm CP,in-band}} = S_{i_{\rm CP}} \frac{2\pi^2 N^2}{I_{\rm CP}^2} \tag{3}$$

where $\mathcal{L}_{\rm CP}$ is the single-sided output phase noise due to the CP noise.

The graph of $\mathcal{L}_{\rm CP}$ is drawn together with the measured phase noise spectrum of the free-running VCO. The optimum loop bandwidth can now be determined from the point of intersection of these two lines [10], as shown in Fig. 17. This works out to be about 2 MHz.

F. Layout

The clock multiplier was realized in a standard 0.18-μm CMOS process with five metal layers, one poly layer, and a substrate resistivity of 10 $\Omega \cdot$ cm. The process did not provide the possibility of triple-well isolation. A die micrograph of the complete CMU is shown in Fig. 18. The area consumed is about 1×1 mm^2, including the bond pads.

All digital circuitry (PD, FD, frequency dividers, and buffers) was implemented using CML to minimize both the sensitivity

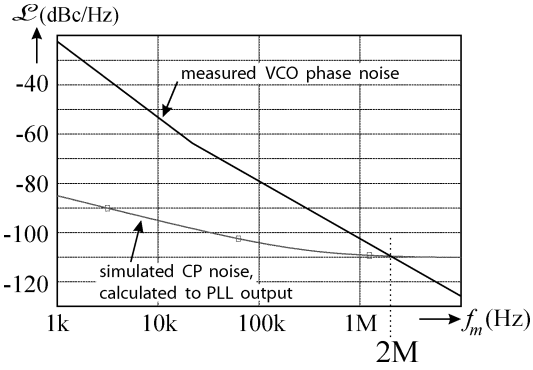


Fig. 17. Determination of optimal loop bandwidth.

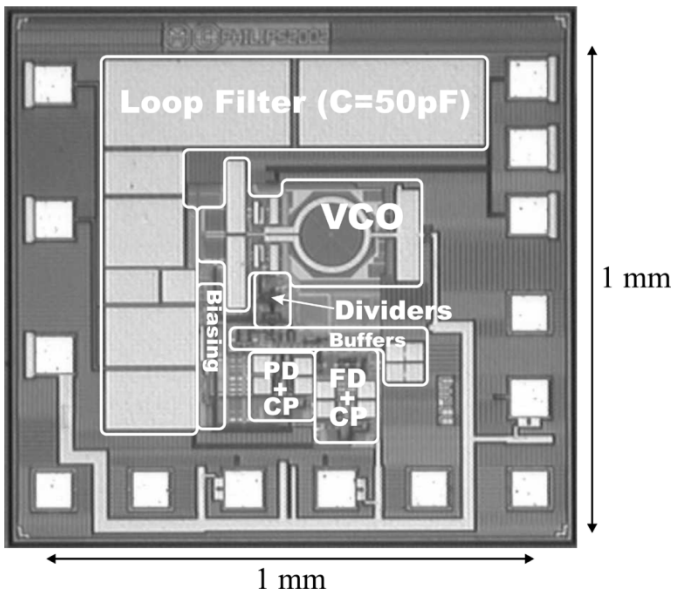


Fig. 18. CMU die micrograph.

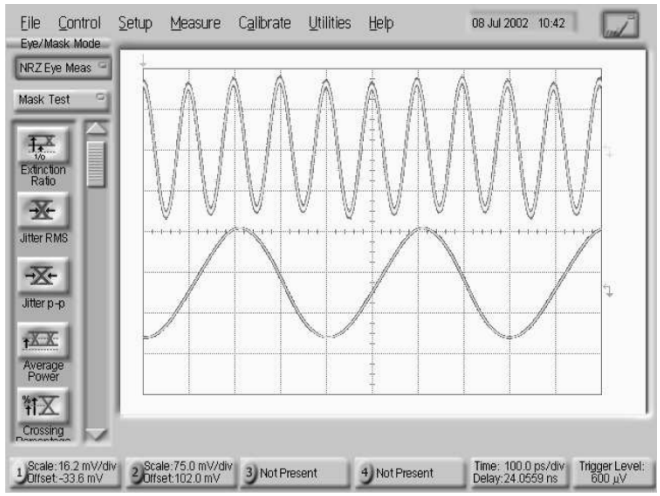


Fig. 19. Oscilloscope screen-dump of reference clock and CMU output.

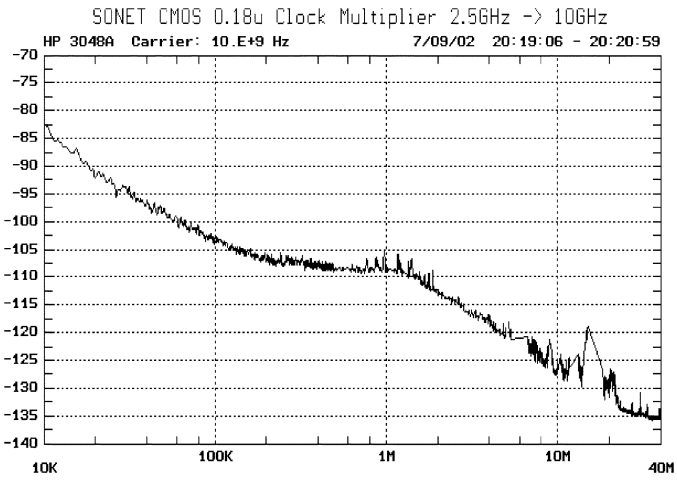


Fig. 20. Measured generated CMU phase noise spectrum.

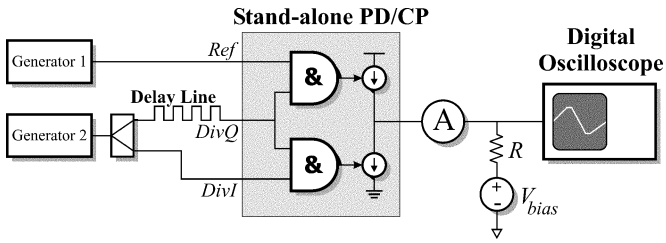


Fig. 21. Setup for PD/CP transfer measurements.

to and the generation of supply noise and substrate bounce. Both the input and the output buffers were terminated with 50 Ω on-chip. The input buffer is ac coupled on chip to adapt to the correct CML levels.

A large portion of the total chip area is taken by the loop filter capacitors (the largest of which has a capacitance of 50 pF). This chip area could have been drastically reduced by using techniques presented in [17]. This was not done however due to a lack of correct capacitor models for these more advanced and dense capacitors; the capacitors were realized with ordinary five-metal parallel plate capacitors.

IV. Experimental Results

Two ICs were fabricated, one with the complete CMU and the other containing the PD/CP and the FD/CP combinations, for open-loop measurements. The results of on-wafer measurements on these chips are presented here.

The 10-GHz output signal generated by the CMU is shown on the Agilent 86100B oscilloscope screen-dump of Fig. 19, together with the 2.5-GHz reference clock, which was derived from a Marconi 2042 signal generator. The reference clock was also used as the trigger signal for the oscilloscope. For practical reasons, the differential buffered VCO output was measured single-ended. The measured CMU power consumption was 99 mW including the 10-GHz output buffer. The estimated consumption without the buffer is 77 mW, of which 25% is consumed by the VCO and 28% by the first divide-by-two. The PD, FD, and charge pumps consume 6 mW.

The oscilloscope could in principle be used to measure the peak-to-peak jitter of the generated clock signal. In this case, however, the generated clock jitter was below the oscilloscope noise floor. To determine the CMU output clock jitter, we used

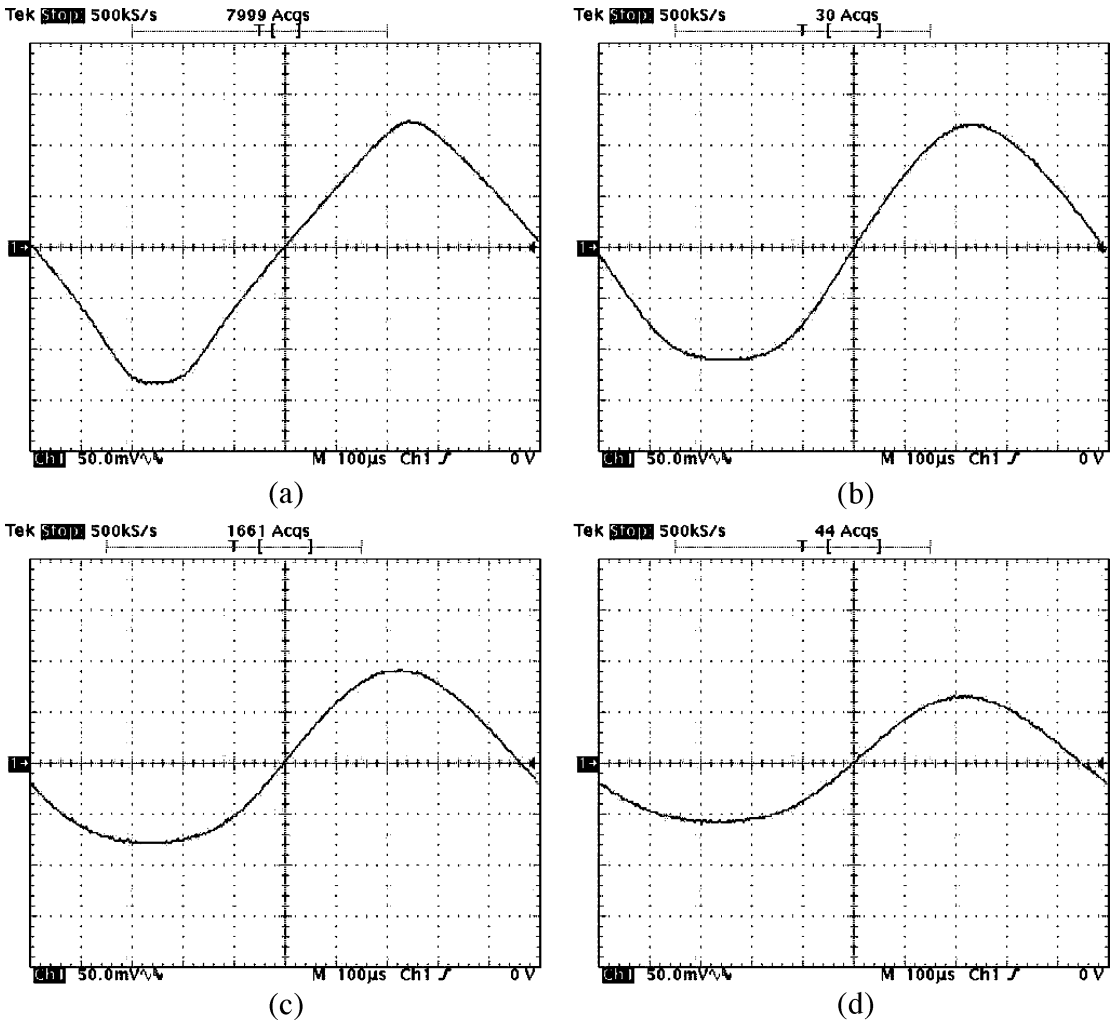


Fig. 22. PD/CP measurement results, measured at (a) 1.0 GHz; (b) 2.5 GHz; (c) 4.0 GHz; (d) 5.0 GHz.

a more accurate phase noise measurement, the results of which were integrated to determine the rms output jitter. Measuring the complete phase noise spectrum has the advantage that it gives a more complete picture of the possible sources of jitter and the optimal setting of the PLL loop bandwidth.

The CMU output phase noise was measured using the HP3048A phase noise measurement setup in PLL configuration. The 2.5-GHz reference to the CMU was derived from a Marconi 2042 signal generator in low noise mode. An HP83731B generator was controlled by the measurement setup to follow the CMU output clock at 10 GHz. The measured phase noise plot of the CMU is shown in Fig. 20. This graph clearly shows the open-loop VCO phase noise (at offset frequencies higher than $\sim$1 MHz) and the in-band phase noise, which is dominated by the charge pump noise.

In order to benchmark our PLL based on the fast PD, we choose to measure according to SONET jitter generation specifications. Integration of the phase noise spectrum using the frequency limits defined for OC-192 SONET systems (50 kHz up to 80 MHz), yields an rms jitter of 0.22 ps (equivalent to 2.2 mUI rms), which is almost a factor 5 lower than the SONET recommendation of 10 mUI rms. A usual rule-of-thumb approximation of the peak-to-peak jitter of a factor of ten times the rms jitter shows a jitter of 2.2 ps peak-to-peak (22 mUI p-p). A performance summary of the CMU chip is given in Table I.

TABLE I
CMU PERFORMANCE SUMMARY

Output Frequency	9.953 GHz
Reference Frequency	2.488 GHz
Technology	0.18µm standard CMOS
Jitter Generation (RMS)	0.8º rms, equiv. to 0.22 ps rms
Jitter Generation (peak-to-peak)	2.2 ps (spec. = 10 ps)
Supply Voltage	1.8 V
Chip Size	0.83 x 0.86 mm^2
Power Consumption	99 mW 81 mW without output buffer

Please note that from the SONET jitter specifications, only the jitter *generation* is important. If the data multiplexer is part of a serial input/serial output regenerator application, the jitter tolerance is resolved in the clock and data recovery PLL and the jitter transfer can be resolved in an external low-bandwidth clean-up PLL [1], or by using external high-Q filtering of the recovered clock [18], [19]. In many cases, the outgoing data

source is a network processor ASIC and the data rate is independent of the incoming data rate. In that case, both ASIC and transmitter are controlled by a separate clean reference clock [1], [18]; jitter transfer and tolerance do not apply to such a system.

The PD speed was measured using the chip containing the open-loop PD and CP combination. The measurement setup is shown in Fig. 21. The two generators deliver two independent signals, close in frequency. The delay line in series with the second generator creates a frequency dependent phase difference between *DivI* and *DivQ*, that can be controlled such that the mean output current of the CP is about zero and falling with increasing input frequency. In that case, the phase difference between *DivI* and *DivQ* is close to 90 degrees.

The PD's input phase difference increases linearly due to the constant frequency difference of the generators. The CP output current will, thus, be a periodic signal with a frequency equal to the difference frequency of both generators and the signal on the digital oscilloscope can be considered a plot of the mean charge pump output current versus PD input phase error.

Fig. 22 shows some of the measured output plots for different PD input frequencies. The first two plots, at 1 GHz and 2.5 GHz, show the expected linear behavior around zero degrees phase offset (the origin of the oscilloscope dump), and the flat area in the third quadrant due to the narrow *UP* pulses described before.

It should be noted that the actual value of the PD input phase error is not be known, in contrast to the value of the CP output current. The actual input phase for which the CP output current equals zero can deviate from zero degrees due to device mismatch errors on the chip, both of the PD AND gates and the CP current sources. Only the CP current mismatch will influence reference breakthrough, a PLL specification that is not crucial in an optical transmitter design. During layout, effort has been taken to minimize CP current mismatch. The fact that cascoded current sources were used greatly reduces the influence of VCO control voltage on CP current mismatch.

The plots measured at higher input frequencies show a slight degradation of both the gain in the origin and the size of the linear range of the PD/CP combination. This is due to the fact that both the *UP* and *DN* pulses become too narrow to fully control the CP.

Measurements performed on a stand-alone FD/CP combination implemented on a single chip showed that the FD had an input range of 23%. This is much higher than the combined VCO tuning range together with its expected process spread.

V. Conclusion

The design and measurement of an experimental 2.5–10-GHz clock multiplier unit in a standard 0.18-μm CMOS process has been presented. The design employs a fast, simple phase detector structure capable of running at input frequencies well beyond the necessary 2.5 GHz. The PD uses readily available frequency divider output signals. It generates pulses like those generated by a conventional tri-state PFD and controls a charge pump with almost no net activity while in lock. Initial PLL locking is achieved with a frequency detector that automatically becomes inactive while in lock, therefore not influencing generated output jitter and spurs. This technique makes a lock-detect circuit superfluous. The CMU achieves an output jitter of 0.22 ps rms, almost a factor 5 lower than the 10-Gb/s SONET recommendation, while consuming 100 mW (including the 10-GHz output buffer). Comparing to state-of-the-art [1], this design realized an approximate factor 3 improvement in peak jitter performance, and 2 to 3 times less power dissipation in a comparable technology.

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Remco C. H. van de Beek (S'99–M'04) was born in 1974 in Wageningen, The Netherlands. He received the M.Sc. degree in electrical engineering in 1999 and the Ph.D. degree on the subject of "high-speed low-jitter frequency multiplication in CMOS" in 2004, both from the University of Twente, Enschede, The Netherlands.

In 2004, he joined the Philips Research Laboratories Eindhoven, where he is currently a Research Scientist in the Integrated Transceivers department. His research interests include gigahertz-range low-jitter clock multiplication, frequency synthesis, high-frequency logic, and RF circuits.

Cicero S. Vaucher (M'98–SM'02) was born in São Francisco de Assis, Brazil, in 1968. He graduated in electrical engineering from the Federal University of Rio Grande do Sul, Porto Alegre, Brazil, in 1989. In 2001, he received the Ph.D. degree in the same field from the University of Twente, Enschede, The Netherlands.

Since 1990, he has been with Philips Research Laboratories, Eindhoven, The Netherlands, where he is a Senior Research Scientist in the Integrated Transceivers Department. His research activities have included implementations of low-power high-speed building blocks for PLL frequency synthesisers, synthesiser architectures for low-phase-noise and fast-settling-time applications, CAD modeling of PLL frequency synthesisers, and data/clock recovery and clock conversion circuits for optical transceivers. Currently, he is involved with analog IC design for microwave applications. He is the author of *Architectures for RF Frequency Synthesizers* (Kluwer, 2002) and a coauthor of *Circuit Design for RF Transceivers* (Kluwer, 2001). He holds 14 international patents on the subject of PLL and receiver design.

Domine M. W. Leenaerts (M'92–SM'96) studied electrical engineering at Eindhoven University of Technology and received the Ph.D. degree in 1992.

From 1992 to 1999, he was with the same university as an Associate Professor of the microelectronic circuit design group. In 1995, he was a Visiting Scholar at the Department of Electrical Engineering and Computer Science, University of California, Berkeley. In 1997, he was an Invited Professor at the Technical University of Lausanne (EPFL). Since 1999, he has been a Principal Scientist at Philips Research Laboratories, Eindhoven, where he is involved in RF integrated transceivers design. His research interests include nonlinear dynamic system theory, ADC/DAC design, and RF and microwave techniques. He has published over 100 papers in scientific and technical journals and conference proceedings, and has written three books, including *Circuit Design for RF Transceivers* (Kluwer).

Dr. Leenaerts is an IEEE Distinguished Lecturer and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I.

Eric A. M. Klumperink (M'98) was born on April 4, 1960, in Lichtenvoorde, The Netherlands. He received the B.Sc. degree from the Hogere Technische School, Enschede, The Netherlands, in 1982.

After a short period in industry, he joined the Faculty of Electrical Engineering of the University of Twente, Enschede, in 1984, where he was mainly engaged in analog CMOS circuit design. This resulted in several publications and a Ph.D. thesis, in 1997, on the subject of transconductance-based CMOS circuits. He is currently an Assistant Professor at the IC Design Laboratory and is also involved in the MESA+ Research Institute. He holds four patents and has authored or coauthored more than 50 journal and conference papers. His research interest is in design issues of HF CMOS circuits, especially for front-ends of integrated CMOS transceivers.

Dr. Klumperink is a corecipient of the IEEE ISSCC 2002 Van Vessem Outstanding Paper Award.

Bram Nauta (S'89–M'91) was born in Hengelo, The Netherlands, in 1964. In 1987, he received the M.Sc. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991, he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high-speed A/D converters. From 1994, he led a research group in the same department, working on analog key modules. In 1998, he returned to the University of Twente as Full Professor heading the IC Design group in the MESA+ Research Institute and Department of Electrical Engineering. His current research interest is analog CMOS circuits for transceivers. He is also a part-time consultant in industry, and in 2001 he cofounded Chip Design Works. His Ph.D. thesis was published as the book *Analog CMOS Filters for Very High Frequencies* (Kluwer, 1993). He holds 11 patents in circuit design.

Dr. Nauta received the Shell Study Tour Award for his Ph.D. work. From 1997 to 1999, he served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING, and in 1998 he served as Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. In 2001, he became an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and he is also a Member of the Technical Program committee of ESSCIRC and ISSCC. He is a corecipient of the IEEE ISSCC 2002 Van Vessem Outstanding Paper Award.