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The development of titanium silicide–boron-doped polysilicon resistive temperature sensors

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Abstract
Thin films of titanium silicide ($TiSi_2$) formed on heavily boron-doped polycrystalline silicon (poly-Si/B^+) were applied for the first time for resistive temperature sensing. The temperature sensors exhibited a high-temperature coefficient of resistance of 3.8×10^{-3} °C^{-1}, a linear dependence of resistance on temperature and an excellent thermal and electrical stability up to 800 °C. This work discusses the fabrication method and the morphological and electrical characterization of the $TiSi_2$/poly-Si thin film resistors throughout the stages of its formation.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Accurate control and measurement of temperature is an essential requirement in various sensor and microfluidic applications. The precise measurement of reaction heats by microcalorimetry is used as a transduction mechanism for the detection of combustible gases, with typical examples [1–4]. Also, high-throughput, sensitive thermal analysis of bio-chemical interactions is an important application and was achieved using microfluidic calorimeters as demonstrated by Lee and co-workers [5]. In microreactors used for production or analysis of (bio-)chemical compounds [6, 7] and in heterogeneous catalysis research [8], good control over the temperature is necessary because of the exponential dependence of reaction rates.

For many of the commonly used resistive materials, e.g., metallic thin films and semiconductors, poor sensitivity and stability at high temperatures and incompatibility with integration on a silicon chip still belong to the major drawbacks. Additionally, microsystems for chemical analysis require materials that are chemically resistant toward the reactive components and the reaction products: on one hand to prolong the life-time of a thermistor and on the other hand to ensure zero blank activity of the device during operation. Moreover, commonly used metal thin-film resistors, when not passivated, can act as a very reactive catalyst, thereby actuating (undesirable) reactions. These drawbacks bring a demand for new emerging materials that meet requirements of technological compatibility and exhibit excellent thermo-electrical properties and stability at high temperatures.

There is a wide range of materials that can be successfully applied in thermistors [9]. From the candidates for high-temperature sensing, we selected $TiSi_2$ on heavily boron (B^+)-doped poly-Si. To the best of our knowledge, this is the first time that the combination of these two materials has been employed for resistive temperature sensing up to 800 °C. Other types of silicides for heating and temperature-sensing purposes are tantalum silicide ($TaSi_2$), cobalt silicide ($CoSi_2$) [10], molybdenum silicide ($MoSi_2$) [11], nickel silicide (NiSi) [12] and platinum silicide (PtSi) [13].

$TiSi_2$ is commonly used in the semiconductor industry to reduce parasitic series resistance and contact resistance between metallization and the device [14–17]. Therefore, it is a promising material for accurate temperature sensing. It has a low resistivity, high-temperature coefficient of resistance (TCR), good thermal, chemical and electrical stability,

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low silicide-to-silicon contact resistance and established compatibility with silicon technology [18, 19].

An objective of this work is to evaluate the feasibility of $TiSi_2$/poly-Si thin films as resistive temperature sensors. We will discuss here the technological aspects of the silicide formation, the integration in a Si-based process and the morphological and electrical characterization. Realized structures exhibited a high TCR and excellent thermo-electrical stability and are, therefore, suitable for integration in temperature-assisted lab-on-a-chip microsystems.

2. Choice of a material for temperature sensing

2.1. Requirements of the sensor material

The material for temperature sensing should satisfy a number of important constraints imposed by the manufacturing technology and the field of potential application:

- linear change of resistance in a wide temperature range;
- high and stable TCR;
- short- and long-term stability of electrical characteristics;
- chemical inertness at elevated temperatures;
- compatibility with established CMOS processing facilities;
- potential applicability in MEMS/NEMS.

Platinum (Pt, TCR = 3.9×10^{-3} °C^{-1}) might be a preferred material for temperature sensing [20, 21]. However, thermistors based on Pt often require non-standard, low-temperature processing which is not compatible with processing on poly-Si. Moreover, during operation above 550 °C, Pt thin films may agglomerate and alter the resistive properties. Pt has poor adhesion to Si, SiO_2 and Si_xN_y and, therefore, an adhesion layer is required. Most of the issues related to Pt reliability are due to the degradation of the Pt adhesion layer at elevated temperatures [22].

Thin films of poly-Si do not require an adhesion layer and a high electrical stability is reported [23]. Highly doped poly-Si can be used for temperature sensing in a limited temperature range and at high dopant concentrations a positive TCR is observed [4]. However, for these high dopant concentrations, the nonlinearity of electrical properties, the relatively low TCR and the potential to resistive drift may limit its application. In addition, above 450–500 °C, effects of grains and grain boundaries movement lead to the deviation of resistance and, therefore, burn-in procedure is required.

In table 1 the thermo-electrical properties of commonly utilized thin silicide films are summarized. NiSi and PtSi do not match the criteria of high-temperature stability. The resistance of $TaSi_2$ changes nonlinearly with temperature, and along with $MoSi_2$ it exhibits lower TCR values compared to other silicides. Based on the above-mentioned design constraints, reported electrical properties and desirable compatibility with standard CMOS processing, $TiSi_2$ or $CoSi_2$ is the best option for temperature sensing.

Table 1. Comparison of thermo-electrical properties of thin silicide films.

Silicide	T_{form} (°C)[a,b]	Resistivity ($\mu\Omega$ cm)[b]	TCR $\times 10^{-3}$ (°C^{-1})[a,c,d,e]	R–T curve[e]	T_{max} on Si (°C)[f]
$TiSi_2$	700–900	13–20	3.8–4.3	Linear	950
$TaSi_2$	650	50–60	1.57–1.75	Nonlinear	1000
$CoSi_2$	600–700	14–20	3.62–4.33	Linear	950
$MoSi_2$	525	100–120	2.58	Linear	1000
NiSi	400–600	14–20	4.3	Linear	850
PtSi	300–600	28–35	–	–	750

[a] [19], [b] [15], [c] [10], [d] [11], [e] [12], [f] [16].

2.2. $TiSi_2$/poly-Si thin films for temperature sensing

We selected $TiSi_2$ on heavily B^+-doped poly-Si as sensor material because, unlike the commonly used Pt and poly-Si thin films, it meets all criteria mentioned above. The $TiSi_2$ was formed by the reaction of Ti with poly-Si during rapid thermal annealing (RTA). Conventional thermal annealing (CTA) is not practical because Ti is prone to oxidation. During the first annealing step at a temperature of 700–750 °C, the metastable C49 $TiSi_2$ phase is formed. In the second annealing step, at a temperature of 850–900 °C, the stable low-resistive C54-$TiSi_2$ phase is obtained. A detailed description on the kinetics of this transformation to the C54 phase can be found elsewhere [24]. The stable low-resistive C54 phase of $TiSi_2$ is the desirable material for sensing applications in this study. It exhibits metallic-like behavior with a resistivity (ρ) in the range of 13–20 $\mu\Omega$ cm and a TCR in the range of $(3–3.6) \times 10^{-3}$ °C^{-1} [25]. In $TiSi_2$/poly-Si thin films the electrical properties are governed by the $TiSi_2$. We concluded this based on the fact that $TiSi_2$ has lower resistance and higher TCR compared to poly-Si. This was also demonstrated experimentally (see figures 6 and 7). This makes the $TiSi_2$/poly-Si system suitable for use in resistive temperature sensing.

By nature, $TiSi_2$ is covered with a layer of native oxide (SiO_2). It can be oxidized further to a thicker SiO_2 layer at the cost of the underlying poly-Si layer. The $TiSi_2$ film itself remains undisturbed.

The sensing material should not initiate any (undesirable) reactions in the system, i.e. stay chemically inert at elevated temperatures, such that only the reactions of interest give a significant signal. $TiSi_2$ is a chemically stable material and reported to resist temporally immersion in a potassium hydroxide (KOH) solution [26]. It can also be used as a masking material for the silicon surface [27] and bulk [28] micro-machining. $TiSi_2$ is formed where Ti is in contact with Si. Therefore, the formation of silicides will only occur on predefined Si-based structures. This is commonly addressed as the self-aligned silicide (SALICIDE) technology [14].

The compatibility with Si technology allows the realization of miniature sensor devices with advanced functionality at reduced costs in Si IC manufacturing facilities. The good thermal stability of $TiSi_2$ up to 800 °C permits high-temperature processing, such as temperature-assisted anodic bonding. This facilitates merging of the silicon-based sensors with MEMS/NEMS technology.

In addition, the $TiSi_2$ has unique light-absorptive properties and, therefore, can be attractive for the lab-on-a-chip devices utilizing optical detection [29].

2.3. The technological aspects of $TiSi_2$ integration

In this section we discuss the issues to be considered during the fabrication and integration of the $TiSi_2$/poly-Si temperature sensors in the Si-based process. The factors that influence the thermo-electrical properties of the formed $TiSi_2$ on poly-Si are given below [30]:

- annealing conditions (ambient gas, temperature and time);
- properties of the poly-Si (grain size distribution and doping level);
- cleanliness of the Ti/poly-Si interface prior to the formation of the $TiSi_2$;
- thickness of the formed $TiSi_2$;
- sensitivity of the grain boundaries to the high-temperature anneals;
- oxidation behavior of the $TiSi_2$/poly-Si stack.

The annealing temperatures are known from the studies in which, by means of the *in situ* four-point-probe measurements, the resistivity and the phase changes from Ti to C49-$TiSi_2$ and further to C54-$TiSi_2$ were monitored during the annealing. From such measurements it is known that the C49–C54 phase change occurs around 850–900 °C.

Commonly, argon (Ar) or nitrogen (N_2) is used as annealing ambient. Annealing in Ar leads to the formation of $TiSi_2$ at the risk of an excessive lateral growth of silicide over the neighboring dielectric. This can cause problems in CMOS applications limited to the nanoscale dimensions of the Si gates. Therefore, to suppress a lateral diffusion of Si into Ti, annealing in N_2 ambient is preferred.

The silicide formation for Ti on Si in N_2 ambient results in the simultaneous formation of TiN and $TiSi_2$ in Si areas, whereas only TiN is formed in the dielectric regions. This prevents the lateral growth of the silicide. The TiN layer can be further etched to release silicide.

The substrate and dopant in the underlying poly-Si have great impact on grain size, resistivity and the thermal stability of the formed silicide layer. This was demonstrated for Co/poly-Si resistive lines by Chen and co-workers [31]. The presence of the dopant also impacts silicide properties. It has been reported that n-type dopant leads to a modification of the grain structure of poly-Si, and that doping of poly-Si with As or P greatly enhances the thermal stability [32].

The surface of the poly-Si should remain particle- and water-free prior to the sputtering of Ti. Besides the formation of a native oxide during CTA (performed for the activation of B in poly-Si), a thicker under stoichiometric boron oxide (B_2O_5) can be formed at the interface of poly-Si/SiO_2. Therefore, a standard oxide etch must be done to ensure an oxide-free surface.

Karlin and co-workers pointed out that the thickness of the $TiSi_2$ plays an important role. They report on the improved thermal stability as the thickness of the $TiSi_2$ was doubled [32]. By applying a thicker Ti layer, a thicker silicide layer can be obtained with the enhanced consumption of the underlying poly-Si. This is reflected in the total resistance of $TiSi_2$/poly-Si stack.

The poly-Si/B^+ combination is known for a lower sensitivity to oxidation, which is an advantage. On the other hand, at high temperatures, atoms of B^+ can inhibit the formation of the $TiSi_2$ due the formation of titanium diboride (TiB_2).

3. Formation and characterization of the $TiSi_2$ thin films

3.1. The silicidation procedure

In this section we discuss the technological aspects of the $TiSi_2$ formation. $TiSi_2$ was formed by a two-step temperature-assisted reaction of sputtered Ti and poly-Si. Prior to the manufacturing of the sensor prototype, the silicidation procedure was tested on two types of substrates:

- Si containing 200 nm of silicon rich nitride (SiRN);
- fused silica (FS) wafers.

The preparation procedure was as follows. Single-crystal, p-type, {1 0 0} oriented one-side-polished Si wafers, 100 mm in diameter, 525 μm thick and with a resistivity of 5–10 Ω cm, were used. Prior to the deposition of 200 nm thick SiRN, the wafers were subjected to standard chemical cleaning with nitric acid and strip of a native oxide. The nitride was grown by low-pressure chemical vapor deposition (LPCVD) at 850 °C using $SiCl_2H_2$ and NH_3 gases. For the electrical characterization of $TiSi_2$ thin films above 250 °C, we used double-side-polished FS wafers (see section 3.3) of Q1 quality with a diameter of 100 mm and a thickness of 525 μm, supplied by SCHOTT AG (Grünenplan, Germany). The Si/SiRN and FS wafers were subjected to a growth of 500 nm of LPCVD poly-Si at 620 °C from SiH_4. Ion implantation of poly-Si was performed to define its sheet resistance (R_{sheet}): B^+ with a dose of 5×10^{15} at cm^{-2} and an activation energy of 80 keV was implanted into the poly-Si. Subsequently, CTA in N_2 at 800 °C for 30 min was done to remove the damage in Si and to activate the B^+. This resulted in a dopant concentration of about 10^{20} B cm^{-3}. The R_{sheet} of poly-Si on Si/SiRN was measured to be ca 220 Ω sq^{-1}. The R_{sheet} of poly-Si on FS was slightly lower compared to Si: ca 190 Ω sq^{-1}.

These B-doped poly-Si films with R_{sheet} values in the range 190–220 Ω sq^{-1} were used as a base layer for the formation of integrated $TiSi_2$/poly-Si resistive temperature sensors and poly-Si heaters. The presence of any n-type (As, P) or p-type (B) dopant in the poly-Si is generally known to slow down the transformation rate to the desirable C54 phase [14]. Considering this fact, the annealing temperatures were selected as 700 °C for the first anneal and 900 °C for the second anneal. The annealing was performed using a Solaris 150 Rapid Thermal Processing System (Surface Science Integration, El Mirage, AZ, USA). The heating and cooling rates were 50 °C s^{-1} and the wafer was kept at a set temperature for 30 s. A flow of the forming gas (95% N_2 / 5% H_2) was used to prevent oxidation. The experiments in pure N_2 were also performed. The resistance of the layers obtained by

Table 2. The annealing conditions in nitrogen and former gas and the measured values of sheet resistance.

	Ramp	Temperature	Duration	Sheet resistance (Ω sq^{-1})	
	($^{\circ}$C s^{-1})	($^{\circ}$C)	(s)	Nitrogen	Forming gas
First anneal	50	700	30	25.38	18.54
Second anneal	50	900	30	11.78	5.75

annealing in N_2 was larger than that of samples annealed in the forming gas (see table 2). This was ascribed to contamination by residual oxygen (O_2). It is recommended to keep the concentration of O_2 in the annealing gas below 10 ppm. In practice, it is difficult to eliminate O_2 completely in an atmospheric system.

Prior to the deposition of the Ti films, wafers were chemically cleaned and dipped for 1 min in 1% hydrofluoric acid solution (HF). A 50 nm thick Ti was deposited at pressure of 0.066 mbar, in 148 sccm Ar flow and power of 200 W using a home-built dc magnetron sputtering system. A pre-sputtering run for 20 min was performed to clean the Ti target before the actual deposition. The thickness of the Ti films was measured by a profilometer Veeco Dektak 8 (Veeco, Plainview, NY, USA). The measurements indicated a centersymmetric non-uniformity: a thicker film in the center and decreasing with ca 10% toward the edges of the wafer. The non-uniformity of the Ti thickness should be taken into account during the fabrication because the thickness of the formed silicide layer and the phase formation rate are dependent on it. The surface roughness (Ra) of the Ti thin film was 1.81 nm as measured using Veeco Dektak 8.

After the deposition of Ti, wafers were placed in the RTA system. After flushing with forming gas, the first anneal was performed. A typical RTA run in the forming gas consisted of a temperature ramp of 50 $^{\circ}$C s^{-1} up to 700 $^{\circ}$C , hold for 30 s, and cooling at 50 $^{\circ}$C s^{-1} rate down to room temperature. In figure 1, we schematically illustrate the uptake of the poly-Si and formation of the $TiSi_2$ and TiN. The formation of $TiSi_2$ proceeded by the consumption of the underlying poly-Si. The part of the Ti was consumed by the gas-phase nitridation to titanium nitride (TiN). High-resolution scanning electron microscopy (HRSEM) analysis revealed that during the reaction 60–70 nm of the poly-Si was consumed for the formation of about 25 nm of $TiSi_2$. The cross-sectional SEM images of the $TiSi_2$/poly-Si stack are presented in figure 2. The formation of the meta-stable C49 phase, the TiN and the stable C54 phase was confirmed by the 4-point-probe resistance measurements.

During the first anneal, Ti reacts with poly-Si to form $TiSi_2$ and TiN. However, Ti may also react with the SiO_2 resulting in a metal-rich Ti_3Si_5 silicide compound. The unreacted Ti, the formed TiN as well as the Ti_3Si_5 were etched for 10 min in a solution of hydrogen peroxide (H_2O_2), ammonia and water (1:1:1). During the etching a color change was observed: from light-gold of TiN to grayish of $TiSi_2$. After

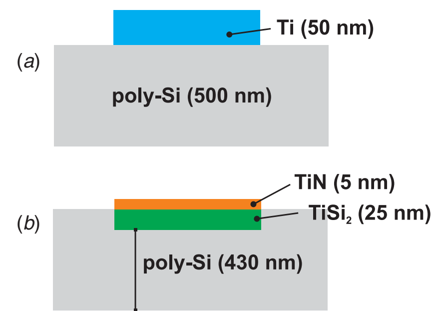

Figure 1. Schematic representation for the poly-Si uptake due to the silicidation process.

stripping of TiN the second anneal was performed at 900 $^{\circ}$C. The 4-point-probe measurements indicated a resistance drop from 46 $\mu\Omega$ cm, for the C49 meta-stable phase, to 14 $\mu\Omega$ cm for the stable C54 phase of $TiSi_2$. The R_{sheet} resistance values are listed in table 2 and correspond to 25 nm $TiSi_2$ on 430 nm poly-Si. The silicide with R_{sheet} of the order of 5–6 Ω sq^{-1} for C54-$TiSi_2$ was used further for integration in the fabrication process. This was a sufficiently low resistance for our thermistor application. Additionally, it is recommended to realize the whole silicidation procedure in the shortest possible time frame. In particular, the first anneal after the Ti deposition and the etching of TiN.

In further sections, the structural and electrical analysis of the $TiSi_2$ thin films are discussed.

3.2. Morphological characterization of the $TiSi_2$/poly-Si thin films

Cross-sectional high-resolution transmission electron microscopy (HRTEM) images were taken using a Philips CM300ST-FEG TEM system (Philips, Eindhoven, the Netherlands). All HRTEM images were recorded at an acceleration voltage of 300 kV without an objective aperture. Two samples were analyzed following these fabrication steps:

- after the anneal at 700 $^{\circ}$C and before strip of TiN;
- after the anneal at 900 $^{\circ}$C.

The aim of the TEM analysis was to measure the thickness of the formed $TiSi_2$ and TiN. Using fast Fourier transform (FFT) we were able to measure the spacings of the atomic planes. During the measurements internal calibration was performed for the (1 1 1) plane of poly-Si on both samples to identify an off-set correction factor. The off-set was estimated to be ca 0.04 Å.

In order to determine the crystalline orientation of the $TiSi_2$, x-ray diffractograms (XRD) were taken using a Philips XRD model Expert System (Panalytical, Almelo, the Netherlands). High-angle measurements were performed in the 2Θ-range from 20° to 60°. Four samples from the same wafer were analyzed:

(a) Si/SiRN/poly-Si/Ti directly after the Ti sputtering and prior to any annealing;
(b) Si/SiRN/poly-Si/TiSi (C49)/TiN after the 700 $^{\circ}$C anneal and prior to the TiN etch;

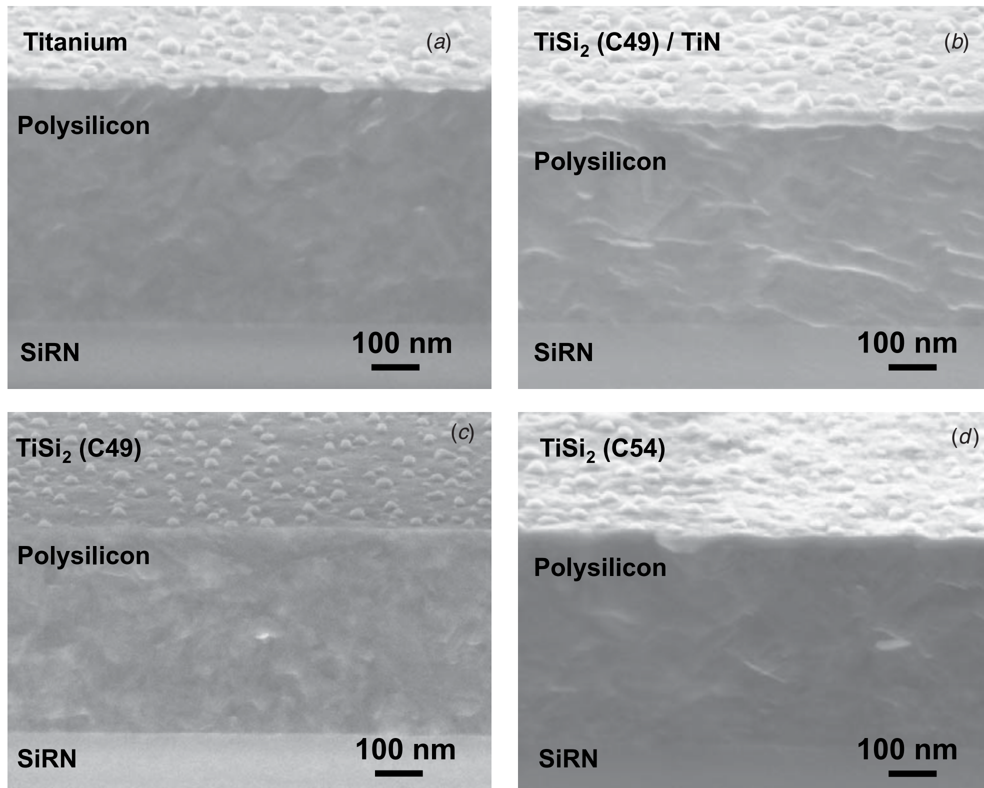

Figure 2. HRSEM cross-sectional view of the Si/SiRN/poly-Si/$TiSi_2$ stack after deposition of Ti and before the first anneal (*a*), after the first anneal at 700 °C before (*b*) and after (*c*) the etching of the TiN and unreacted Ti and after the second anneal at 900 °C (*d*).

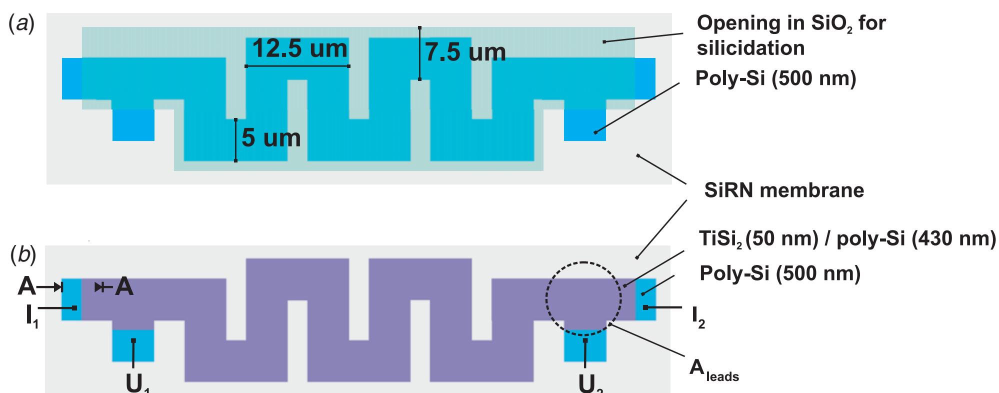

Figure 3. The $TiSi_2$/poly-Si resistor outlook showing dimensions of resistor, an opening in the SiO_2 layer which was exposed to Ti (*a*) and an area of the poly-Si resistor converted to silicide (*b*).

(c) Si/SiRN/poly-Si/TiSi (C49) after the 700 °C anneal and strip of the TiN;
(d) Si/SiRN/poly-Si/TiSi (C54) after the 900 °C anneal.

X-ray photoelectron spectroscopy (XPS) surveys were performed on two $TiSi_2$ samples using a Quantera SXM scanning XPS microprobe (Physical Electronics, Inc., Chanhassen, MN, USA). The first sample was $TiSi_2$ as formed. The second sample was from the same wafer subjected to deposition of 50 nm oxide by plasma enhanced chemical vapor deposition (PECVD) at 300 °C. The XPS analyses were performed to identify the content of Ti and Si in the $TiSi_2$ layer, to verify the presence of any contamination (such as O and N) and to study the influence of the PECVD SiO_2 on $TiSi_2$. Element spectra scans were taken during depth profiling. The composition of the $TiSi_2$ layer was measured at a given point at a depth of 10 nm. The times are 3 min and 8 min 30 s for pure $TiSi_2$ and SiO_2-capped sample, respectively.

Atomic force microscopy (AFM) in a tapping mode was used to measure the roughness and estimate surface morphology before and after the silicidation.

3.3. Electrical characterization of the $TiSi_2$/poly-Si thin films

The TCR and the stability of the poly-Si and $TiSi_2$/poly-Si thin films were studied from 25 to 800 °C. The measurement setup was equipped with four probes at a fixed position

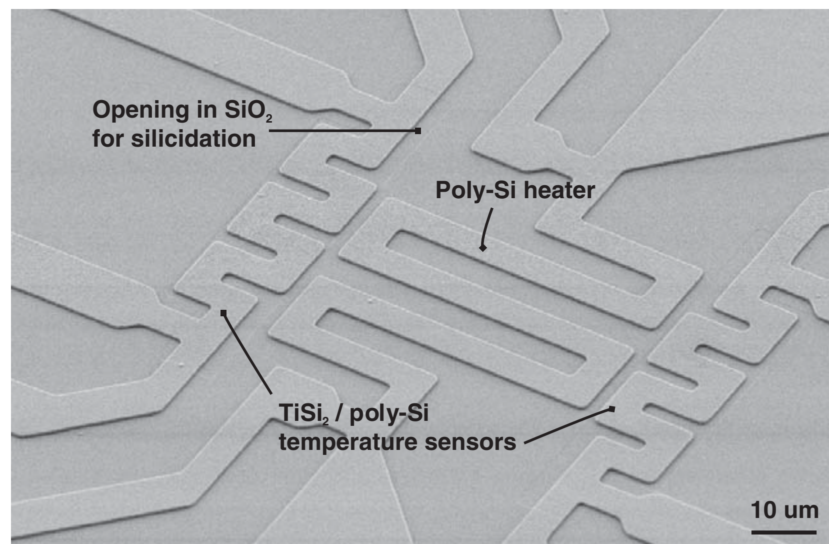

Figure 4. HRSEM top-view image of the sensor device.

(16 × 16 mm). A heating element and an aluminum nitride substrate holder allowed temperature ramps up to 800 °C were used for *in situ* electrical characterization of $TiSi_2$/poly-Si. The substrate was mounted with a silver thermal paste on the holder to ensure a good thermal contact. The temperature was regulated via a thermo-couple mounted under the sample. Measurements were performed in vacuum.

The measurements on the Si substrate were valid in the lower temperature range, i.e. from room temperature to 200–250 °C. Above 250 °C, the SiRN-film loses its isolating properties and may provide a short circuit to the intrinsic Si substrate. This effect was investigated by Tiggelaar *et al* [33]. The FS substrate was used for measurements up to 800 °C.

The FS substrates were used to permit the high-temperature resistance measurements on the thin films. The temperature was ramped between 50 and, subsequently, 200, 400, 600 and 800 °C. After each annealing step, sufficient time was given to stabilize the temperature at 50 °C again. This allowed us to extract the TCR and to test the presence of any electrical degradation (hysteresis). A stability test was performed on thin films that were already exposed to 800 °C. During this measurement the temperature was ramped between 200 and 500 °C and stabilized after each heating ramp at 200 °C. The wafer was kept for 5 min at 500 °C during each cycle. The resistance was monitored *in situ* to observe the change in resistance.

4. Fabrication of the $TiSi_2$/poly-Si resistive temperature sensors and the poly-Si heaters

4.1. Design overview

The design of the $TiSi_2$ resistive structures used in this study is shown in figure 3. A meander-shaped $TiSi_2$/poly-Si thermistor consisted of about 430 nm thick poly-Si and 50 nm thick $TiSi_2$. The width (5 μm) and length (100 μm) were selected to form a resistor of about 100–150 Ω. The resistor had poly-Si/aluminum (Al) leads for an electrical readout in the four-points-probe configuration to eliminate parasitic resistances during the measurements. The area where poly-Si leads were connected to the resistor was also subjected to the silicidation process. This eliminated possible failures in measurements associated with a high contact resistance or (and) a temperature gradient between the active part of the resistor and the connections to the leads. The 11.4 kΩ poly-Si resistor used for heating was 5 μm wide and 230 μm long. In these wide $TiSi_2$/poly-Si lines no dimensional limitation was expected. Dimensional limitation is characteristic for nanoscale designs, where the width of the silicide line is comparable to the size of the silicide grains. An overview of the heater and temperature sensors is shown in figure 4.

4.2. Fabrication process flow

The main steps of the fabrication procedure are schematically demonstrated in figure 5. On a {1 0 0} oriented Si wafer, we deposited 200 nm of LPCVD SiRN and 500 nm of LPCVD poly-Si. The resistance of the poly-Si was defined using ion implantation as discussed before. The resulted sheet resistance was ca 190–220 Ω sq^{-1}. The patterning of the poly-Si into resistive structures was achieved by RIE in SF_6, CHF_3 and O_2 plasma with an Olin-17 photoresist mask. The structures were covered by a 50 nm PECVD SiO_2 oxide. The thin oxide film served as an electrical isolator for the poly-Si heaters and as a protection to the poly-Si areas not used for the formation of the $TiSi_2$. Before the silicide formation, the openings in the oxide were defined by standard lithography with the Olin-17 photoresist (as shown in figure 3). The 50 nm Ti film was deposited by dc magnetron sputtering at a base pressure of 2×10^{-7} mbar. It is important to keep the background pressure below 1×10^{-6} mbar to ensure oxygen-free metal deposition. This was followed by a 700 °C anneal step in forming gas and selective etching of the TiN. After the strip of TiN, a 900 °C anneal in forming gas was carried out. At this stage the poly-Si and $TiSi_2$/poly-Si resistive structures were realized. The $TiSi_2$/poly-Si temperature sensing structures were formed by

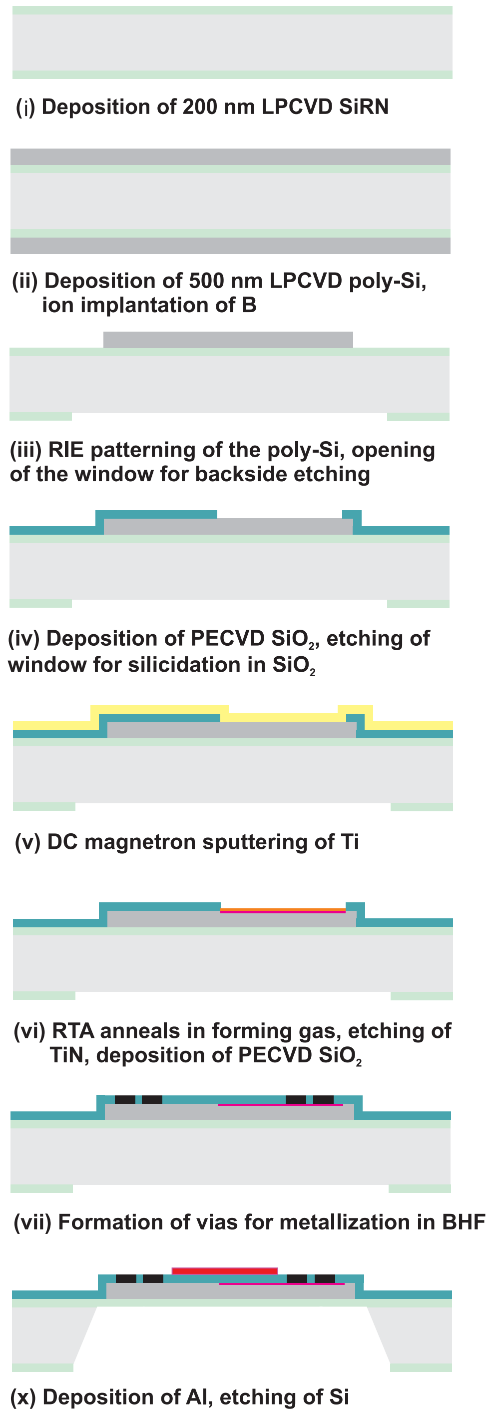

Figure 5. The fabrication process flow for the suspended-membrane $TiSi_2$/poly-Si resistive temperature sensors.

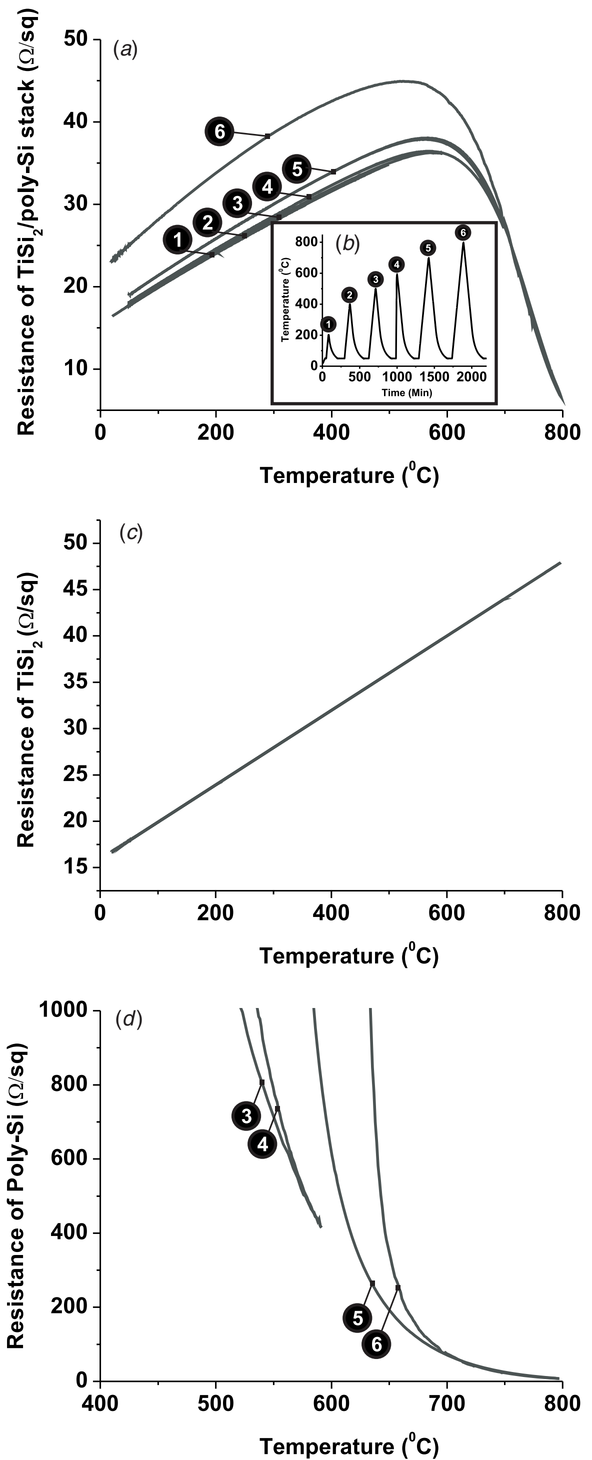

Figure 6. Contribution of poly-Si and $TiSi_2$ to the total resistance of $TiSi_2$/poly-Si stack on the Si/SiRN substrate: (*a*) measured temperature dependence of $TiSi_2$/poly-Si stack under the temperature ramps applied in time (*b*); derived temperature dependence of resistance of the $TiSi_2$ layer (*c*), indicating linear TCR and no hysteresis; derived temperature dependence of resistance of the poly-Si layer (*d*), indicating contribution of poly-Si and intrinsic Si substrate at temperatures above 450 °C.

the silicidation reaction between Ti and the patterned poly-Si. This is a self-aligned process, i.e. the silicidation will take place only in the poly-Si area which was in a direct contact with Ti. This manufacturing approach allowed the formation of the highly resistive poly-Si heaters and the $TiSi_2$/poly-Si temperature sensors within one layer. The technological details of the silicidation process were discussed in section 3.1.

Next, the structures were covered with another 50 nm PECVD SiO_2. Standard lithography with the Olin-17 was used to define the openings in the SiO_2 layer. The contact holes were etched using a buffered hydrofluoric acid (BHF) etching solution. A 400 nm of Al was sputtered and patterned

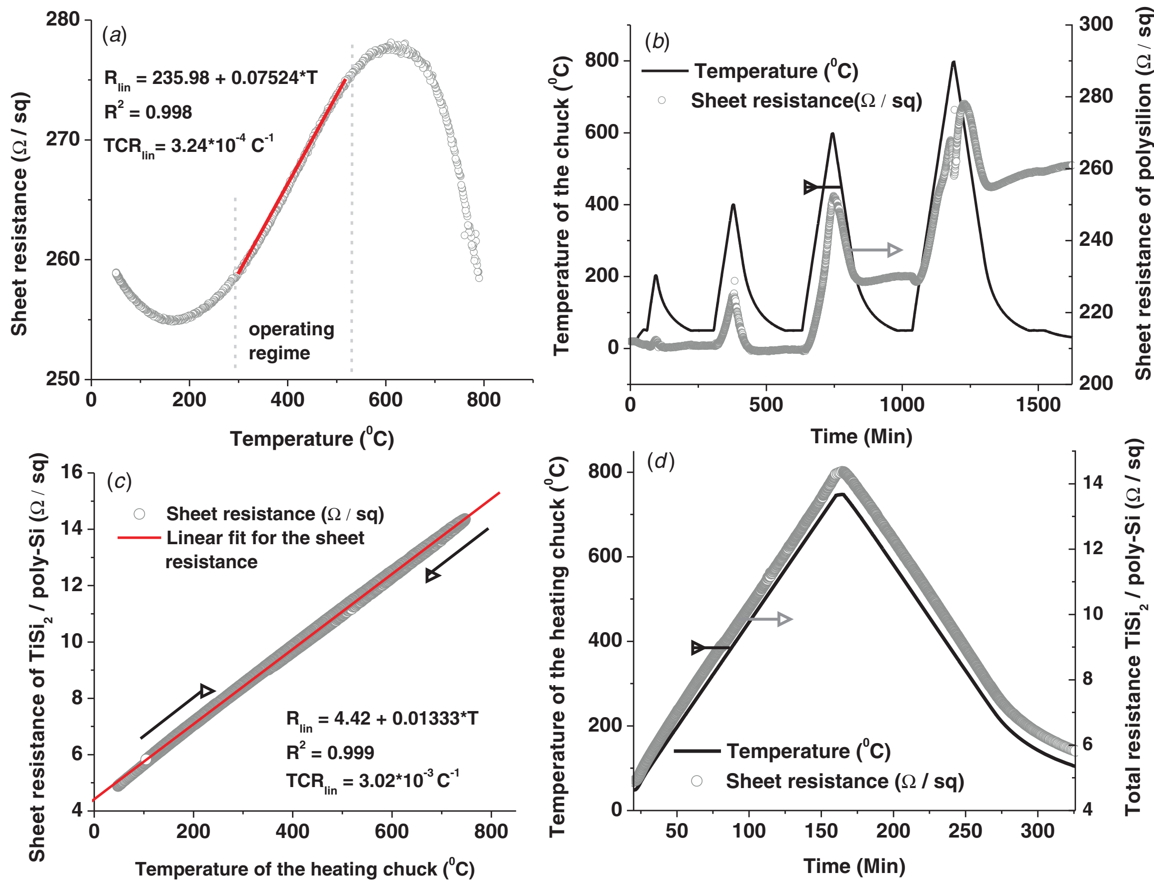

Figure 7. The temperature dependence of the sheet resistance (*a*), (*c*) and the stability test (*b*), (*d*) for 500 nm poly-Si/B+ and $TiSi_2$/poly-Si, respectively. Figures 7(*a*) and (*b*) reproduced with permission from [4]. Copyright 2011 Elsevier.

with standard Al wet etchant (MERCK 115435.200). Next, the structures were annealed in N_2 at 450 °C for 20 min to form a stable ohmic contact to resistive structures. Thermal insulation was realized by bulk micromachining of Si, i.e. anisotropic wet etching in 25% KOH with SiRN as the etch-stop layer. During the Si etching, the front side of the wafer containing the functional structures was protected in a stainless steal holder.

5. Results and discussion

5.1. Thermo-electrical properties of the $TiSi_2$/poly-Si thin films

Figure 6 shows the dependence of the sheet resistance on temperature for the $TiSi_2$/poly-Si stack formed on the Si/SiRN substrate. The contribution of the $TiSi_2$ and the poly-Si sheet resistance to the total resistance of parallel $TiSi_2$/poly-Si stack is shown. Due to the conductive properties of the SiRN above 250 °C, the intrinsic substrate contributed to the measured resistance (the negative TCR above 500 °C was due to the Si substrate). To avoid this effect, the thermo-electrical properties of the $TiSi_2$/poly-Si stack were also analyzed extensively on the FS substrates.

In figure 7, we present the temperature dependence of resistance for a system of parallel resistances $TiSi_2$/poly-Si on the FS as a function of temperature (*c*) and time (*d*). We found a linear temperature dependence of resistance. TCR values were between $(3.01–3.15) \times 10^{-3}$ °C^{-1}. No hysteresis was observed during the temperature ramps. A stability test was performed by several temperature cycles between 200 and 500 °C. The test indicated no degradation of material due to thermal or electrical stress (see figure 8). The results of poly-Si/B+ measured with the equal conditions on FS (see

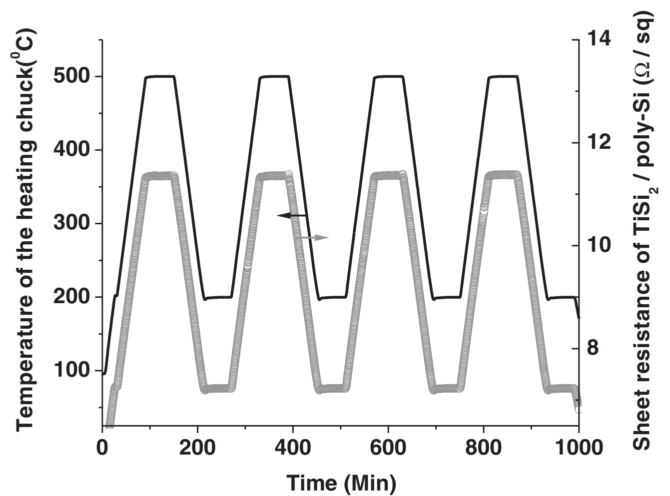

Figure 8. The thermo-electric stability test of $TiSi_2$/poly-Si performed by ramping temperature between 200 and 500 °C.

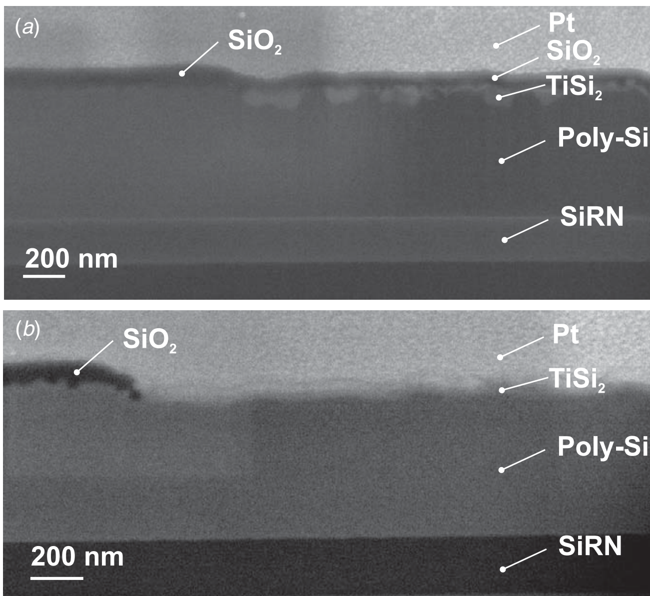

Figure 9. FIB/SEM cross-sectional images acquired at the edge of the $TiSi_2$/poly-Si resistor showing formation of the non-uniform $TiSi_2$ thin film, improved thin film thickness uniformity as the Ti thickness was doubled (*b*).

figures 7(*a*) and (*b*)) show that poly-Si itself exhibited a much lower TCR (extrapolated for the linear part for about 2.5×10^{-4} °C^{-1}) and its resistance depends nonlinearly on temperature. In practice, the poly-Si-based integrated thermistors have to be stabilized by high current densities or high temperature ramps. The addition of the $TiSi_2$ clearly improved the thermo-electrical characteristics in this respect.

We tested the influence of the passivation layer on the resistive properties of poly-Si and subsequent formation of $TiSi_2$. The goal of this test was to identify whether any redistribution of dopant or other processes occurred during the deposition of high temperature (TEOS) and low temperature (PECVD) oxides which may cause alteration of the resistance of the poly-Si or formed silicide. The $TiSi_2$ layer was formed on three samples:

- poly-Si without passivation;
- poly-Si with 50 nm TEOS oxide deposited at 800 °C;
- poly-Si with 50 nm PECVD oxide deposited at 300 °C.

Table 3. The sheet resistance of poly-Si/$TiSi_2$ after the oxide deposition at 800 °C (TEOS) and 300 °C (PECVD) compared to poly-Si without the oxide layer.

	Sheet resistance (Ω sq^{-1})	
	First anneal	Second anneal
No passivation	16.31–17.4	4.532–7.89
TEOS	20.4–21.3	7.16–7.43
PECVD	17.54–20.94	7.07–9

The TEOS and PECVD oxides were removed from poly-Si surface prior to deposition of Ti in the BHF solution. In table 3 a summary of the measured sheet resistances after first and second annealing steps is presented. The obtained resistances were in the same range for both annealing steps. Based on the results we conclude that the deviation in the resistance for the patterned structures was not caused by the passivation layer. Four-point-probe measurement confirmed that SiO_2 as the passivation layer did not alter resistive properties of poly-Si and, subsequently formed, poly-Si/$TiSi_2$.

In figure 9(*a*), the SEM/FIB cross-sectional image indicated a non-uniform silicide formation for the initial thickness of 50 nm Ti. This non-uniformity can be addressed to the presence of native oxide on the poly-Si, enhanced silicide formation at the grain boundaries or nucleation limited growth. For the $TiSi_2$/poly-Si resistors formed from 50 nm Ti a much higher resistance than the desired value (100–150 Ω) was measured. To improve the uniformity and resistance, a 100 nm thick Ti film was used. As a result an improved uniformity of the $TiSi_2$ thin film (figure 9(*b*)) and the desired resistance value was achieved.

5.2. *Morphological properties of the $TiSi_2$/poly-Si thin films*

TEM analysis of $TiSi_2$ after 700 and 900 °C anneal revealed that both samples have well-defined crystalline orientations. The TEM image of the sample after 700 °C (figure 10) shows the formation of about 25 nm of $TiSi_2$ and 5 nm of TiN. From *in situ* FFT analysis a diffraction pattern was obtained and indicated a lattice spacing of 2.38 ± 0.05 Å for TiN.

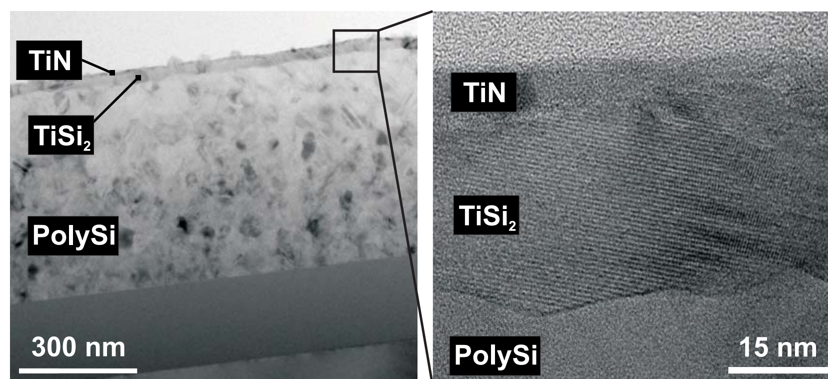

Figure 10. Cross-sectional TEM view on the substrate after first annealing at 700 °C showing the interface between the TiN, the C49-$TiSi_2$ phase and the poly-Si.

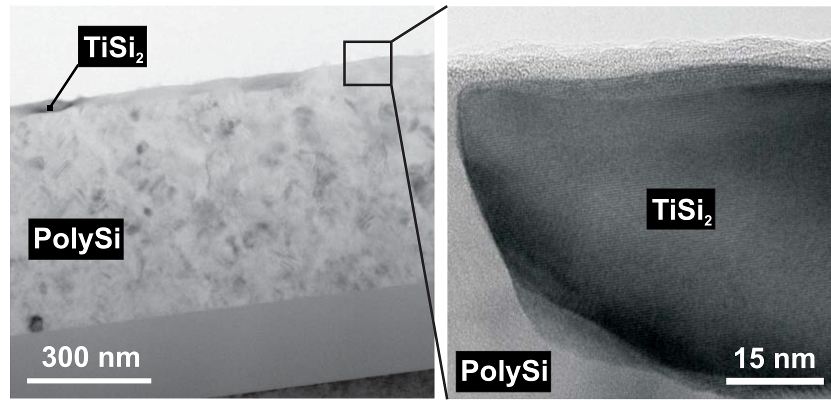

Figure 11. Cross-sectional TEM view on the substrate after second annealing at 900 °C and stripping of the TiN and unreacted Ti, indicating the interface between the C54 phase and the poly-Si.

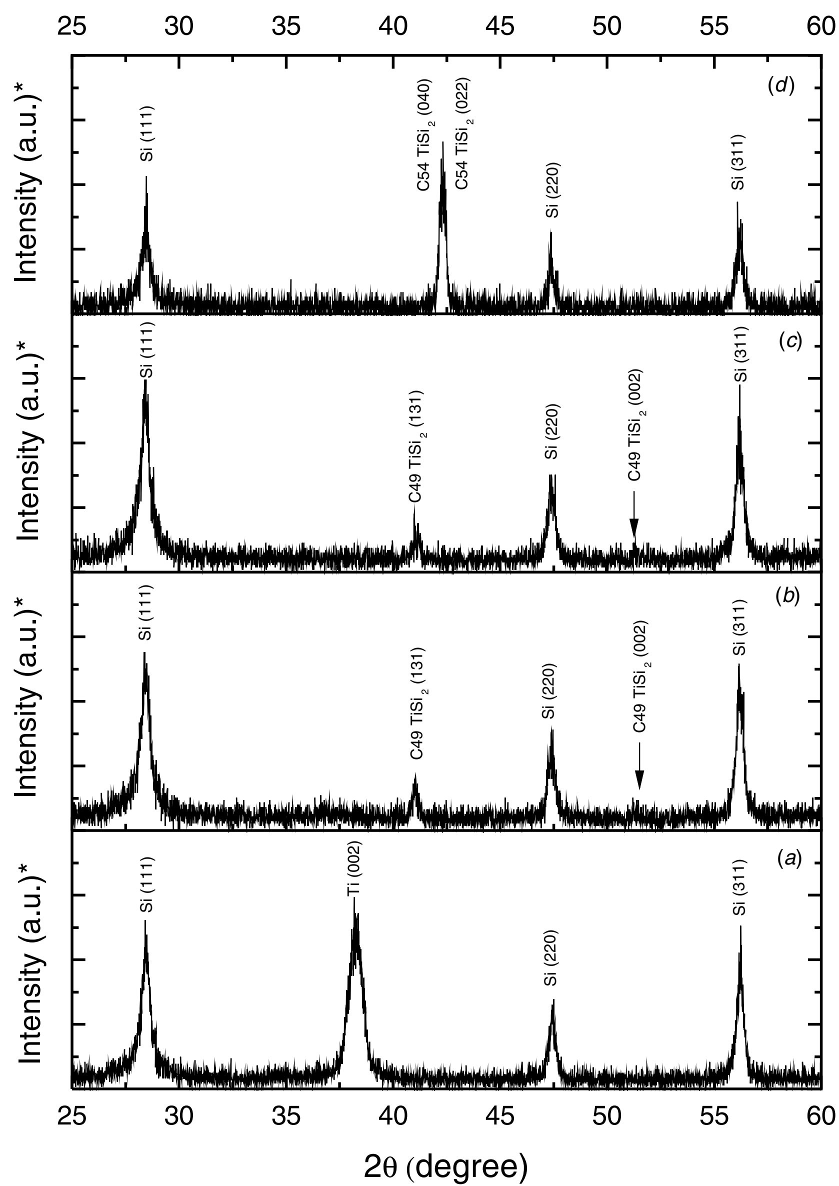

Figure 12. The XRD taken on each stage of the production of the $TiSi_2$: (*a*) sputtering of Ti on the poly-Si, first anneal 700 °C before (*b*) and after (*c*) the TiN etch, (*d*) after the second anneal at 900 °C.

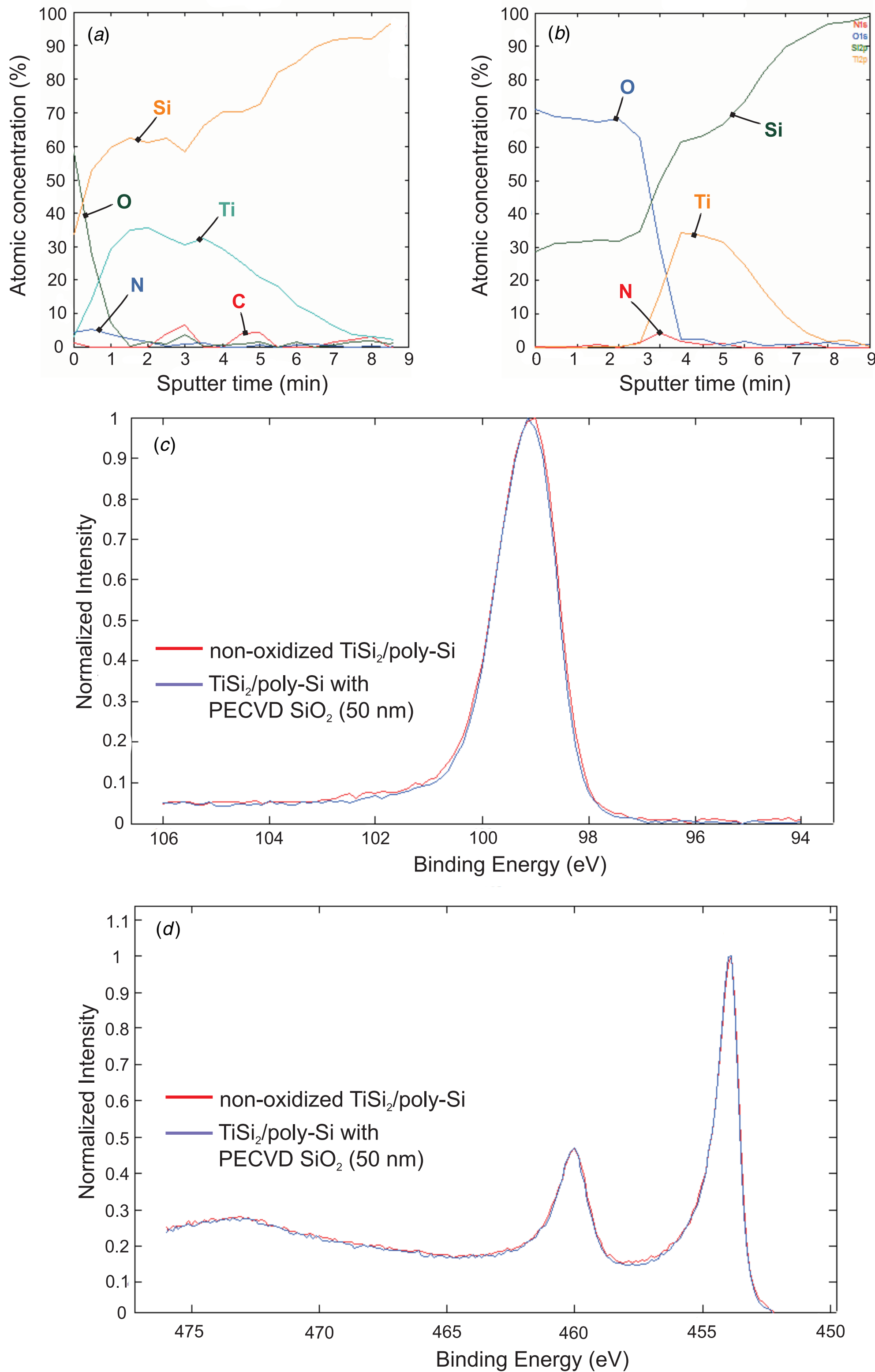

Figure 13. XPS analysis showing the atomic concentration of the elements as a function of sputter time for non-oxidized (*a*) and PECVD oxidized (*b*) $TiSi_2$/poly-Si samples, and the binding energies for Si (*c*) and Ti (*d*). The relative peak height and the shape show that the binding energies of the Si, Ti atoms are similar.

This spacing corresponded to the (1 1 1) orientation [34]. The lattice spacing of 2.17 ± 0.05 Å corresponded to the (1 2 1) orientation [35]. A larger lattice spacing of 6.66 ± 0.05 Å was also observed for the $TiSi_2$ layer, but has not been identified.

TEM images collected from the $TiSi_2$ after 900 °C (figure 11) show an increase of the silicide thickness up to 50 nm. From the FFT obtained from a diffraction pattern the experimental values for d-spacings were found: in the

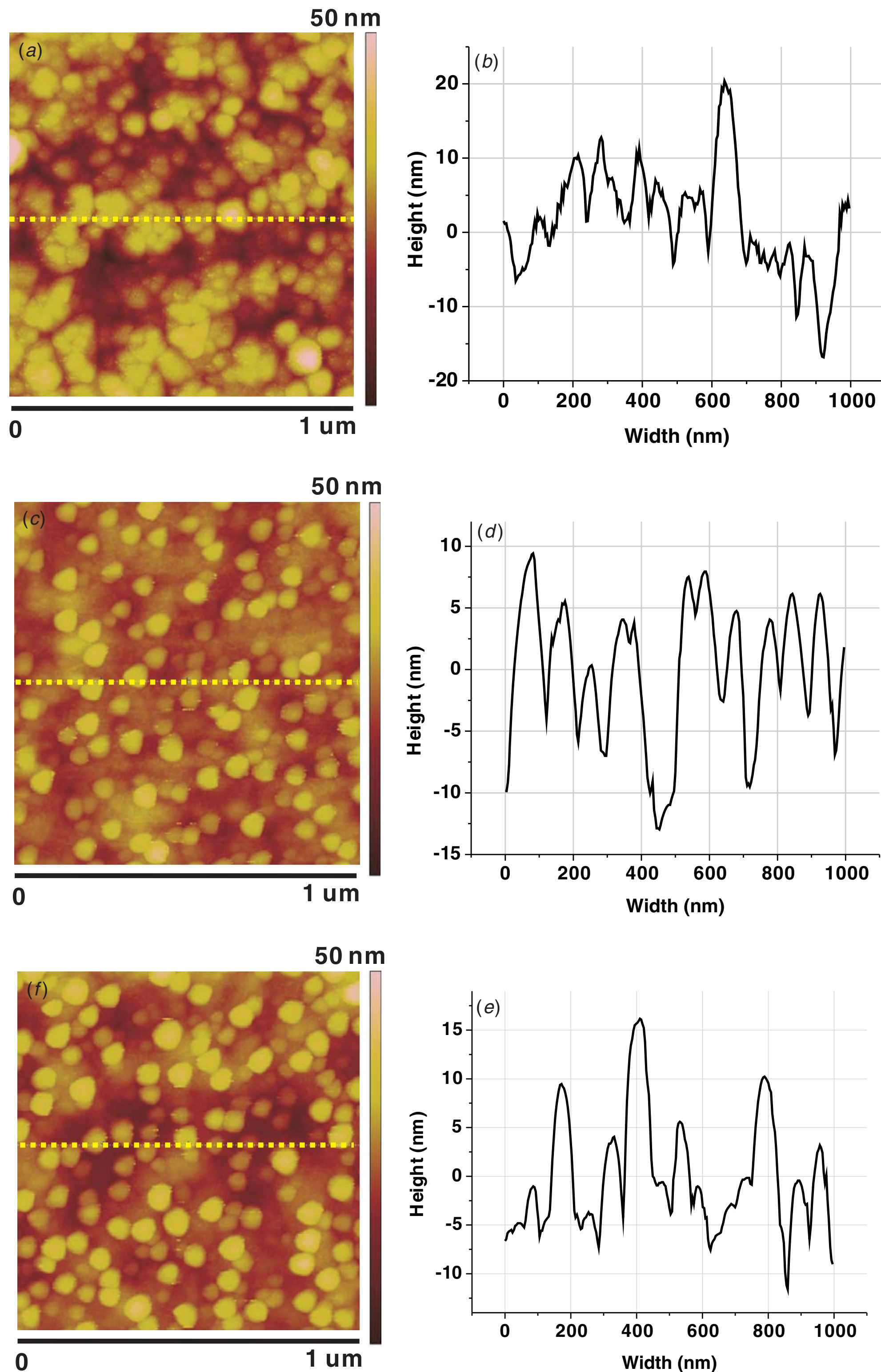

Figure 14. AFM images showing the morphology of the poly-Si thin film prior to silicidation (*a*), (*b*), $TiSi_2$/poly-Si thin films after the first anneal at 700 °C (*c*), (*d*) and the second anneal at 900 °C (*f*), (*e*).

growth direction normal to the film surface 4.23 ± 0.04 Å and parallel to the film surface 2.29 ± 0.03 Å. The obtained lattice spacings, though not corresponding to available database values, show good agreement with the findings of Kittle *et al* in [36]. Kittle discusses the effect of molybdenum impurities on the formation of titanium silicide, and reports lattice spacings of 2.27 Å and 4.15–4.3 Å for the C54 phase of silicide of unidentified orientation (the phase was not present in samples without Mo).

It should be mentioned that XRD had a limited applicability in this study due to the fact that the $TiSi_2$ thin films that were investigated were between 25 and 60 nm

thick and data available in the literature are based on powder samples. However, comparison to diffractograms obtained in other studies was still relevant. In figure 12 XRD taken on every step of the $TiSi_2$ formation are presented. All four samples show peaks of (1 1 1), (2 2 0), (3 1 1) attributed to the poly-Si layer. In graph (a) the peak appearing at 38.87° represented a thin film of Ti with orientation (0 0 2). After the first annealing the two peaks at 41° and 51° were attributed to the (1 3 1) [25] and (0 0 2) [36] orientations of the C49-$TiSi_2$ phase, respectively. Etching of TiN did not result in phase changes as can be seen in the XRD (figure 12(*b*) and (*c*)). After the second anneal, a strong peak at 42.33° was observed and attributed to the (0 2 2) [25] orientation of the C54 phase or the (0 0 4) orientation.

Two samples were investigated by XPS (see section 3.2). The results are presented in figure 13. The elemental scan during depth profiling of the sample without the PECVD SiO_2 indicated some carbon contamination at the surface and an unknown amount of nitrogen. In the $TiSi_2$ film only Ti and Si were found. The interface of the $TiSi_2$ and poly-Si was found to be quite wide. This was caused by the roughness of the sample which was also revealed by the AFM study. The surface of the oxidized sample showed almost no C contamination. The spectra for Ti and Si at the optimum depth for the two samples are almost identical. Thus, the bonds in the $TiSi_2$ compound were identical. Nitrogen contamination was present in both samples. The concentration of nitrogen was higher in the oxidized sample. To conclude, the PECVD SiO_2 layer did not alter structural properties of the formed $TiSi_2$ layer and can be applied as a passivation.

Using AFM, the roughness of the produced silicide thin films was studied and compared to the initial poly-Si layer (see figure 14). The formed $TiSi_2$ layer showed a good homogeneity. A minor difference in morphology was observed between the samples representing $TiSi_2$ surface after 700 and 900 °C anneals. Small, rough, hemispherical structures were observed. The diameter of these structures varied from 40 to 50 nm.

5.3. The TCR of the $TiSi_2$/poly-Si resistors

The 4-probe electrical characterization of the $TiSi_2$/poly-Si resistors was performed in the temperature range from 20 to 185 °C using a Cascade Microtech Low Leakage Manual Probe Station (Cascade Microtech Inc., Beaverton, OR, USA) and a Keithley 4200 Semiconductor Characterization System (Keithley Instruments Inc., Cleveland, OH, USA). Dual current sweep measurements were performed from 0 to 100 μA. Resistive values were derived by averaging forward and back sweep values.

The TCR of the $TiSi_2$/poly-Si resistors was measured before and after the release of the membrane. The typical temperature behavior is presented in figure 15. For different resistors the TCR was found to be in the range (3.6–4) $\times$ 10^{-3} °C^{-1} and was not influenced by the release of the Si from the backside. For comparison, the TCR of Pt is 3.92 $\times$ 10^{-3} °C^{-1}.

The TCR value for the resistors was higher than observed previously for the flat, non-patterned $TiSi_2$/poly-Si thin films.

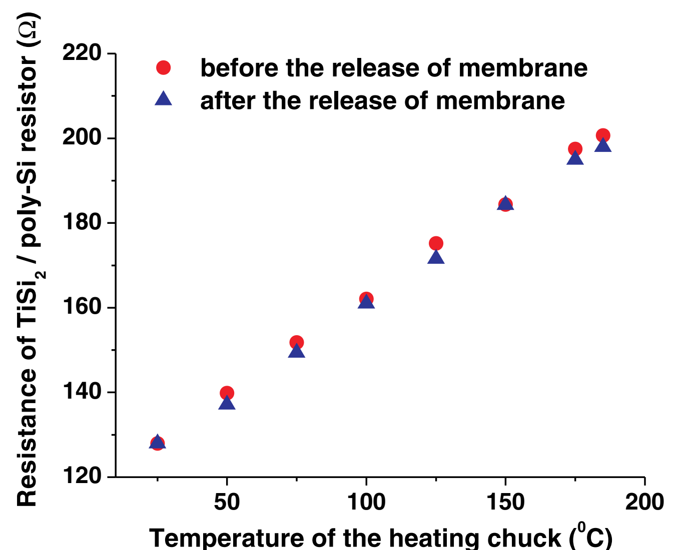

Figure 15. The TCR of a typical resistor derived for the range from 25 to 185 °C before and after the release of the membrane with the linear fit $R_{\text{lin}} = 117 + 0.45 \times \text{T}$ and TCR = 3.85 $\times 10^{-3}$ °C^{-1} and $R_{\text{lin}} = 115.87 + 0.45 \times \text{T}$ and TCR = 3.883 $\times 10^{-3}$ °C^{-1} , respectively. Voltages below 50 mV were used for calibration and TCR measurements to prevent the self-heating effect.

This is attributed to the different thicknesses of the $TiSi_2$ (60 nm) /poly-Si (430 nm) resistor stack. It is worth studying the influence of the thickness of $TiSi_2$ on the TCR values.

6. Conclusions

Thin films of titanium silicide ($TiSi_2$) formed on heavily boron-doped polycrystalline silicon (poly-Si/B^+) were applied for resistive temperature sensing. The TCR and the thermal stability were tested on $TiSi_2$/poly-Si thin films on the Si and FS substrate and on $TiSi_2$/poly-Si resistors suspended on a SiRN membrane. The TCR for flat, non-patterned layers were found to be (2.9–3.1) $\times$ 10^{-3} °C^{-1} in the range of temperatures from 20 to 800 °C. The TCR of suspended $TiSi_2$/poly-Si resistors was measured (3.6–4) $\times$ 10^{-3} °C^{-1} from 20 to 185 °C.

To the best of our knowledge, this is the first time that the combination $TiSi_2$/poly-Si has been used for temperature sensing purposes. In this contribution we provided the details for the design and realization of such $TiSi_2$/poly-Si temperature sensors. The fabrication process is suitable for integration into silicon-based lab-on-a-chip devices.

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