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Fabrication of Transistors on Flexible Substrates: from Mass-Printing to High-Resolution Alternative Lithography Strategies

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In this report, the development of conventional, mass-printing strategies into high-resolution, alternative patterning techniques is reviewed with the focus on large-area patterning of flexible thin-film transistors (TFTs) for display applications. In the first part, conventional and digital printing techniques are introduced and categorized as far as their development is relevant for this application area. The limitations of conventional printing guides the reader to the second part of the progress report: alternative-lithographic patterning on low-cost flexible foils for the fabrication of flexible TFTs. Soft and nanoimprint lithography-based patterning techniques and their limitations are surveyed with respect to patterning on low-cost flexible foils. These show a shift from fabricating simple microlense structures to more complicated, high-resolution electronic devices. The development of alternative, low-temperature processable materials and the introduction of high-resolution patterning strategies will lead to the low-cost, self-aligned fabrication of flexible displays and solar cells from cheaper but better performing organic materials.

1. Introduction

With the invention of the first European movable type printing around 1440 by the goldsmith Johannes Gensfleisch zum Gutenberg, economical and multiple production of alphabet communication became feasible.[1] Knowledge spread rapidly and literacy increased as a result of typography. One of the first books widely spread across Europe was the Gutenberg Bible around 1450. Today, practically all movable type printing ultimately derives from Gutenberg's movable type printing, which is often regarded as the most important invention of the second millennium. Four conventional mass-printing techniques exist, named after the type of master used for printing: relief printing (flexographic), intaglio printing (gravure), planographic printing (offset), and print through (screen printing).[2] All four printing techniques are introduced here, and their relevance for the fabrication of flexible printed electronics with the focus on TFTs for flexible display applications is discussed.

The conventional mass-printing techniques apply pressure to the substrate during ink transfer. In digital printing forms such as inkjet and aerosol jet, ink is dropped from a nozzle onto the substrate according to a digital image. Thereby, no pressure is applied to the substrate, which makes them thus non-impact techniques. Thin layers of a donor material can also be transferred to a substrate with a laser, in a process called laser-induced forward transfer (LIFT).[3] With a laser, material can also be selectively ablated from a substrate, representing a subtractive patterning technique. From the digital printing forms, only the more often in flexible electronics manufacturing applied inkjet printing and LIFT will be discussed in this report.

The absence of a printing master makes digital printing more customizable and results in less waste with respect to chemicals and the target material. Utilization of a digital master has the considerable advantage of reduced cost, as the cost and complexity of producing a master range from relatively low cost in the case of screen printing to medium cost for flexographic printing and very high cost for gravure printing.[4]

The area of printing continued to develop and expand from printed text on paper to printed electronics on materials such as textiles and polymeric foils. Semiconductor research and the invention of the point-contact transistor at Bell laboratories in 1947[5] by Bardeen, Brattain and Shockley was followed up by the invention of the first silicon transistor[6] by Texas Instruments in 1954 and the first metal-oxide-semiconductor field-effect transistor (MOSFET)[7] in 1960 again at Bell labs, paving the way to practically all modern electronics. The worlds ever demanding decrease of feature sizes for the fabrication of more densely packed, faster electronic circuits and devices has been described by Gordon Moore in 1965.[8] His law predicts the doubling of the number of transistors that can be placed inexpensively on an integrated circuit approximately every two years. Research and development of tools, allowing reproducible patterning at an ever decreasing scale, are in the focus of the semiconductor manufacturers. Fabrication costs

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and addition of device functionalities follow thereby Moore's law as a target roadmap. Since all competitors work with the identical development timeline, Moore's law can be viewed as a self-fulfilling prophecy.[9] However, the 2011 annual report of the International Technology Roadmap for Semiconductors maintained the in 2010 predicted slowing growth at the end of 2013,[10] after which time transistor counts and densities are to double only every three years. High-end products with extremely short switching times and high integration densities are made of conventional electronics, fabricated on small areas on rigid substrates with sophisticated, high energy consuming techniques.

More recently, the area of printed electronics encountered a rapid development towards flexible devices. The motivation for this development can be found in the promise of low-cost, high-volume, high-throughput production in roll-to-roll (R2R) or sheet-to-sheet (S2S) processing lines of electronic components or devices which are light weight and small, thin and flexible, inexpensive and disposable.[11] Typically, the aim is to fabricate (semi-) transparent, bendable and even rollable flexible electronic devices such as organic light-emitting diode (OLED)-based displays (**Figure 1**),[12] radio frequency identification (RFID) tags,[13,14] and organic solar cells (OSCs).[15] Flexible electronics face new challenges, not necessarily originating from the small dimensions of the device, but from the deformations and dimensional instability of the substrate.[16]

A key requirement for flexible displays and flexible complementary metal-oxide-semiconductor (CMOS) devices is the low temperature fabrication of organic thin-film transistors (OTFTs) on flexible substrates.[17] This report will focus on the progress on this particular topic. Mass-printing and patterning techniques for flexible TFTs, with flexible displays as the main application, will be discussed here. Attention will also be given to the restricted temperature budget of device materials and substrate compatibility in this respect. The tremendous area of stretchable organic electronics, a subcategory of flexible electronics, will not be reviewed here. The readers are directed to excellent reviews in the literature.[18–22]

Figure 1. 3.4 inch flexible AMOLED Display with 326 pixels per inch and a total thickness of 50 µm. Reproduced with permission.[177] Copyright 2011, The Japan Society of Applied Physics.

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In the first part of this Progress Report, the history of mass-printing techniques is briefly reviewed and examples of these printing strategies for the fabrication of flexible transistors are given and discussed, providing mostly examples from display

applications. The next part describes the development of photolithography and the bottlenecks of processing on low-cost polymeric substrates. From the class of alternative high-resolution patterning strategies, soft and nanoimprint lithography are introduced and their applicability for the fabrication of flexible transistors is discussed and reviewed.

2. Conventional Mass-Printing Techniques

2.1. Flexographic Printing

In flexographic printing, a relief printing technique very similar to letterpress, the image is printed from protruding elements on a plate cylinder to almost any type of substrate (e.g., plastic, metallic films). The elastic printing plate is made by exposure of a light-sensitive polymer, by computer-guided laser engraving, or through a molding process from a metallic plate creating a 3D relief in a rubber or polymer material. Ink is transferred from the ink or fountain roll to an anilox roll, the textures of which hold a specific amount of ink. From the anilox roll, a controlled amount of ink with a uniform thickness is evenly and quickly transferred to the printing plate. The reliefs on the printing cylinder pick out ink from the anilox roll, whereafter the ink is finally printed by pressing the web substrate against an impression cylinder.

For flexographic printing, one can choose from three line-ups either for an easy access and printing on both sides of the substrate, a good registration, or printing of heavier substrates such as corrugated boards. Next to the wide variety of substrates, a typical advantage of flexography is the wide range of inks that can be printed: solvent-based inks, water-based inks, electron-beam curing inks, UV curing inks and two-part chemically-curing inks (usually based on polyurethane isocyanate reactions).

With flexography, continuous conductive grids of Ag ink have been reported on indium tin oxide (ITO)-coated poly(ethylene terephthalate) (PET) foil with a minimal line width of 75 μm.[23] The typical resolution limit of 50–100 μm[24] for flexography can be reduced to ~20 μm by controlled edge dewetting and film breakup of inks, transferring for example Ag ink from a poly(dimethyl siloxane) (PDMS) mold to SU8-coated substrates.[25] In combination with slot-die coating, *n*-octanol has been flexographically printed on poly(3-hexylthiophene): phenyl-C61-butyric acid methyl ester (P3HT:PCBM) to enhance the wettability for the following slot-die coated poly(3,4-ethylenedioxythiophene) - poly(styrene sulfonate) (PEDOT-PSS) layer for the fabrication of a polymer solar cell on PET foil.[4] With flexography, the dielectric and gate of a top-gate OTFT on PET foil have been printed, being the only mass-printing technique applying a low pressure in order to avoid destruction of the underlying layers.[26] A lift-off process was introduced for the fabrication of the lower electrode of a microelectromechanical system (MEMS)-controlled Fabry-Perot display on poly(ethylene naphthalate) (PEN) foil, patterning a 2 μm thin sacrificial layer of black ink by flexography at 5 m/min (**Figure 2**).[27,28]

2.2. Gravure Printing

In gravure (intaglio) printing, an engraved cylinder is rolled over a moving substrate, typically paper or plastic.[29] Excess ink is removed from the protruded elements of the cylinder by a doctor blade before the relatively low-viscosity ink is transferred from the cells to the substrate. Typical cell densities are between 220 and 400 cells per inch, with a groove or cell depth ≈40 μm and width <100 μm.[30]

The width and thickness of printed dots depend on the cell emptying[30,31] and drop spreading behavior, being a function of the depth and width of the engravings in the mold,[32] print speed, ink viscosity and the ink/substrate surface energies.[29] Uniform lines can be formed by merging droplets at a cell spacing to cell width ratio of 1.06 up to 1.40. At a ratio larger than 1.40, scalloped lines will be produced. A combination of rotogravure and inkjet printing has been utilized to fabricate top and bottom gate TFTs on PEN foil.[33] Gravure printing was used to print 70 nm thick, 20–21 μm wide Ag lines (rms roughness 5.8 nm), a 100 nm thin dielectric and the semiconductor.

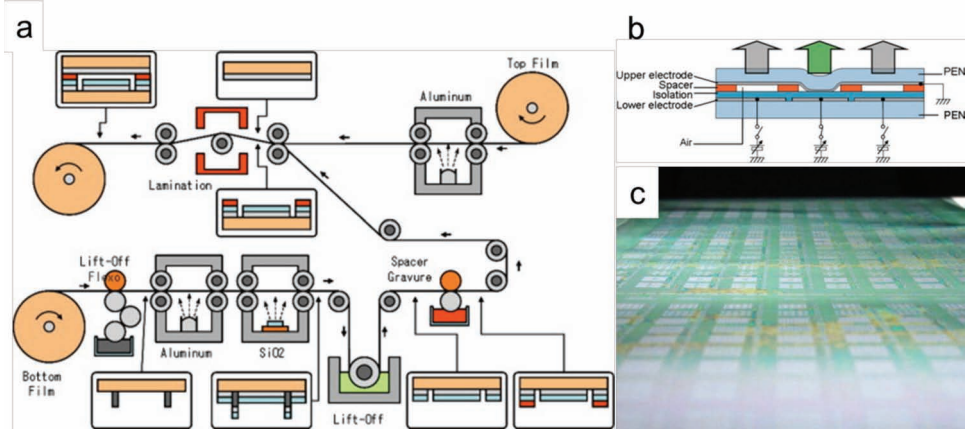

Figure 2. (a) Schematic representation of the R2R fabrication of a MEMS Fabry-Perot display on PEN foil. The lower electrode was fabricated by flexographic printing of a sacrificial black ink for subsequent lift-off. The spacer layer was gravure printed. (b) Schematic representation of a MEMS Fabry-Perot display. (c) Photograph of duplicated display pixels on a large area. The substrate width is 30 cm. Reproduced with permission.[28] Copyright 2011, Elsevier.

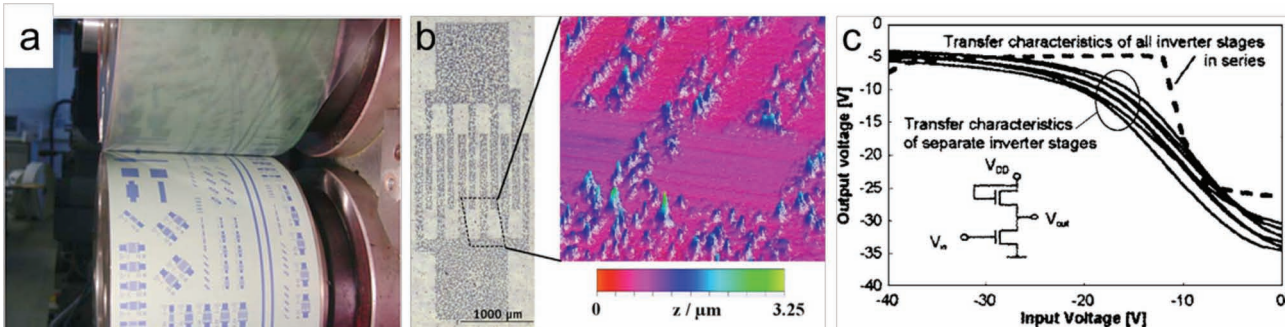

Figure 3. (a) Photograph of an offset printing machine to produce (b) offset printed source/drain structures on PET. (c) Transfer characteristics of separate inverters and of a whole seven-stage ring oscillator. Reproduced with permission.[36] Copyright 2005, American Institute of Physics.

The top electrode was patterned by inkjet printing for precise alignment with a novel fluid guiding technique, resulting in an overlap with the gate and <20 µm line spacing. All-gravure printed OTFTs on PET foil with single-walled carbon nanotubes (SWNT) as a semiconducting layer have been reported, studying the overlay printing registration accuracy (OPRA) and line edge roughness of the source-drain electrodes.[34] Bottom-gate TFTs with a channel length of 170 µm, a width of 3000 µm, a thickness of 680 nm, OPRA of ±10 µm, and a surface roughness of 200 nm have been obtained. Gravure printing has also been used to pattern SiO_2 isolation and spacer structures of a MEMS-controlled display on PEN foil (Figure 2)[27,28] and the semiconductor and dielectric of a ring oscillator on PET foil.[35] An optimized gravure plate design, containing the mesh, cell size, cell density, cell depth and cell angle was used to control the thickness of the SiO_2 to print the three primary colors red, green and blue.

2.3. Offset Printing

In offset lithography, introduced at the end of the 18th century by Alois Senefelder,[2] images are formed by the physicochemical difference between oleophobic and oleophilic areas on the printing master, thus not requiring a pattern relief. The main carrier is oleophobic and often made of aluminum, while the color is taken up mostly by an oleophilic grease layer. Offset-printed features have typically a resolution in the range of 20 µm and a layer thickness below 1 µm,[36] allowing microstructuring up to 200 000 m^2/h. Offset-printed source and drain electrodes of top gate TFTs and a seven-stage ring oscillator have been reported on PET foil (**Figure 3**), showing a gap width in the range of 50 µm and a linewidth down to 100 µm. The dry layer thickness obtained for printed PEDOT was 600 nm.[36] In a modified offset printing technique,[37] developed by LG Display Co., thin and uniform layers of etch resist were printed to form fine patterns of 10 µm width and 6 µm spacing as short channels of a TFT on Si.

2.4. Screen Printing

In screen printing,[38] ink is pressed with a squeegee through a screen onto the substrate. The screen is typically made of a porous mesh, from materials such as a porous fabric or stainless steel. The image to be replicated, the stencil, can be photochemically or manually defined on the mesh. Due to the simplicity of the process, a wide variety of substrates and inks can be used, allowing a high layer thickness which is typical for screen printing. From the three types of screen printing, rotary screen printing has the highest throughput, edge definition/resolution and achievable wet thickness.[39]

In industrial processes, screen-printed films usually have a thickness larger than ≈0.5 µm.[40] Thin and homogeneous layers are not easily obtained by screen printing. As an example, the inhomogeneous 100 nm hole transport layer of an OLED has been reported.[41] Nevertheless, also a 40 nm thin active layer of a bulk hetero-junction photovoltaic device with an rms value of 2.6 nm has been reported.[40] Both devices have been fabricated on glass substrates. Silk screen-printed polymer solar cells have been reported on PET foil by Krebs et al.[42] The anode pattern was defined into an ITO-coated PET foil by rotary screen printing an etch resist and subsequent etching. Electrical contacts made of epoxy silver paste and the conjugated polymer were also screen printed. A screen with a thread diameter of 27 µm and a mesh count in the range of 140–220 cm^{-1} was used. Flexible pentacene transistors have been demonstrated[43] with room temperature, silk screen printed silver resist, forming the top contact source-drain electrodes on poly(phthalate carbonate) foil. The channel length was varied from 40 to 200 µm at a fixed channel width of 1.5 mm. CMOS devices on PEN foil[44] have been fabricated by laser ablation of a 30 nm gold source-drain layer and screen printing. The p- and n-type semiconductor, a 800-nm-thick dielectric fluoropolymer and a gate layer of silver paste were subsequently screen printed, showing a process alignment of ± 25 µm for all printed materials. With the printed inverters, a voltage-controlled oscillator and two differential organic amplifiers were presented. Very recently, a solely screen-printed device, a flexible thin film supercapacitor on polyester (PE) foil, has been reported.[45]

2.5. Concluding Summary

In summary, each of the conventional mass-printing techniques offers its own specific working range. Depending on the desired throughput, layer thickness, material formulation, pressure and temperature sensitivity of the (pre-patterned) substrate, but

certainly also on the cost of fabricating the patterning plate, an optimal choice has to be made.

Flexographic printing is designed for thin, uniform layers providing a better pattern integrity and sharper pattern edges than gravure printing.[27] Basically all types of substrates can be printed, with only low pressures applied to pre-patterned structures on the substrate,[26] thereby resembling a less destructive printing process compared to the other mass-printing techniques. Unique in flexography is the formation of continuous, arbitrarily orientated, uniform lines not relying on merging of discrete dots. The lack of a continuous line in the other three printing techniques, particularly for fine features, has a negative effect on the line consistency, caused by defects such as pin-holes, blocked cells and missing dots.[23] However, flexographic printing of a liquid-phase ink material is prone to film instability and dewetting, thereby forming many defects such as open lines.[25]

Gravure printing is a mechanically simple process known to be advantageous for its high-throughput, high-quality printing of halftone images, and printability of different materials.[46] Adjustment of the cylinder's cup design[27] (e.g., depth of cell) and precise adjustment of each ink formulation regarding its viscosity and surface energy,[47] allows printing of low viscosity inks (e.g., semiconductor inks)[26] or thick layers on flexible substrates, not to be handled by the other mass printing techniques. The fabrication of the gravure plate is expensive compared to other printing techniques though.[4]

Offset printing combines the high resolution and layer quality of gravure printing with a comparatively simple and inexpensive printing plate fabrication,[26] making it an attractive patterning strategy for the fabrication of source and drain of top-gate OTFTs. However, the layer thickness resulting from offset-printed features is reported to be inhomogeneous showing a higher surface and edge roughness when compared to other mass-printing techniques.[26]

Screen printing is an inexpensive, large-area printing technique with good control over the deposition area, resembling an important requisite for fabricating a device that is integrated onto a substrate containing other electronic devices. The quality of screen-printed films depends highly on the number of fibers in the screen mesh, the tension of the mask, the distance from the mask to the substrate, the characteristics (hardness, edge) and process parameters (speed, pressure, angle) of the squeegee, the temperature, the humidity, and the air flow around the printing area.[48] The ink viscosity is linked to all parameters mentioned, and has to be critically adjusted to match the mesh used in the screen mask.[42]

The conventional mass-printing techniques described here have a long-lasting history in printing and will remain important for a wide application, material and substrate range. Flexible electronic devices with a less complex architecture have been demonstrated (e.g., polymer solar cells on PET[42]), using the here reported conventional mass-printing exclusively or in combination with other patterning techniques. However, the limited resolution and control over the layer thickness and homogeneity restrict the applicability for the high-throughput, large-area fabrication of high-resolution flexible-device components such as small-channeled, flexible thin-film transistors.

3. Digital Printing

3.1. Inkjet Printing

A printing technique in the field of organic, large-area electronics often combined with the above reviewed mass-printing techniques is the additive, direct patterning technique of inkjet printing. Therefore, it will be discussed at this point. Precise quantities of a wide range of materials can be deposited in the form of conducting lines or single droplets on various substrates (e.g., foils). It is a low-cost, non-impact and rapid technique with a large potential to manufacture electronic circuits. Costs are reduced owing to digital imaging, eliminating the multiple process steps involved in using a photolithographically defined etch mask and the subsequent deposition and etching steps. As inkjet printing is a relatively fast technique, it potentially enables fast R2R patterning of conductive precursor materials,[49] such as metal nanoparticles[50,51] or metal–organic complexes.[52]

The key challenge is developing suitable ink formulations, determining the drop ejection characteristics and dictating the quality of the printed electrocircuits by influencing the evaporation behavior and orientation (e.g., crystal orientation) upon solvent evaporation. Clogging of nozzles is a serious issue of inkjet printing and can reduce the yield substantially. The resolution is limited to 20 to 50 μm by statistical variations of the flight direction of droplets and their spreading on the substrate.[53] Especially in metal conductive inks, uniform and monodisperse metal nanoparticles in aqueous or organic solvent dispersions[54] contribute to attain a high dispersion stability and low electrical resistivity at low metallization temperatures.[50] The typical sintering step needed to render the precursor compound conductive requires >30 min process time and/or higher temperatures (>250 °C).[49] High sintering temperatures are incompatible with common, polymer foils, such as PET and polycarbonate (PC), having a relatively low glass transition temperature. The choice of foil is therefore restricted to more expensive polymers such as polyimides (PI).[49]

Among the inkjet-printed metal conductive inks, Ag formulations receive a lot of attention,[54] and the first Ag inks are commercially available (e.g., BayInk nanoparticle silver inks, Bayer Material Science). A second type of Ag ink is known as a metal-organic decomposition (MOD) ink. Typically, heat is required to precipitate the metal and burn off the organic ligand in MOD inks, or, in case of NP inks, decompose the organic stabilizer.[49] Reported room temperature sintering techniques destabilize the metal inks by slow evaporation of the solvent or in a faster approach by chemical destabilization. As an example, the coalescence of Ag NPs by exposure to HCl vapor has been reported.[54,55] Inkjet printing of seeding particles for subsequent electroless deposition of metals is another R2R-compatible route to metal lines.[56] Inkjet-printed, conjugated polymers have been reported in LEDs and, in combination with photolithographic patterning of hydrophilic and hydrophobic areas, TFTs on glass.[53] Fully inkjet-printed TFTs have been reported by patterning and sintering each individual layer of the device at an annealing temperature <150 °C (compatible to PET) forming conductive lines.[56] Recently,[57] self-aligned fully printed TFTs on PET

foil have been reported with a minimal gate to source-drain overlap of 0.47 μm. Self-alignment was obtained by wetting-based roll-off techniques of the droplets from previously patterned layers.

In summary, inkjet printing is a versatile, non-contact patterning technique with a resolution down to 20 μm. It is a fast technique often combined with other patterning strategies. Examples of combinations with mass-printing techniques have been given in the previous sections. Combination with high-resolution patterning strategies will be given in the following sections. Furthermore, digital mastering reduces processing costs and allows fast changes to the design.[4] Drawbacks of the technique are the necessary adjustment of the ink viscosity, concentration and solvent system to the nozzle (to prevent clogging) and the substrate material. Spreading of the ink and wanted or unwanted merging of dispensed droplets needs to be controlled. Further solvent, concentration and viscosity fine-tuning is required to control the shape, thickness and morphology of the dried droplet.

3.2. Laser Patterning

With lasers, thin layers of a donor material can also be transferred, in a process called laser-induced forward transfer (LIFT), from a glass support onto an acceptor substrate (e.g., Si, foil) which is placed in close vicinity. In this process, developed by Bohandy[3] in 1986, a pulsed laser beam heats and melts for example a metal through the glass support. Upon sufficient heating, mainly glass components[58] are turned into their gaseous state at the glass/metal interface, building up high pressures that blast metal off the glass support. Metals,[3,58,59] liquids,[60,61] and organic materials[59,62] have been transferred onto acceptor substrates with a highest resolution of 30 μm[59] to fabricate OTFTs on Si,[59] and polymer light-emitting diodes (PLEDs) on glass (**Figure 4**).[62] Flexible OLEDs and OFETs have been reported with a slightly altered LIFT process.[63] Direct laser damage of sensitive materials, such as organic dyes or semiconductive polymers, can be avoided by addition of a dynamic release layer (DLR), converting light to heat by thermal evaporation or chemical decomposition.[62]

4. High-Resolution Patterning

With conventional printing techniques, only a resolution of around 10 μm can be obtained, limiting the bandwidth to 10 kHz for printable semiconductors with a typical mobility of 0.01 $cm^2V^{-1}s^{-1}$.[64] Advanced and flexible electronic devices demand high-resolution patterning techniques. When taking OTFTs as an example, high-resolution patterning would result in a larger bandwidth and higher switching speed while the geometric (parasitic) capacitance, the operation voltage and power consumption will be reduced. In addition, an improved on/off ratio at lower costs with a higher yield on smaller areas is possible.

In general, two types of high-resolution patterning techniques can be distinguished: top-down and bottom-up. In top-down, various lithography methods are miniaturized to pattern nano- to micrometer-scale patterns. Photolithography and scanning beam (or maskless) lithography (e.g., electron beam and focused ion beam lithography) are the main patterning techniques of this area. The most known and widely spread patterning technique in semiconductor industry is optical lithography, which is therefore the only technique covered here.

4.1. Photolithography

Photolithography (and its descendants) is the patterning technique of the semiconductor industry. It proved to be far more capable of reducing the minimal feature dimensions to fulfill Moore's law than one could have imagined. In the 1960s through the mid-1980s, mercury lamps were utilized as light source, producing light across a broad spectrum with several strong peaks at 436 nm ("g-line"), 405 nm ("h-line") and 365 nm ("i-line"). Light filters allowed specific selection of the required spectral line to ideally match to the photoresist. The request of the semiconductor industry for denser and faster chips was met by the development of excimer laser lithography in 1982 by Kanti Jain[65,66] at IBM, leading in the end to the steppers and scanners as primary patterning tools used in microelectronics production of today's world. Today, the world's leading provider of lithography systems for the semiconductor industry ASML, has started shipping their pre-production, extreme ultraviolet lithography tool NXE:3100.[67] The tool is based on 13.5 nm wavelength technology, patterning according to their roadmap at a resolution of 16 nm.[68]

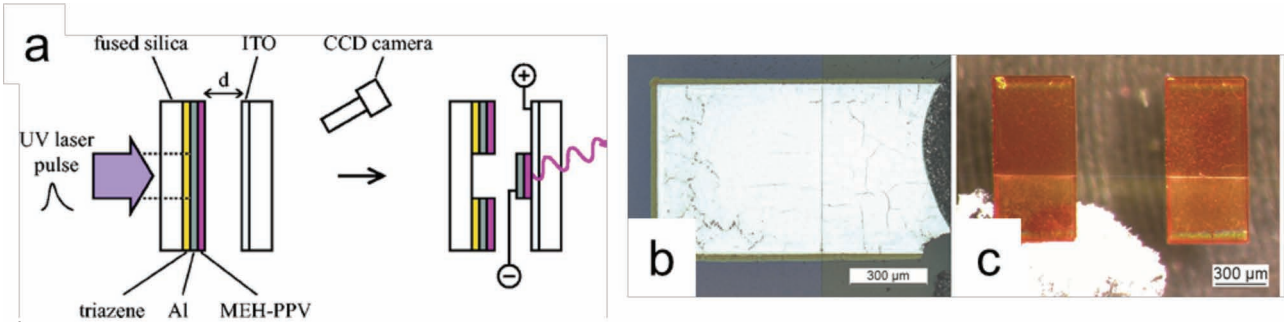

Figure 4. (a) Schematic representation of the transfer of pixels by LIFT. Photographs showing (b) details of the back side of a pixel (Al layer on top), and (c) two pixels through the ITO substrate, where the one on the left is contacted with Ag paste. Reproduced with permission.[62] Copyright 2007, American Institute of Physics.

In the following lines, the basic principle, developments and limitations of photolithography are described. Thereafter, the main challenges of transferring this technology and derivatives to flexible foil will be discussed.

In photolithography, patterns are made by exposure of a thin layer of a photosensitive lacquer (i.e., a photoresist) on a substrate through a mask. The photomask is usually made of glass and a thin, light-blocking layer, typically made of chromium. Light exposure induces a chemical change of the light-sensitive material, changing its solubility in a developer solution. For positive tone resists the exposed, and for negative tone resists the unexposed regions are removed upon developing, resulting in a three-dimensional replica or inverted replica of the photomask on the substrate. The patterned photomask can be used in a subsequent process step as etch mask in order to define features on the wafer.

Photolithography has a couple of limitations. The minimal resolution R (i.e., the critical dimension, CD), given by the Rayleigh equation (Equation 1), is diffraction limited to the wavelength λ_0 in vacuum of the irradiating visible or UV light by the Rayleigh coefficient of resolution κ_1 and the refractive index n of the incident medium, divided by the angular aperture θ of the lens system. The product $n \bullet \sin\theta$ is known as the numerical aperture (NA) of the imaging system. The factor κ_1 is a process-dependent parameter that is determined by illumination conditions, mask technology, and photoresist capabilities with a lower limit of 0.25 for single-exposure optical lithography.[69]

$$R = \frac{\kappa_1 \lambda_0}{n \cdot \sin\theta} \quad (1)$$

The resolution limit of optical lithography has been continuously improved by reducing the exposure wavelength and increase of the numerical aperture. High-end optical lithographic patterning techniques such as deep- and extreme UV,[70] X-ray[71] and immersion lithography[69,72] have pushed the resolution limit into the sub-micrometer and tens of nanometers regime on Si substrates.

On flexible substrates, photolithography is often used to pattern large micrometer features such as a gate or source-drain terminals,[73,74] but also the semiconductor is regularly patterned by photolithography.[75] Flexible, all-polymer FETs have been fabricated by exposing a conducting polymer mixed with a photoinitiator through a photomask with deep UV radiation, rendering the exposed polymer non-conductive.[76]

4.2. Towards Alternative Methods for High-Resolution Patterning

Photolithographic processing requires many steps, is subtractive, and only suitable for patterning small areas.[77] The substrates and organic electronic materials are exposed to corrosive etchants, high-energy radiation, and relatively high temperatures during processing. The high investment and operation costs of photolithographic processing at the resolution limit, are feasible as long as high yields and volumes are targeted. An economically more feasible route to high-resolution electronic devices is envisioned by one of the next-generation lithography techniques (e.g., nanoimprint lithography) on low-cost, polymeric foils. These alternative, high-resolution patterning techniques can be operated at lower costs to obtain the same or an improved resolution compared to the high-end photolithography systems. The integration in high-throughput patterning facilities such as a R2R line, would allow the fabrication of low-cost, large-area, flexible and lightweight devices. However, the transfer of processes from Si to polymeric foils is challenging and not straightforward.

Flexible materials offer lower profiles, lighter weight, more compact end-products, and, often, a better performance.[78] Thin-film polymeric foils with a thickness in the range of 25–200 μm are typically made of polyester (PE), polyimide (PI) or polycarbonate (PC).[79,80] The choice of polymeric foil depends on the desired application, costs and temperature budget of the fabrication process. PE, and then mainly PET and PEN, are often used[81–83] and well-studied[84,85] as polymeric substrate for the fabrication of flexible TFTs in low-cost, low-temperature processes showing a reasonable good mechanical stability and resistance to oxygen and water vapor penetration. Protection of the mainly organic materials of the electronic device from moisture and oxidation can be enhanced by barrier layers, additionally deposited on the foil. Barrier layers can also increase the chemical resistance of the polymers. The most stringent restriction to the patterning process and materials is the limited temperature budget. The low glass transition temperature of the polymeric foils (e.g., ≈70–85 °C for PET[86]) requires alternative deposition techniques and newly engineered materials. As examples of recently developed, low-temperature materials, a high-k dielectric from titanium dioxide[87] and highly conductive self-sintering silver nanoparticles[54] have been reported. The second effect of temperature elevation on the polymeric substrates is a reduced dimensional stability due to a high coefficient of thermal expansion, even for biaxially oriented and thermally stabilized foils.[88] The dimensional stability and waviness of the foils can be improved by a bond-debond approach, temporarily laminating and flattening the foil to a carrier (e.g., Si or glass). These foil-on-carriers supply a stable platform for foil processing, but many new variables are introduced (e.g., bowing) and need to be studied and tuned.[16,88–92] Other bonding strategies developed are Electronics-on-Plastic by Laser Release (EPLaR) by Philips Research,[93] and Flexible Universal Plane for Display (FlexUPD) by ITRI.[94] In EPLaR, PI is coated on display glass as used in TFT-LCD processing plants. A regular TFT matrix is formed on top of it, whereafter the flexible display is released using a laser, allowing also reuse of the glass. In FlexUPD, PI is deposited on glass substrates with local debonding areas. A device (e.g., AMOLED) is patterned over the debonding area, allowing simple and quick cut-out of the patterned device with a slot die coater. The glass carrier cannot be reused however. For mass production, a prototype of an automated flexible-substrate debonding apparatus facilitated with a vacuum system has been reported by ITRI.

The limitations of conventional patterning resulted in the development of new or "alternative" nanopatterning strategies. Amongst these are soft lithography and nanoimprint lithography (hot embossing and UV NIL).

5. Soft Lithography

Soft lithography[95,96] is a collective term for a set of techniques to pattern substrates from the micro- to nanoscale using an elastomeric stamp or mold,[96] typically made of PDMS. A variety of techniques has been developed and named after the utilization of the soft mold. In soft lithography, patterns are formed by printing inks, embossing microstructures, and replica molding by any of the following techniques: Microcontact printing (μCP),[97] Micromolding in capillaries (MIMIC),[98] Nanotransfer printing (nTP),[99–101] Replica molding (REM),[102] Microtransfer molding (μTM),[103] Solvent-assisted micromolding (SAMIM).[104]

In the following lines, only the main soft-lithographic techniques utilized to pattern electronic devices on flexible foils will be further introduced and the obtained results discussed.

5.1. Microcontact Printing (μCP)

Microcontact printing (μCP) is probably the best known soft-lithographic patterning technique. Invented by Whitesides et al. in the beginning of the 1990s,[105] this remarkably simple patterning technique forms routinely self-assembled monolayers terminated by different chemical functionalities with sub-micrometer lateral dimensions.[96] In short, a flexible, elastomeric stamp (typically made of PDMS) with patterned reliefs is inked by an alkanethiol solution. After drying, the stamp is pressed gently against a gold-coated substrate (or other thiol-compatible surface, e.g., silver or copper). Conformal contact between stamp and substrate ensures the transfer of the ink molecules to the substrate, forming rapidly a self-assembled monolayer (SAM) in the contact areas. In a subsequent step, the patterned SAM can be used as etch mask to transfer the pattern into the underlying gold, or a second SAM can be deposited by backfilling.

μCP is not restricted to the transfer of thiols to gold. Silanes, organic or inorganic species, biomolecules, and all sorts of materials can be transferred as inks.[106] As an example of alternative inks in the area of flexible electronics, the printing of Al-porphyrin SAMs on carboxylic groups formed on plastic foils (PET, PEN, and PI) upon oxidation and on inert polymers (i.e., PE, polypropylene (PP) and poly(tetrafluoroethylene) (PTFE)) has been reported.[107] The patterned Al-porphyrin was used in a subsequent step to selectively deposit palladium-tin colloids, initiating Cu growth by electroless deposition (ELD). Also other SAMs have been printed on PET foil to induce Cu growth by ELD, resulting in Cu wires with a resolution of 0.45 to 10 μm.[108,109] Microcontact printed SAMs can also be used to induce a wetting/dewetting contrast on a substrate for selective deposition of a sacrificial resist layer in a lift-off procedure to pattern metals.[110,111] In a wetting-controlled, parallel, low-temperature process, although only demonstrated on Si wafer, μCP was used to pattern a "molecular template" on the substrate directing thin films by spincoating into the desired pattern to fabricate TFTs.[112] Contact printed, organic active matrix backplanes on 5 × 5-inch PET sheets, with 10 μm wide and 20 μm spaced source and drain electrodes forming bottom-contact transistors, have been demonstrated as well (**Figure 5**).[113]

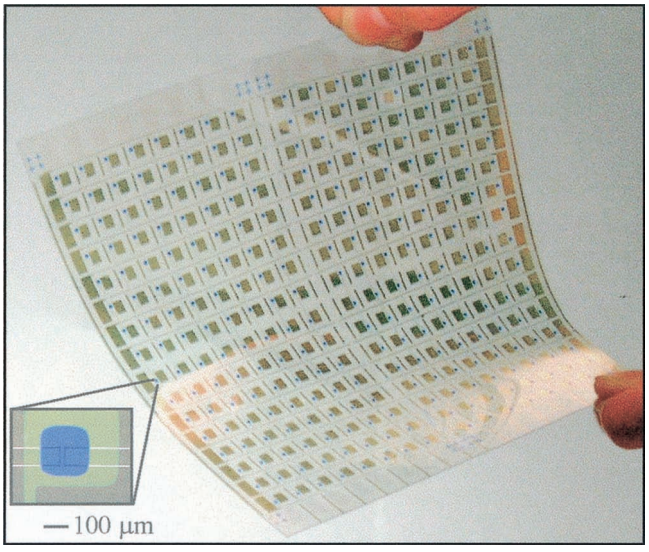

Figure 5. Image of a completed plastic active matrix backplane circuit, patterned by μCP. The inset shows an optical microscopy image of a typical transistor. Reproduced with permission.[113] Copyright 2001, National Academy of Sciences, U.S.A.

5.2. Micromolding in Capillaries (MIMIC)

In micromolding in capillaries (MIMIC), first reported by Whitesides et al. in 1995,[98] capillaries are formed by placing a soft elastomeric stamp, usually made of PDMS, with parallel protrusions on a smooth surface. The grooves form channels (capillaries), which are spontaneously filled with a solution as an effect of capillary pressure upon placement of a drop of the solution at the open end of the capillary. The filling speed is proportional to the cross-sectional dimensions of the channel and inversely proportional to the length of the channel containing the liquid and to the viscosity of the liquid.[114] After complete solvent evaporation or, in case of a low-viscosity polymer precursor after crosslinking, the stamp is removed leaving the patterns on the substrate.

Upon gradual solvent evaporation in the channels, a meniscus is formed under the roof of the stamp channels by capillary forces. Depending on the solute concentration, two kinds of patterns can be obtained. In the high concentration regime, the solution reaches supersaturation when the channel is still filled with solution, resulting in deposition of solute on the entire bottom of the channel. In the dilute concentration regime, supersaturation is reached when most of the solvent has evaporated, and the volume of the residual solvent is not enough to fill the channel completely. In this case, the meniscus forms a U-[115] or W-shape[116] in the channel, dragging under capillary force the solute to the edges of the channel, where it accumulates and aggregates forming defects in the stripes or creating split lines.[117] Specific polymers (e.g., polyaniline, polystyrene) can however, at slow solvent evaporation speed at room temperature, replicate the entire mold dimensions even from very low concentrated solutions of ≈1%.[118] They need to undergo a transition to a dispersion in the channel from which polymer chains precipitate out as very small particles. The small

particles aggregate upon attractive forces into nucleation sites. Particle influx from the larger reservoir at the channel entrance to the nucleation sites is generated to compensate for the loss of solvent upon evaporation. As an example, lines of polyaniline (emeraldine base) with a resolution between 350 nm and 50 μm were formed by MIMIC. After patterning, the emeraldine base was protonated with an acid to the electrically conductive emeraldine salt. With these polyaniline lines, all-plastic field-effect transistors (FETs) have been fabricated on PE substrates.[118] Due to the mechanical instability of the soft polymeric stamp, the dimensions of the channels in MIMIC are typically limited to about a few hundred nanometers.[119] A similar process of patterning a precursor material with MIMIC on a flexible substrate, and transition into a conductive material after stamp removal, has been reported for graphene oxide.[120] With a hard PDMS stamp, centimeter-long and large-area 10 μm wide, ultrathin (1–3 nm) microwires of reduced graphene oxide flakes (500 nm to 1.5 μm) have been patterned by MIMIC of graphene oxide in aqueous solution on 3-aminopropyl-triethoxysilane (APTES)-treated substrates (SiO_2 wafer, quartz, and PET), followed by a chemical reduction with hydrazine vapor. With the resulting microwires, front-gate FETs for sensing applications have been fabricated. Also free-standing films or polymer networks with a resolution of 1 μm can be created by simply dissolving (e.g., dissolving a SiO_2 sacrificial layer with HF), melting or vaporizing the solid support after MIMIC.[98]

5.3. Micro and Nanotransfer Printing (μTP and nTP)

In transfer printing,[99–101] a functional layer is picked up by a rigid or elastomeric mold from one substrate and transferred as continuous[121] or patterned film[122,123] to a second substrate. The substrate's adhesion energy needs to be carefully selected, allowing material pick-up from the first substrate by the mold and deposition onto the second. The adhesion energies can also be adjusted by chemical functionalization. Depending on the patterning scale, the technique is referred to as micro- or nanotransfer printing (μTP[124] or nTP). The feature height of the stamp is in the range of 0.2–10 μm, and the width is between 0.05 and 100 μm.[100]

Molds made of UV-curable poly(urethane acrylate) (PUA), so-called rigiflex[125,126] molds, were rigid enough for sub-100 nm patterning[127] and yet flexible enough in its film form for large-area application in R2R processing. Small molecule and polymer semiconductors for device applications are typically patterned by transfer printing. They are sensitive to oxidation in air and/or show a performance dependence on the polymer microstructure, substrate roughness, film deposition conditions, and solvent exposure.[122] The advantage of transfer printing in this case is the absence of process steps degrading the organic semiconductor or polymer, such as photoirradiation or exposure to incompatible chemicals (e.g., etch solutions), or solvents. Hines et al.[79,128,129] added the basic concept of NIL[130,131] to nTP, patterning all components (metal, dielectric and semiconductor) of a TFT on plastic substrates (latex, nitrile, polyvinyl chloride (PVC), PET, and poly(methylmethacrylate) (PMMA)). Organic materials allowing processing near or above their glass transition temperature, were transferred by the heat and pressure of the thermal NIL process. Bottom-contact, bottom-gate TFTs with a PMMA dielectric layer, Au source-drain and gate electrodes and three semiconductor films from different classes (pentacene (small-molecule), P3HT (polymer), and carbon nanotubes (CNT) (macromolecule)) have been patterned on PET foil. John Rogers and coworkers continuously extend the patterning capabilities of nTP, patterning new materials (large-area flexible 3D optical negative index metamaterials[132]) or transferring fully formed, releasable MOSFETs with thermally grown gate oxides and integrated circuits constructed with them to basically any substrate (includling PI foil) (**Figure 6**).[133]

The strong point of soft lithography is also the technique's weakness. The elastomeric character of PDMS results in stamp deformation upon contacting and during stamp removal. At high aspect ratios, defined as the height divided by the width of the features, buckling or pattern collapse of the elastomeric features can occur owing to gravity, adhesion and capillary forces,[134] generating defects in the pattern to be formed. Low aspect ratios result in sagging as a result of the compressive forces typical of printing and the adhesion between the stamp and the substrate.[96] An aspect ratio between 0.2 and 2 of the relief structures on PDMS surfaces is required to obtain defect-free stamps.[135] Other technical issues for the application of PDMS are the swelling when in contact with nonpolar solvents and the shrinking of about 1% upon curing.[136] An accurate registration for patterning multilayers is also more difficult with a flexible stamp than with a rigid stamp. Next to

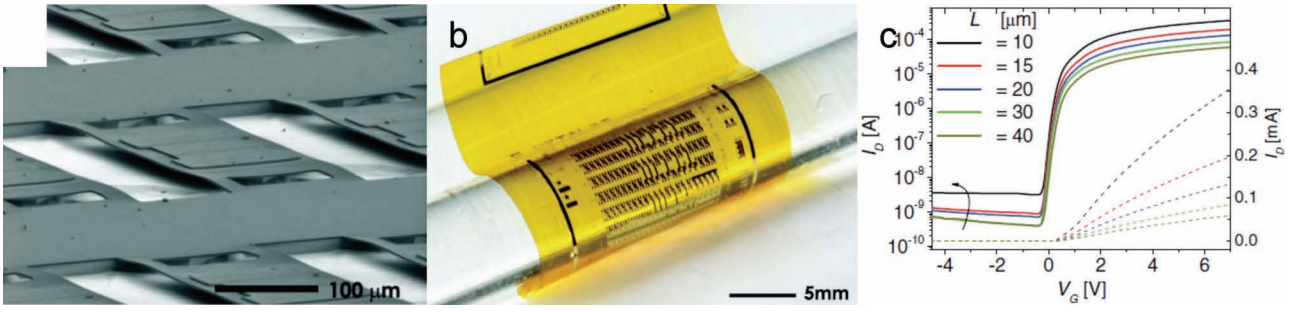

Figure 6. (a) Angle-view SEM image of fully on Si fabricated, releasable MOSFETs. (b) Image of an array of MOSFETs containing various W/L values and a set of logic gates transfer printed onto PI foil. (c) Transfer curves (V_D = 0.1 V) of devices with various channel lengths, L, all with a channel width, W = 150 μm. Solid and dashed lines correspond to logarithmic and linear scale, respectively. Reproduced with permission.[133] Copyright 2011, John Wiley & Sons.

the general challenges of soft lithography, each technique has its own specific limitations. A drawback in μCP is for example diffusion of the SAM-forming molecules to areas not contacted by the PDMS stamp, broadening the feature itself and blurring the feature edge. With MIMIC, it is difficult to replicate the entire channel in case of a high aspect ratio. Line splitting can occur, breaking up the film in wide channels to result in splitted patterns and a non-flat feature profile. Line splitting can also be willingly used to fabricate thin lines at the channel sidewalls, but control over the morphology is limited and line ruptures are a risk. Furthermore, only low-viscosity inks in structures exhibiting a capillary force can be patterned. Arrays of individual dots for example, do not offer an open side for liquid influx. Nanotransfer printing allows selective transfer of materials to a wide range of substrates, making it a very broadly applicable patterning strategy, especially in combination with rigiflex molds. However, this printing technique requires precise adjustment of the intrinsic surface energies or adjustment by chemical modification or topography, to direct the transfer from the mold to the first or subsequent substrates.

6. Nanoimprint Lithography

In thermal nanoimprint lithography (NIL),[137,138] a technique developed by Chou et al.,[130,131] a rigid mold typically made of Si is pressed for a predefined time into an amorphous polymer at a temperature typically 50–70 °C[138] above the glass transition temperature (T_g) of that resist. Above the T_g, the resist turns suddenly low-viscous by altering the mechanical and thermodynamic properties of the polymer.[139] The mold protrusions are thereby filled with resist by squeeze flow (pressure is the driving force to displace the viscous resist) and capillary forces (surface energy controls the wetting and spreading of the viscous resist) until it conforms to the surface relief of the mold.[138] Typically, a highly fluorinated SAM (e.g., 1H,1H,2H,2H-perfluorodecyltrichlorosilane)[140] is applied as an anti-sticking layer to induce easy demolding and complete transfer of resist. Intrinsically, low-energy molds with high mechanical strength have also been reported, for example made of Teflon AF 2400 (T_g = 240 °C).[141] Demolding occurs after reducing the temperature below T_g and release of pressure. A thin residual layer remains on the imprinted substrate, which is removed by anisotropic reactive ion etching (RIE). The opened windows in the resist layer can be used to etch uncovered parts of an underlying layer (e.g., metal) in a direct etch process. Material (e.g., metal) can also be deposited after residual layer removal, followed by a lift-off step dissolving the resist and the material deposited on top of it. With direct etching, an inverted pattern and with lift-off, a replica of the original mold pattern is obtained. Control over pattern replication and residual layer thickness has been improved by the development of UV-based nanoimprint lithography (UV NIL) in 1996,[142] and the further development into step-and-flash lithography (SFIL) by Wilson et al.,[143] crosslinking a low-viscosity resist by UV irradiation through a fused silica mold. UV NIL allows room temperature imprinting at low pressure with good control over the residual layer thickness, making it (also) an ideal tool for patterning on foil.

NIL has been pointed out as one of the ten next-generation lithography techniques addressing the need for low-cost, high-resolution and high-throughput manufacturing of high-density integrated circuits and optics. In addition to the fabrication of rigid microchips, NIL can also be used as structuring technique in the fabrication of flexible electronic devices. For example, flexible OTFTs with source-drain contacts defined by thermal[144] and UV NIL[145] have been reported. Over the past 16 years, a variety of NIL processes has been developed, concerning different types of substrates, resist materials and molding processes. Semi-continuous and continuous imprinting techniques, such as step-and-repeat imprint lithography (step-and-stamp IL[146,147] for thermal resists, step-and-flash IL[143] for UV resists) and R2R NIL[148] have been invented for an increased throughput. Nonflat surfaces can be patterned with rigiflex molds[125] and reverse NIL (rNIL).[149,150] Small and large features can be patterned by hybrid solutions combining NIL and conventional photolithography (combined nanoimprint- and photolithography; CNP).[151] Simultaneous thermal imprinting from the sub-micrometer to millimeter scale on foils is given by double-layer NIL (dlNIL).[152]

Complex electronic devices demand a good registration and overlay control in the patterning process. In OTFTs for example, the overlay of the source-drain and gate layers is important in order to reduce parasitic effects. Optimal alignment and therefore minimal gate overlap can, especially for R2R processes, only be obtained with a self-aligning patterning strategy. The critical overlay can thereby be obtained by "programming" one of the functional layers (e.g., gate) to define the next layer, or a multilevel etch mask defining all following layers can be fabricated on the substrate. In self-aligned imprint lithography (SAIL),[153–155] the entire material stack is deposited on the flexible foil whereafter a single, three-dimensional imprint is made defining all layers of the electronic device. The individual layers and structures of the device are patterned by smartly switching etch processes, opening one layer after the other using the just opened layer as etch mask and the next layer as etch stop. As an example, individual and arrays of bottom-gate transistors with amorphous silicon and transition metal oxides as active layer have been made on a web of 50 μm thick PI.[153,156] A UV-curable resist is thereby patterned with a PDMS mold wrapped around a drum replicated from a patterned Si master. Fabricating a PDMS mold from a Si master mold allows numerous replications of the expensive master, without affecting its properties. The fabrication of a multilevel imprint mold in a two-step photolithographic and RIE process for top-gate a-Si TFTs has been reported and demonstrated on Si substrates.[157] Stadlober et al.[64] introduced a self-aligning technique that utilizes a thermal or UV NIL-patterned Al gate as photolithographic mask in a backside exposure step to define the positions of the source and drain in a photoresist. Following shadow evaporation of the source-drain metal, the photoresist remaining exactly above the gate is removed by lift-off. A minimal overlap of 25—30 nm has been obtained. Very recently, vertical OTFTs have been fabricated on PET foil by a single UV imprint step, defining all layers of the device (**Figure 7**).[158]

For high-throughput, large-area fabrication of flexible electronics, both sheet-to-sheet (S2S) and R2R NIL (e.g., Roller NIL[159]) configurations seem suitable. An extensive review of

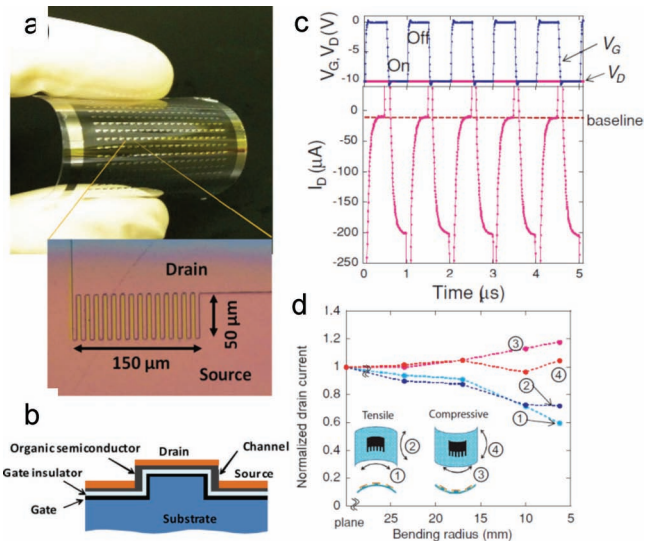

Figure 7. (a) Photograph of an array of OFETs on PET foil patterned in a one-step UV nanoimprint lithography process. (b) Schematic of the cross-sectional view of the vertical channel OTFT. (c) Dynamic response of I_d (lower panel) in response to the pulsed gate voltage shown in the upper panel, with $V_D = -10$ V. (d) Response of the normalized drain current as function of the bending radius when the substrates are bent in different directions. Reproduced with permission.[158] Copyright 2012, John Wiley & Sons.

continuous roller micro- and nano-patterning has been very recently reported by Dumond,[160] giving a good overview of this large-area imprint strategy. Therefore, only a brief summary will be given here. Two types of continuous imprinting exist, distinguished by the type of roller mold. Most often, the roller mold is patterned (**Figure 8**a). This can be done either directly,[161] or by patterning a flexible sheet mold[162–164] or shim and wrapping, or respectively mounting to a blank roller.[24,165–167] Also, patterned molds spanning several rolls have been fabricated, so-called belt molds.[148] Alternatively, the roller mold can be used to apply pressure to a flat (Figure 8b) mold.[159] The latter suffers from similar scaling limitations as batch mode imprinting, in that the mold still has to be scaled to the full size of the substrate.[160] Furthermore, a classification in thermal[168] and UV-roller NIL (Figure 8c)[162,164,165] can be made like in batch patterning.

Since the first introduction of sub-micrometer and nanoscale thermal roller NIL in 1998[159] and UV roller NIL in 2006,[154,169] the community improved the field immensely. Nowadays, seamless roller molds[161] can be fabricated and web tension control systems adjust the influences of temperature, vibration and thermal expansion. Furthermore, resist formulations (especially for UV roller NIL[148]), deposition systems and substrate coatings have been designed or optimized for uniform deposition and spreading, resulting in thin and reproducible layer thicknesses. With a cylindrical mold, pressure is only applied at the contact line between roller and substrate, allowing a considerable decrease of applied pressure and reduced gas entrapment. The distortion span in the resist layer, caused by local defects (e.g., dust) and surface contours or topography, is also reduced by the small contact line width between roller and substrate. Furthermore, the diameter of the cylinder with respect to the feature dimensions should be sufficiently large, in order to prevent damage by demolding to the just imprinted patterns.[170] A typical overlay resolution for a recently built R2R manufacturing line is around 5 µm.[171] With thermal roller NIL, mainly (nano-)gratings[24,159,168,171] have been patterned. UV roller NIL has been applied in applications such as gratings,[148,168] microlenses,[162,164,169] 3D-microstructures with undercuts,[170] antireflective coatings,[163] and flexible electronics.[153,154]

A new member of the imprint lithography family is Substrate Conformal Imprint Lithography (SCIL).[172] It was designed to bridge the gap between UV NIL with rigid molds for best resolution and soft molds for large-area patterning.[173] As a mold, a patterned high-modulus PDMS layer is bonded to a thin glass carrier of up to 6 inches covered with a low-modulus PDMS layer. The PDMS mold is replicated from a Si master mold, allowing numerous replications without affecting

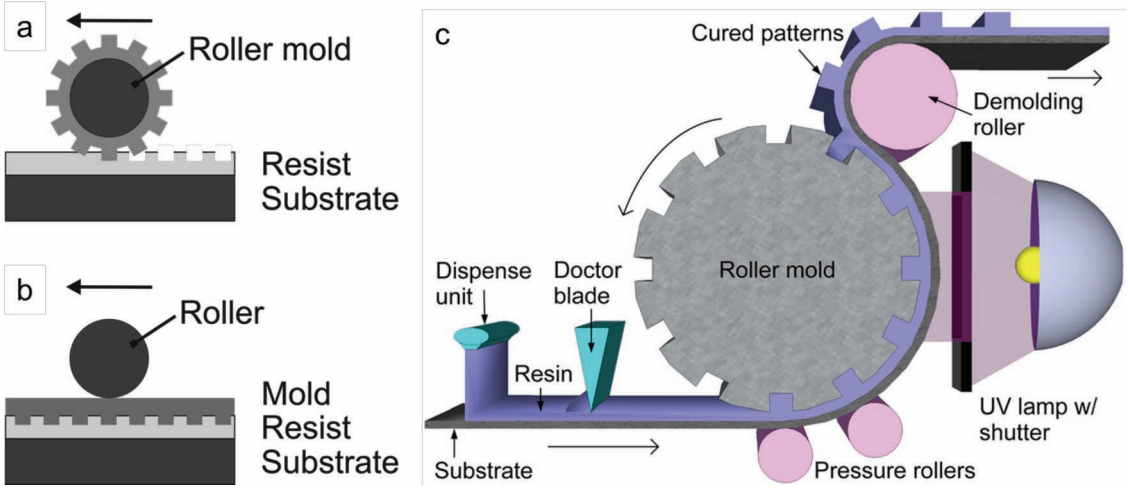

Figure 8. Schematic illustrations of various types of roller NIL, with (a) a patterned roller mold and (b) a flat mold pressed by a non-patterned roller. Reproduced with permission.[159] Copyright 1998, American Vacuum Society. (c) Example of a typical UV roller NIL setup. Reproduced with permission.[160] Copyright 2012, American Vacuum Society.

the original. The 200 μm thick glass carrier provides in-plane rigidity avoiding lateral mold deformation as well as sufficient out-of-plane flexibility. Sequential imprint pressure is applied by evacuating a grooved vacuum plate attached to the mold sheet, allowing entrapped air to escape. Capillary forces pull down the mold achieving contact and induce resist filling into the PDMS features. Demolding of the mold occurs in a wave motion ("peel-off fashion") as well. UV- and sol-gel-based resists have been utilized for the fabrication of 2D and 3D photonic crystals[172–174] and lines with a minimal resolution of 135 nm.[175] Charged particle nanopatterning of 2D and 3D masters allowed the fabrication of SCIL molds and pattern transfer into sol-gel resist with a minimal resolution of 20 nm.[176] The throughput of sol-gel imprinting is strongly limited by the diffusion speed and uptake of the solvent by the PDMS mold. The small layer thickness of the sol-gel (≈100 nm) in comparison to the PDMS mold (≈0.5 mm) is reported to not saturate or swell the PDMS mold, and to diffuse out of the PDMS upon mold release. SCIL is a low-cost, high-resolution patterning technique with potential for large-area fabrication of electronic devices. Its defect-tolerant, room temperature and low-pressure process makes it an interesting patterning technique for flexible substrates. However, no studies have been reported in this direction to date.

7. Conclusions

Large-area, high-throughput patterning of flexible electronic devices has gone through a rapid development in the past decades. With the promise of low-cost, light-weight, thin and bendable devices, commercial mass-printing techniques have been further developed and adjusted to meet the process restrictions given by the polymeric foil substrates. The mechanically unstable and wavy foils limit most strictly the temperature budget of the process to below 150 °C, due to generally low glass transition temperatures of low-cost foils. The use of other polymeric foils, such as PI in EPLaR[93] and FlexUPD,[94] allows higher processing temperatures. A reduced temperature budget also puts pressure on well-established materials and fabrication processes in semiconductor industry. Low-temperature, or even better, room-temperature processes need to be engineered to deposit dielectrics with a high dielectric constant and to pattern and anneal metals or metal precursors. Thermal expansion mismatches between the polymeric foils and patterning molds or masters need to be compensated for high-resolution and precisely registered printing. The polymeric nature of the foils makes them also sensitive to chemicals and aging or yellowing induced by (high-energy) irradiation. Organic compounds of the electronic device need to be protected from influences of humidity and oxygen by specially designed coatings or barrier layers. The limited resolution and quality of the mass printing techniques has led to the request for new, high-throughput R2R lines integrating more recently developed, alternative and high-resolution patterning soft and imprint lithography techniques. Especially for these high-resolution patterning strategies, the dimensional instability, deformations and variations in thickness of the foils contribute to the given challenges of developing large-area, flexible electronics patterned by a R2R strategy. Other than in batch mode, accurate registration and therefore alignment of a multilayer device is not possible or economically feasible to date. Self-aligning device architectures and processes need to be developed and integrated in R2R lines, while keeping the perspective of low-cost and high-throughput processing.

The mass printing techniques flexography, gravure, offset and screen printing, reviewed in the beginning of this report, have a long history in printing on paper and textiles, to which printing on polymeric foils can be added now. Each technique has its individual benefits and drawbacks, and therefore specified applications. Common benefits are the widespread and well understood processing steps and conditions required for large volumes to be printed, up to 200 000 m/h for offset printing. A general and important drawback of these techniques, in particular for fast operating electronic devices meeting Moore's law, is the low resolution, typically down to 20 μm. Inkjet printing is a simple process and is easily combined with mass printing and high-resolution patterning strategies. It is a low-cost, non-contact, low-impact patterning technique benefiting from the flexibility of digital mastering. Digital printing is more customizable, produces less waste and reduces fabrication costs. Costs for the fabrication of a printing master range from relatively low-cost in screen printing to medium cost for rotary screen printing and flexographic printing to very high costs for gravure printing. The resolution of inkjet printing is limited to approximately 20 μm. Ink parameters need to be carefully set to meet the required viscosity, spreading, merging and drying behavior for each type of substrate. The main yield-limiting factor in inkjet printing is nozzle clogging.

Photolithography is probably the most established patterning technique with an extreme resolution bandwidth. However, the high initial and processing costs combined with a relatively low throughput and patterning area make it less attractive for low-cost fabrication of large-area and flexible devices. Furthermore, substrates and organic materials are exposed to corrosive etchants, high-energy radiation, and high temperatures during processing.

The alternative, high-resolution patterning techniques developed in recent years with the aim to deal with the resolution limitations, exceeding costs and small patternable area of photolithography have been reviewed in the last part of this chapter. The family of soft-lithographic techniques allows large-scale, high-resolution patterning of thin and uniform layers on foil. However, no flexible electronic device singularly patterned by one of these techniques has been demonstrated. The low-cost, easily formable, and material-transferring mold material PDMS is mechanically instable under higher pressure and at high aspect ratios: features in PDMS tend to buckle, collapse or sag. Furthermore, PDMS swells in non-polar solvents and shrinks upon curing. μCP is mainly used to print a mask of a patterned SAM onto the substrate, leading in several subsequent steps to selective metal growth. The dimensions of regular microcontact printed features tend to increase and show blurred feature edges due to ink diffusion over the surface. With MIMIC, thin layers can be reproducibly replicated from low-viscous inks experiencing a sufficient capillary force upon channel filling. Channels with a high aspect ratio are usually not completely filled, leading to a concentration-dependent drying profile of the patterned line and/or line splitting and film break-up. nTP

requires careful adjustment of surface energies, allowing pick-up of a prefabricated feature by PDMS from one substrate and transfer to another substrate. In this way, the target substrate is not degraded by irradiation or exposure to incompatible chemicals due to fabrication and patterning on the first substrate. Even complete MOSFETs have been recently transferred to flexible and temperature sensitive foil.[133]

Nanoimprint lithography has been indicated on the ITRS roadmap as one of the ten next-generation lithography techniques addressing the need for low-cost, high-resolution and high-throughput manufacturing of high-density integrated circuits and optics. Numerous reports have shown the applicability of NIL to pattern at least part of an electronic device on rigid, flexible and non-flat surfaces. However, the dimensional bandwidth of simultaneously patternable features in NIL is not as wide as in photolithography. Resist flow is limited, and replication of high-aspect ratio features with the risk for air entrapment is difficult and slow. An additional risk in R2R imprinting of high-aspect ratio features, is the rupture or damage of the imprinted features by the peeling mode of demolding. Thermal NIL is less suited for high throughput processing than UV NIL due to thermal cycling and the risk of thermal expansion mismatches of substrate and mold. Removal of the residual layer, which is typical for NIL, is non-trivial, and should be circumvented by residual layer-free imprinting or used as integral part of the patterned device if possible. The development of R2R imprint with patterned or belt molds has raised the throughput immensely, and the first successful flexible electronic devices have been demonstrated. Key challenge in R2R NIL is the low-cost fabrication of seamless cylindrical molds of a sufficiently large diameter. Web tension and cleaning, continuous ink deposition and layer registration are other challenges in R2R processing. Minimal overlay and good layer registration are evident for fast switching and well performing electronic devices showing low parasitic effects, but they are difficult to control on the mechanically instable and wavy foils. Only self-aligned imprint lithography strategies can be a cost-effective solution for large-area patterning of multilayer devices. The new technology SCIL bridges not only the high resolution obtained with hard molds and large-area processing obtained with soft molds, but it bridges also the batch mode of regular NIL strategies and the continuous mode of R2R. Its defect-tolerant, room-temperature and low-pressure process makes it an interesting patterning technique for flexible substrates. However, resist compositions have to be engineered for optimal and fast filling and replication behavior. Sol-gel systems seem not to meet the request for high-throughput patterning, due to the slow, solvent-diffusion dependent patterning.

8. Outlook

The steadily increasing number of reports and applications in the area of high-resolution printing on low-cost flexible foils reflect the increasing interest of the community to fulfill the promise of low-cost, high-volume, high-throughput production in R2R processing lines. Promising electronic devices such as OLED-based displays, RFID tags, and OSCs are to be lightweight, thin and flexible, inexpensive and disposable. While microlenses and similar simple structures can be reproducibly fabricated today, more complicated, multilayered electronic devices are still a challenge. For every device architecture, a combination of the available deposition, printing and patterning techniques will need to be chosen to provide the most efficient process regarding throughput and costs. For example, high-resolution features will need to be patterned by NIL, but larger contacts can be easily printed by one of the more established, conventional mass-printing techniques. A universal patterning strategy for all applications seems unlikely. The resolution, processing temperature and throughput are the main limitations in the process. Dramatically coinciding with the resolution of multilayered devices is the overlay accuracy, a challenge probably only to be solved in a self-aligned assembly mechanism. First self-aligned fabrication designs have been reported and seem promising for the future. From a materials perspective, cheaper but higher performing low-temperature processable (organic) materials will need to be engineered to meet the restrictions given by the patterning process and thermally sensitive foil.

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