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Development of an array of transition edge sensors for application in X-ray astronomy

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Abstract

We report on the development activities towards a cryogenic array of micro-calorimeters, based on voltage-biased Ti/Au transition edge thermometers. Fabrication issues are discussed along the lines of two fabrication routes. One route utilizes bulk micromachining in [1 1 0] Si wafers, the other route surface micromachining with a sacrificial layer. Prototype 5 × 5 arrays have been fabricated and we present the first performance data: Two arrays were irradiated with 5.9 keV X-ray irradiation and an energy resolution of 6–7 eV FWHM was obtained. The arrays have been designed and their performance is analyzed with the aid of finite element simulation of the electrothermal behavior of a single pixel and thermal conductivity in the supporting structure.

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Keywords: Microcalorimeter; X-ray astronomy; Imaging array; X-ray detector; Cryogenic sensor; Micro machining; XEUS

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1. Introduction

Future space astronomy missions, such as ESA's XEUS, are presently being defined and aim for high resolution X-ray spectroscopy with significantly improved sensitivity and imaging capabilities, compared to the present X-ray observatories [1]. The type of detector which is considered as most promising for the energy range above 1 keV is an array of 32 × 32 voltage-biased superconducting transition edge microcalorimeters [2–4], operated at sub-Kelvin temperatures. In developing these arrays new challenges are encountered, such as the need for low thermal cross talk, the design of high-density electrical wiring, mechanical robustness and the problem of multiplexed readout. In this paper we discuss the two development routes for microcalorimeter arrays and present the first results on a prototype array.

2. Design and processing routes

For the 5 × 5 prototype sensor array two different processing routes are being pursued.

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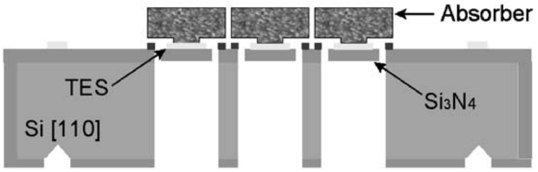

Fig. 1. Schematic side view of a pixel array, formed by route 1. Slots are wet etched into a Si_3N_4 coated Si[1 1 0] wafer. The pixel structure on the top is formed by e-beam evaporation, sputter deposition, etching and lift-off processing techniques.

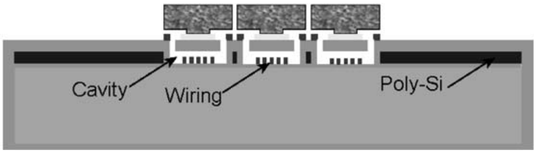

Fig. 2. Schematic side view of a pixel array, formed by route 2. A poly-Si sacrificial layer is used to create a cavity under each pixel. Access to the cavity is either from top or bottom side (not shown in this figure.

The design of the Ti/Au thermometer, Cu/Bi absorber and Si_3N_4 cooling link is in principle identical for both routes. The difference is the formation of the supporting structure. In route 1 this structure is formed by etching deep, vertical slots in the backside of a Si [1 1 0] wafer, using anisotropic wet etching. The resulting walls have a [1 1 1] orientation and a smooth surface (Fig. 1). In route 2 we create a shallow cavity underneath the membrane by surface micromachining techniques, using a poly-Si sacrificial layer. The cavity is opened at the end of the process, by wet TMAH etching from the front side or from the backside through a dry etched access hole. The advantage of route 2 is that it results in a structure with better thermal conductance and lower thermal cross talk. Furthermore, the structure is mechanically more rigid and it opens the way for conducting the wiring under the pixel, see Fig. 2.

An elaborate finite element model[1] of a pixel and arrays has been constructed. It includes diffusive electron and phonon transport, electron-phonon coupling and Kapitza resistances [5]. Together with separate 2- or 3-dimensional models of the heat transport in the support structures, it forms an important tool in the design of a complete array.

3. Array fabrication and characterization results

Recently, the first operating prototype arrays have been fabricated by the SRON-MESA collaboration. A micrograph of one of the arrays is presented in Fig. 3. This array was processed using route 1. Because of limitations in our present characterization setup, not all pixels have been wired to the perimeter. Instead we have chosen to read out three representative pixels, one in the center, one at the edge and one in the corner of the array. The other pixels are connected in parallel so that bias power can be applied across the whole array. This array contains Cu absorbers, while future arrays will have mushroom-shaped Cu/Bi absorbers as schematically shown in Figs. 1 and 2.

Fig. 4 shows that the *R–T* curves of three pixels in one array are very similar. The inset in Fig. 4 shows the *I–V* curve of the side pixel. The power required to voltage bias the pixels ranges from 0.6 pW for pixels with Si_3N_4 beam width of 15 μm to 4.6 pW for pixels with a 200 μm wide strip. The bias power of the center pixels is 10–20% lower than that of the corner pixels. Using the finite element model, we could explain this either by a 4

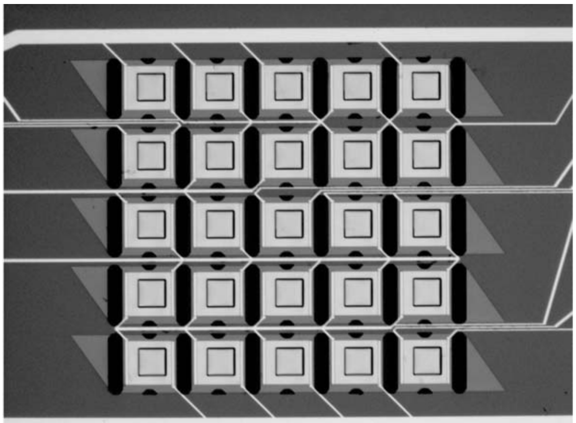

Fig. 3. Prototype calorimeter array, fabricated using route 1. The black areas around the pixels are slots, etched into the nitride membrane, for tuning the thermal conductance. A Cu absorber is at the center of each TES.

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[1] Software and support: FEMLAB 2.3, Comsol AB.

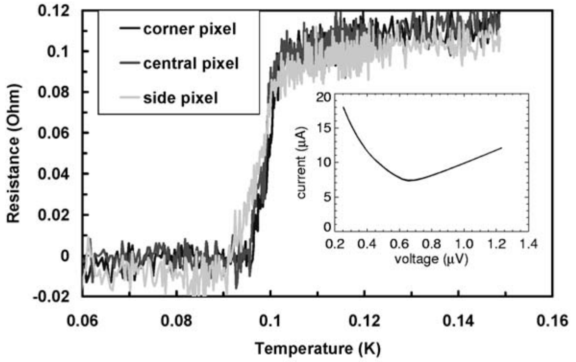

Fig. 4. Resistance vs. temperature of a side-, corner- and center-pixel of a 5×5 microcalorimeter array. The inset shows the current voltage characteristics of the side pixel.

times lower value of the membrane conductivity, compared to that of single pixels on large (3 mm) membranes, or by an interface resistance between the nitride membrane and the Si-support. In the latter case we need to assume a boundary conductance of $0.5\,\mathrm{W/K^4\,m^2}$, much lower than typical metal–insulator interfaces [5]. A more solid analysis will be made when measurement results on specific thermal test structures become available.

Furthermore a preliminary characterization of the X-ray response (5.9 keV photons) was done. For two of the arrays a side pixel was voltage biased and an energy resolution of 6 eV FWHM was measured. The resolution is degraded by bias voltage instabilities and poorer than measured for our single pixels ($\Delta E = 3.9$ eV [4]).

With the surface micromachining route we did not fabricate working prototypes yet. The support structure however has been fabricated separately (see Fig. 5). It was also tested that the process of etching the cavity when the rest of the metal layers are present can be done without affecting the superconducting properties of the thermometer. Key to this process is the use of tiny bumps to prevent sticking of the membrane to the bottom of the cavity. The sidewalls of the cavity are formed by etching narrow slots in the poly-Si sacrificial layer, which are filled during deposition of the top layer of Si-nitride, which will form the membrane (see Fig. 6).

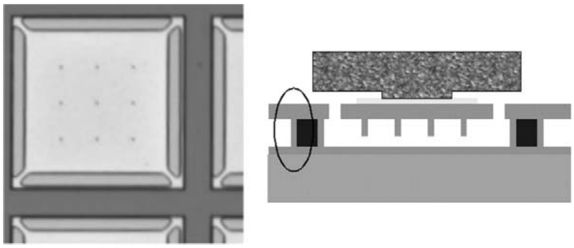

Fig. 5. Left: A pixel from a 5×5 array support structure, fabricated with route 2. Right: A schematic side view of the cavity with nitride bumps and sidewalls. The metal layers in the schematic view have not yet been integrated. A picture of the encircled area is given in Fig. 6.

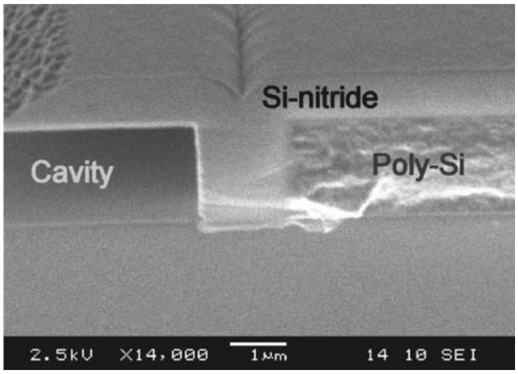

Fig. 6. Detail of the sidewall of the cavity under a pixel. The silicon-nitride fills a narrow slot in the poly-Si sacrificial layer.

Acknowledgements

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