Current Degradation of a-Si:H/SiN TFTs at Room Temperature and Low Voltages

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***Abstract*—This paper focuses on the long-term electrical degradation of hydrogenated amorphous silicon (a-Si:H)/silicon nitride (SiN) thin-film transistors (TFTs). Different from the classical method where the electrical degradation of a-Si:H/SiN TFTs is quantified by the shift of the threshold voltage after a period of stress, the authors choose to describe the degradation in terms of drain–current transients that appear during alternative periods of electrical stress. It is shown that the contributions of charge trapping and defect creation to the drain–current degradation can be discriminated based on stress time, stress voltage, and temperature. A numerical model with variable parameters is proposed to fit both short- and long-term transients. This paper shows that the long-term current degradation is related to the changes in the interface trapped charge, whereas the creation of the defects dominates the short-term current degradation.**

***Index Terms*—Charge carrier processes, modeling, semiconductor device reliability, semiconductor-insulator interface, thin-film transistor (TFT).**

I. Introduction

DURING its operation, a thin-film transistor (TFT) is subjected to repeated electrical stress and relaxation periods that degrade its electrical characteristics. A reliable TFT must overcome both short- and long-term effects of alternative electrical stress.

A vast majority of the papers regarding degradation of electrical parameters of TFTs focuses on the shift of the threshold voltage due to gate voltage stress at room temperature or at elevated temperatures. The threshold voltage is generally extracted from current–voltage (I–V) characteristics before and after a period of stress, and the time dependence of the shift in the threshold voltage is fitted with degradation models in the literature.

The threshold voltage degradation in TFTs with hydrogenated amorphous silicon (a-Si:H) as active layer and hydrogenated amorphous silicon nitride (on short SiN) is explained in the literature by two mechanisms, namely 1) defect creation in the semiconductor and 2) charge trapping in the insulator. The defect creation in a-Si:H is explained by the following two-step mechanism: breaking of weak Si–Si bonds due to stress, followed by the formation of a trap state called dangling bond and dispersive hydrogen diffusion that compensates the broken bond [1]. The defect pool model (DPM) presents a unifying description for creation and removal of the states at different energies in the a-Si:H band gap. In that model, a positive voltage stress leads to the formation of defect states in the lower part of the a-Si:H band gap, whereas a negative voltage stress forms defects in the upper part of the band gap. Because the kinetics and stabilization of defects is considered to be controlled by hydrogen diffusion, the defect creation is a temperature-dependent process. The defect creation is considered to be very slow at room temperature where only the occupancy of the states in a-Si:H changes but not the density of the defects [2]. There is also the view that the defect creation in a-Si:H may actually appear in bias stress measurements performed at room temperature conditions [3]. Charge trapping in the insulator is considered particularly important for TFTs with hydrogenated SiN as gate insulator that is prone to form dangling bonds in the presence of a gate voltage stress. In the charge–trapping model (CTM), it is considered that the interface charge is injected into the existing trap states in the gate insulator when a gate voltage stress is applied. A more recent model proposes that the threshold voltage shift is due to charge injection from the TFT channel into the traps located at the interface and close to the interface in SiN. When a stress is applied, the injected carriers from the channel thermalize in the states at the interface and its vicinity and then move to deeper energy states in SiN at longer stress times, larger stress, or higher temperature [4]. There is evidence that charge trapping is temperature sensitive as well [5], [6].

This paper is organized as follows. In Section II, we refer to the measurement methodology and modeling issues, with reference to some of our earlier published paper. In Section III, we provide a specific description of the devices under test (DUTs), followed by the experimental data in Section IV. The numerical modeling of the experimental results on the drain current transients is presented in Section V. We emphasize the influence of our model parameters on the fitting of the experimental results and the expected agreement with values found in the literature. We also discuss in Section V the short and the long stressing time experiments before the final Section VI in which we present our conclusions.

II. Measurement Methodology and Modeling Issues

In a previous paper, we presented an accelerated degradation method of testing the TFTs during stress based on the measurement of the source-to-drain current I_{sd} transient during

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TABLE I
PARAMETERS OF DUT USED IN THIS PAPER

DUT	a-Si:H thickness [nm]	SiN thickness [nm]	Field effect mobility $\mu[cm^2V^{-1}s^{-1}]$	Initial threshold voltage $V_{t0}[V]$	Ratio between channel width and length (μm) (W/L)	Insulator SiN capacitance per unit area C_i [Fcm^{-2}]	Initial drain current I_0 (A)
1	250	330	0.41	2.3	2 (18/9)	$1.741 \cdot 10^{-6}$	$5.65 \cdot 10^{-6}$
2	250	300	0.38	3.3	2 (200/100)	$1.8 \cdot 10^{-6}$	$2.50 \cdot 10^{-7}$
3	250	300	0.21	4	1 (100/100)	$1.918 \cdot 10^{-6}$	$7.37 \cdot 10^{-7}$

periods of gate voltage stress and relaxation. In the linear operation regime, the source-to-drain current is proportional to the threshold voltage, which means that in either method of testing used, i.e., I–V characterization or transient current method, the mechanisms that contribute to the degradation of the threshold voltage and current must be the same.

The a-Si:H TFTs are known to have a large threshold voltage, and when the threshold voltage is large, I–V characterization itself stresses the device. Thus, in order to measure the drain–current, the gate voltage is swept from zero to values ten times above the threshold voltage, which means that a gate voltage stress is applied on the device. The transient current method eliminates this inconvenience because the measurements of the current are taken at a minimum time allowed by the equipment, thus avoiding the accumulated stress due to voltage sweep. This method of testing is an all-in-one technique to study the short- and long-term current degradation during forward and reverse gate voltage stress and during relaxation.

In the short term, the result of forward and reverse gate voltage stresses was a transient decay and recovery of the measured current, respectively. The decay and recovery of the drain–current was modeled by the progressive degradation model (PDM) that described the charge exchange between channel and adjacent insulator region during electrical stress. The model assumes that extra states are created at the interface during stress; carriers from the channel fill these states and are then trapped in states located in a highly defective region, close to the interface in SiN. In the literature, these states are called switching states, and they exchange charge with the a-Si:H conduction band [7]. The model and fitting of the experimental work that we did on short-term degradation are presented elsewhere [8].

In this paper, we discuss the degradation of the drain–current in a-Si:H/SiN TFTs subjected to long-time alternative gate stress and relaxation in conditions of low voltage stress at room temperature. After many cycles (30 cycles) of alternative stress and relaxation, the current shows a descending trend. In normal working conditions, a TFT works at room temperature, and it is subjected to repetitive forward/reverse low gate voltage stress, followed by relaxation, and therefore, it is important to study the behavior of the TFT's electrical parameters in time in these conditions.

A similar study of the drain–current transient in a-Si:H/SiN TFTs but measuring only the transients during repetitive positive gate voltage stress was studied by Libsch [9]. He showed that after each interruption of a voltage stress and continuation of stress, a slight decreasing trend of source-to-drain current $I_{\rm sd}$ occurs. The trend was fitted with a stretched exponential equation (STE) and interpreted as electron trapping within the gate insulator near the a-Si:H/SiN interface. In this paper, we consider the results of long time testing of the drain–current that resulted from alternative stress/relaxation experiments on TFTs with SiN of different stoichiometry. The devices subjected to tests are described in the following section.

III. DUTs

It is known that charge trapping appears predominantly in TFTs made with Si-rich SiN, and creation of defects is more severe in a TFT with low-quality a-Si:H (γ-a-Si:H) [10], [11]. It is also known that the bottom gate devices are affected more by degradation than top gate devices due to interface state charging [12].

In our experiments, three different types of a-Si:H TFTs here named DUT are made as follows: two bottom-gate TFTs with different $x =$ Si/N ratio (one above-stoichiometric with $x = 1.5$ and one substoichiometric with $x = 1.2$) and one commercial top-gate TFTs with N-rich SiN as gate insulator.

The a-Si:H and SiN layers in all DUT have been deposited in one run by plasma-enhanced chemical vapor deposition (PECVD). The a-Si:H in all three DUTs is considered of similar quality in all three devices. The stoichiometry of SiN layer was altered by changing the ammonia flow in the deposition chamber. The details of deposition and physical characterization of as-deposited layers are given in [13]. We also use commercial top-gate TFTs on glass plate with the following structure: glass/ITO/MoCr/n^+a-Si : H/a-Si : H/ $SiN_{1.7}$/MoCr (labeled DUT 1). For the bottom-gate TFTs, a-Si:H and SiN layers are deposited on a highly doped Si substrate. The bottom-gate TFTs have the following structure: Al/p-type c-Si/ $SiN_{1.5}$/a-Si : H/n^+a-Si : H/Al (labeled DUT 2) and Al/n-type c-Si/ $SiN_{1.2}$/a-Si : H/n^+a-Si : H/Mo (labeled DUT 3).

The electrical parameters of all DUTs are provided in Table I.

Prior to measurement, all the devices are annealed at 220 °C in vacuum for half an hour and then cooled down slowly to room temperature. An exception makes DUT 2 the type of devices that are annealed in vacuum at 180 °C for 1 h in order to avoid the degradation of Al contacts.

A fresh device is used in each experiment in order to avoid the effects of accumulated stress.

IV. EXPERIMENTAL PROCEDURE

The stress tests are performed in duty cycles. Each cycle consists of four periods of positive stress (noted S+), followed by relaxation (R), followed by negative stress (S-), and then

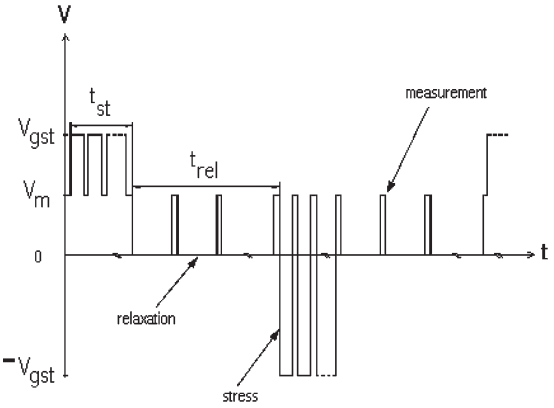

Fig. 1. Measurement and stress sequence used in our experiments.

followed by relaxation (R). We measure the source-to-drain current as function of time during S+, S-, and R (Fig. 1).

In the S+ and S- periods, the gate is forward- and reverse-biased, respectively, with the same stress voltage $|V_{\rm gst}|$, whereas the drain voltage is kept small and the source is grounded. In the R period, the three terminals are grounded. The gate and the source-to-drain voltages used for stress and measurement are listed in Table II.

The chosen conditions for the measurement of the drain–current correspond to the linear regime of TFT's operation. In the linear regime, the channel potential is constant, and the hot carrier effects and drain pinchoff are ruled out. The gate voltage during the measurement of the source-to-drain current is lower than the critical voltage that otherwise might cause insulator breakdown, but it is still higher than the threshold voltage required for a flow of carriers to be established between the source and the drain.

An HP4156B parameter analyzer is used to measure the drain–current. The analyzer is controlled by the Integrated Circuit Characterization and Analysis Program (ICCAP) platform program, which uses a C++-written routine for the voltage stress and current measurement procedure. The precision of the measurement is within 2%. The measurement time including the program-to-analyzer communication is approximately 2 s, which is much less than a total of 30 s measurement time when an I–V characterization is performed.

The values of the applied voltages on the source, drain, and gate terminals are programmed to be applied during certain time intervals for stressing $(t_{\rm st})$ and relaxing $(t_{\rm rel})$. The source-to-drain current $(I_{\rm sd})$ is measured at user-selected times during these intervals (polling times, $t_{\rm poll}$). The gate voltage is switched from high values during stress to low values during current measurement. We choose the experimental stressing time such that the device could be stressed for a long time through many cycles, without damaging it. The relaxation time is set to be longer than the stress time in order to allow the device to relax, and if possible, to reach the initial $I_{\rm sd}$ value measured before the stress being applied. The selected time intervals used in the experiments presented in this paper are shown in Table III.

For the measurements at different temperatures, the sample holder was heated from 273 to 343 K using a Temptronic temperature controller.

V. Results and Discussion

A. Short-Term Degradation

The alternative stress experiments show that the current decreases when stressing the gate with a forward voltage (S+) and increases when stressing the gate with a reverse voltage (S-). The current increases when a relaxation period (R) follows a forward stress and decreases when a relaxation follows reverse stress. We noticed that the current does not recover to its full initial value even if the duration of relaxation after S+ is increased. By each complete duty cycle (S+/R/S-/R), the current $I_{\rm sd}$ progressively degrades in a decreasing trend whose rate of decrease is higher with an increase in the Si/N ratio (Fig. 2).

In a previous paper [14], we presented the results of alternative duty cycle experiments at different temperatures and voltages. We noticed that the resulting trend of current is dependent on temperature only at the beginning of the experiment (Fig. 3). In the first two cycles, we see an increase in the current degradation (as the decrease of the normalized ratio I/I_0) when the temperature increases, but after this, the trends are scattered, and any relationship between current degradation and temperature is not noticed.

The application of the initial cycles of repetitive stress and relaxation sequences might cause a temperature-dependent degradation of the drain–current that can be associated with the thermally activated creation of interface defects. This behavior, however, is not maintained for longer periods of repetitive stress. As the duration of the experiment increases, the degradation of the current seems to become temperature independent. Two explanations are possible: Either the creation of defects is accompanied by the removal of unstable defects at a certain temperature and we see a "back-effect" of creation/removal of interface defects or charge trapping takes place in a region rich in potential defect sites like the transitional region of the insulator, which is close to the interface.

The experiments performed at different gate voltage stresses show that the trend depends on the magnitude of the stress voltage. A dependence of the current degradation with the applied stress voltage is clearly visible during the entire experiment where we noticed that the degradation increases when the applied gate stress voltage increases (Fig. 4).

Two initially different trends appear when the cycle started with a negative voltage stress instead of a positive one (S-/R/S+/R, which is the so-called reverse duty cycle). It is noticed that the trend is logarithmic like in the reversed duty cycles and power-like in the other case (Fig. 5). A possible explanation for the different trends that appear when the test starts with a negative stressing period instead of a positive stressing period is the misbalance between the degradation mechanisms that act during positive and negative stressing periods, respectively. The defects are apparently easier created during the positive stressing period than removed (or recovered) during the negative stressing period. In the negative stressing period, the removal of defects is slower than the detrapping of the carriers, and consequently, we consider that the detrapping prevails upon the removal of defects.

The behavior of the current transients during the experiments at different temperatures, different voltages, and during reverse

TABLE II
BIAS VALUE DURING STRESS AND MEASUREMENT

	S+	R+	S–	R–
Voltages during stress	V_{gst} = 20 V V_d = 0.5 V V_s = 0 V	V_{gst} = 0 V V_d = 0 V V_s = 0 V	V_{gst} = 20 V V_d = 0.5 V V_s = 0 V	V_{gst} = 0 V V_d = 0 V V_s = 0 V
Voltages during measurement	V_{gm} = 10 V V_d = 0.5 V V_s = 0 V	V_{gm} = 10 V V_d = 0.5 V V_s = 0 V	V_{gm} = 10 V V_d = 0.5 V V_s = 0 V	V_{gm} = 10 V V_d = 0.5 V V_s = 0 V

TABLE III
STRESS AND RELAXATION TIME AND INTERVAL BETWEEN TWO MEASUREMENTS

	S+	R+	S–	R–
Stressing times	t_{st} = 100 s	t_{rel} = 300 s	t_{st} = 100 s	t_{rel} = 300 s
Polling times	t_{pollst} = 10 s	$t_{pollrel}$ = 30 s	t_{pollst} = 10 s	$t_{pollrel}$ = 30 s

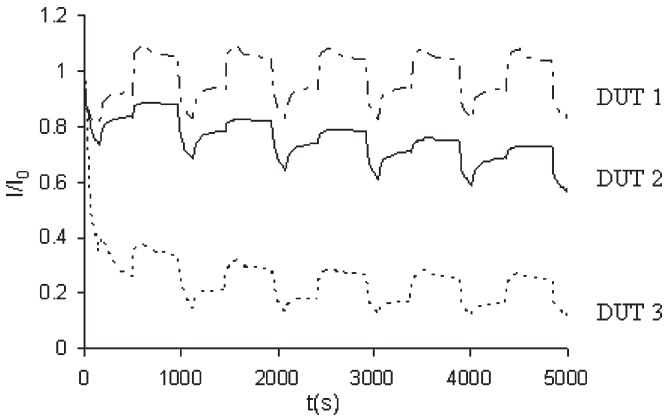

Fig. 2. Normalized currents transient during the S+/R/S-/R duty cycle for DUT 1, 2, and 3 ($T = 273$ K).

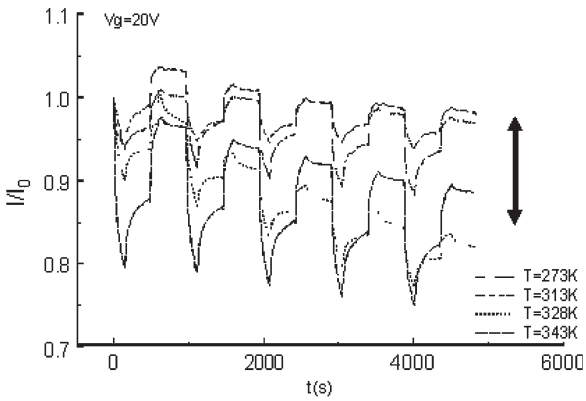

Fig. 3. Reverse test S-/R/S+/R (circles) and forward test S+/R/S-/R (triangles) applied each on fresh devices. The experiments have been performed on DUT 3 at room temperature with the testing time and voltages listed in Tables I and II. The trends are indicated by dotted lines.

duty cycle supports the idea of a multitrapping motion of the carriers at the interface in the SiN region [9], [15] rather than in the bulk of a-Si:H [16], [17].

Our experiments at short stress time were well described by a model named PDM, which describes the current transients as due to the combined effects of interfacial defect creation/removal and charge trapping/detrapping in close vicinity of the interface in the insulator. This model successfully fitted the time dependency of the drain–current during positive,

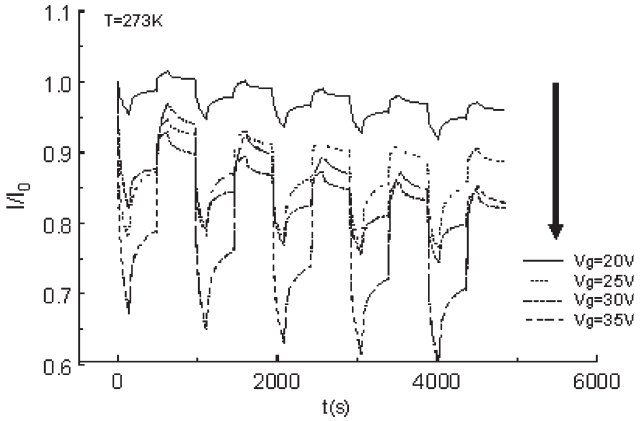

Fig. 4. Tests performed at the same temperature ($T = 273$ K) and different gate biases using DUT 3 TFTs.

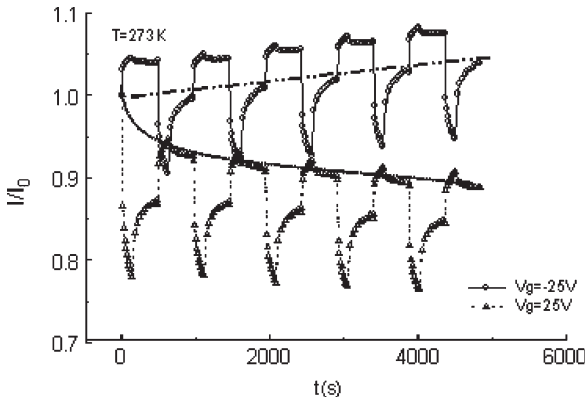

Fig. 5. Tests performed at the same gate bias (conditions of experiment in Table II) and different temperatures using DUT 3 TFTs.

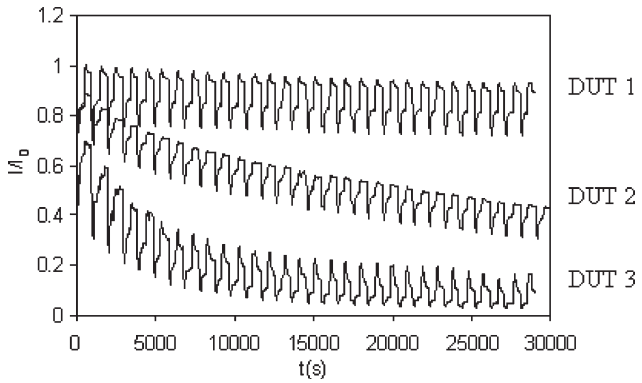

Fig. 6. Normalized currents for long time stress ($T = 273$ K; voltages are given in Table II).

TABLE IV
SYMBOLS AND VALUES USED IN MODELING

Symbols	Signification	Value
V_{gst}	Gate stress voltage	20 V
x_0	Tunnelling distance	$1 \cdot 10^{-8}$ cm
d	Interface states decay distance	$6 \cdot 10^{-8}$ cm
d_i	Insulator thickness	$3.3 \cdot 10^{-5}$ cm
σ	Capture Cross Section	$5 \cdot 10^{-13}$ cm^{-2}
v	Carriers thermal velocity at room temperature	$1 \cdot 10^{+7}$ cm s^{-1}
E_c, E_v	Energy of the a-Si:H conduction and valence bands	1.72, 0 eV

TABLE V
PARAMETERS OF FITTING FOR THE DUT 1 EXPERIMENTAL DATA

model	DUT1	DUT2	DUT3
STE			
τ	$5.324 \cdot 10^{7}$ s	$7.730 \cdot 10^{5}$ s	$7.015 \cdot 10^{5}$ s
β	0.295	0.299	0.448
PDM			
D0	$2.767 \cdot 10^{17}$ cm^{-3} eV^{-1}	$7.767 \cdot 10^{17}$ cm^{-3} eV^{-1}	$8.767 \cdot 10^{17}$ cm^{-3} eV^{-1}
Dint	$1.370 \cdot 10^{18}$ cm^{-3} eV^{-1}	$4.111 \cdot 10^{19}$ cm^{-3} eV^{-1}	$5.244 \cdot 10^{19}$ cm^{-3} eV^{-1}
α	0.285	0.296	0.379

negative, and relaxation periods holding a single set of parameters $D_{\rm int}$ and α that represent the interface state density and a dispersion factor, respectively.

The results of the alternative stress/relaxation experiments S+/R/S-/R at a long period are discussed next.

B. Long-Term Degradation

The prolonged duty cycles (30 cycles in one day as shown in Fig. 6) result in a descending trend of the current whit values that does not saturate, as the short time experiments (5 cycles) would suggest. The trend is well fitted by an STE given by $\Delta I(t) = W/L \cdot \mu \cdot C_i \cdot V_d \cdot (V_g - V_{to}) \cdot (1 - \exp(-(t/\tau)^{\beta})$ and by the PDM with $\Delta I(t) = W/L \cdot \mu \cdot q \cdot V_d \cdot (\int_0^{d_i} \int_{E_v}^{E_c} (D_0 + D_{\rm int} \cdot t^{\alpha} \cdot \exp(-x/d) \cdot G(E,x,t) dE dx)$. Both equations resulted from models where the dominant degradation mechanism was the charge exchange between the a-Si:H channel and the SiN border traps.

We mention that other fitting equations resulting from other models (defect creation and charge trapping) did provide an acceptable fit to our data. The STE has two fitting parameters, namely β and τ, where β is a temperature-dependent dispersion coefficient, and τ is a characteristic trapping time related to the density of weak bonds, density of band tail states, and hydrogen diffusion coefficient. The progressive degradation equation has three parameters, namely D_0, $D_{\rm int}$, and α. D_0 represents the volume density of existent insulator traps, $D_{\rm int}$ is the volume density of the interface traps, and α is a dispersion coefficient. The signification of the symbols and the values used in modeling are listed in Table IV. The parameters of modeling with STE and PDM are presented in Table V. An example of fitting the trend of DUT 1 with STE and PDM is shown in Fig. 7.

The values of the STE's fitting parameters change as the Si/N ratio of the SiN insulator change: τ decreases and β increases as the Si/N ratio increases. Because a-Si:H is considered of the same quality in all devices, the changes are the effect of charge trapping in the gate insulator. The values published by different authors for the STE's fitting parameters vary from 0.25 to 0.57 for β and from 10^{10} to 10^{4} s for τ. The values of these two parameters are impacted also by the fabrication process and the deposition conditions of a-Si:H and SiN layers, but to our knowledge, no comprehensive relation was established between the Si/N ratio and the variance of STE's parameters. The fitting with the progressive degradation equation gives $D_0 \ll D_{\rm int}$ for all devices, thus ruling out the possibility that the drain–current degradation is due to the trapping of carriers in the existent states in the bulk of SiN. The values of $D_{\rm int}$ and α both increase

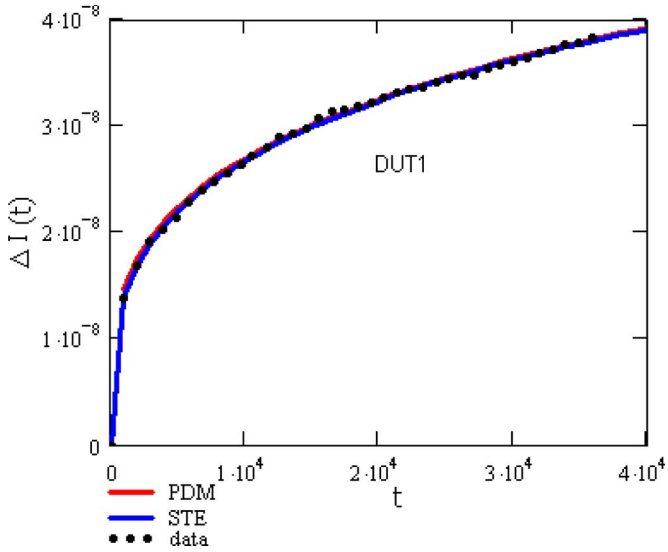

Fig. 7. Fitting the current trend after $3 \cdot 10^4$ s of the S+/R/S-/R experiment (conditions of experiment in Table II) in DUT 1 TFT. (Color version available online at http://ieeexplore.ieee.org.)

as the Si/N ratio increases, suggesting that the energy barrier between a-Si:H and SiN lowers as the Si/N ratio increases, and therefore, interface traps are easily filled with carriers from the a-Si:H channel. As previously shown in [14], α does not show a linear dependency on the stressing temperature, but it does show a strong dependency on stressing voltage, and these findings are in agreement with the results of Libsch.

All parameters used in the modeling, namely τ and β for STE and $D_{\rm int}$ and α for PDM, show a clear dependence on the Si/N ratio, suggesting that the rate of current decay or the trend could be influenced only by the gate insulator stoichiometry; e.g., DUT 1 with above-stoichiometric SiN has the most stable trend, whereas DUT 3 with substoichiometric SiN shows a severe decay in the current. This conclusion is supported by the literature, where it has been shown that the interface between a-Si:H and SiN has a high density of defects, resulting in significant band bending even when no stress is applied to the device [18]. The band bending is higher when a substoichiometric SiN or Si-rich SiN is used as a gate dielectric [19].

VI. Conclusion

A new experimental technique was proposed to explain the cause of drain–current $(I_{\rm sd})$ degradation in a-Si:H/SiN TFTs at room temperature and at low gate voltage stress.

The method of measuring $I_{\rm sd}$ is flexible and allows changes in the sequence of the applied bias stress and in the duration of each stress/relaxation period. By alternating the stress and relaxation, the drain–current degrades progressively, and its short- or long-term degradation is studied. The results of testing the drain–current in a-Si:H/SiN TFTs show that the degradation is due to a combined effect of charge trapping at the interface and interfacial defect creation. Our experiments show that the interface states in the insulator exchange charge with the channel. Although it is widely accepted that both defect creation and charge trapping mechanisms operate simultaneously, our experiments show clear evidence that these two mechanisms do not occur simultaneously but rather they act competitively; the prevalence of one upon the other being dependent on the sign of the applied voltage stress and the duration of experiment. It is the sign and magnitude of the gate voltage stress that determines whether either the defect creation of extra interface states or charge trapping in the switching states leads to the current degradation. When a negative voltage is applied, the charge detrapping influences the recovery of the current more than the removal of the defects. When a positive voltage is applied, the creation of extra interface defects is more important than the trapping of the carriers in the switching states. As the stress time increases, an amount of charge from the a-Si:H channel remains irreversibly trapped in SiN and affects the electric field at the interface. It might be possible that at very long stress times ($>$ 1 day), the defect creation becomes the dominant degradation mechanism that could further lead to device damage, but we believe that this is not the case in our experiments.

Our experiments on DUTs with different stoichiometry of the gate insulator show that the current degradation is related to the stoichiometry of the gate insulator. The degradation of the drain–current is more severe in the devices with Si-rich SiN (substoichiometric SiN) with bottom-gate TFTs than in N-rich SiN (above-stoichiometric SiN) with top-gate TFTs.

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