MOSFET Degradation Under RF Stress

Guido T. Sasse, *Student Member, IEEE*, Fred G. Kuper, and Jurriaan Schmitz, *Senior Member, IEEE*

***Abstract*—We report on the degradation of MOS transistors under RF stress. Hot-carrier degradation, negative-bias temperature instability, and gate dielectric breakdown are investigated. The findings are compared to established voltage- and field-driven models. The experimental results indicate that the existing models are well applicable into the gigahertz range to describe the degradation of MOS transistors in an RF circuit. The probability of gate dielectric breakdown appears to reduce rapidly at such high stress frequencies, increasing the design margin for RF power circuits.**

***Index Terms*—Breakdown, CMOS, device reliability, dielectric breakdown, dielectrics, hot-carrier degradation, negative-bias temperature instability (NBTI), reliability, RF, RF CMOS.**

I. Introduction

The understanding of MOS transistor degradation under use conditions is critical for supplying the market with reliable integrated circuits. Accelerated lifetime tests and degradation models have been successfully developed and applied for advanced CMOS. However, these models describe the performance evolution under dc or low-frequency stress and are typically verified up to ∼10 MHz. For use in RF circuits, the applicability of these degradation models under RF stress conditions should be known up to a few gigahertz. Some authors have compared dc stress conditions to ac conditions (see, e.g., [1]), but RF stress is only marginally addressed in literature.

This stems mainly from the difficulty to perform accurate reliability experiments at frequencies exceeding 10 MHz. Models describing MOS degradation under electrical (and thermal) stress are voltage or electric field based. Verification of these models at higher frequencies thus calls for the generation of well-defined RF voltage signals. In [2], we presented a method of generating well-defined RF voltage signals for on-wafer experiments. This method allows us to perform a large variety of different RF reliability experiments, without the need of designing test structures for every individual experiment. Only one generic test structure is required.

Using this technique, we were able to perform a large amount of experiments to compare the degradation of MOSFETs under RF stress conditions to degradation under ac stress conditions with frequencies below 10 MHz. In this paper, we will show results concerning hot-carrier degradation, negative-bias temperature instability (NBTI), and gate dielectric breakdown.

The following section will present the experimental approach in more detail. Then, the three degradation mechanisms are studied separately in Sections III–V. This paper concludes with recommendations for reliable RF CMOS design.

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G. T. Sasse is with NXP Semiconductors, Nijmegen, The Netherlands.

F. G. Kuper is with the Group of Semiconductor Components, MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands, and also with NXP Semiconductors, Nijmegen, The Netherlands.

J. Schmitz is with the Group of Semiconductor Components, MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands (e-mail: j.schmitz@utwente.nl).

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II. Methodology

The key idea of the methodology applied in this paper is to make use of sinusoidal-shaped voltage signals. The following are the benefits of using sinuses.

1) Stress conditions are comparable for all frequencies; therefore, duty cycle corrections are not needed.
2) Sinusoidal voltage signals are relatively easy to generate, thereby allowing the use of vector network analyzers (VNAs) to generate stress voltages.

A VNA is capable of measuring the power of the incoming and reflected waves in an RF measurement setup. If the absolute power level is also known, the voltage waveform at the device under test (DUT) can easily be determined.

In the methodology used in this paper, we connect the VNA in a one-port setup, thereby generating the desired voltage level at one of the signal pads of the DUT. In [2] and [3], we explained the necessary calibration steps that allow us to relate the measured power waves at the signal ports of the VNA to the voltage level at the DUT. The technique was then successfully applied to carry out charge pumping measurements at RF [3]. In the latter paper, we also presented experimental evidence for the accuracy of the voltage levels generated. In order to determine whether signal distortion due to the nonlinearities of the input impedance of the DUT is negligible, the expected voltage waveform can be calculated from the measured input impedance of the DUT over the entire voltage range of interest.

In digital CMOS, the duty cycle encountered in normal operation usually relaxes the degradation situation compared to worst case lifetime estimates. However, in RF circuits, voltage signals exceeding nominal supply voltage are no exception, particularly in power amplifiers (PAs) [4]. The reliability of these circuits therefore deserves special attention. This paper reports on hot-carrier degradation in nMOS transistors, on NBTI in pMOS transistors (NBTI is negligible in nMOS devices), and on gate dielectric breakdown on nMOS transistors. Due to their higher current-driving capabilities, nMOSFETs are preferred over pMOSFETs in RF PA design. For this reason, degradation is of most relevance in nMOSFETs.

We studied transistors from the 0.13-μm and 90-nm generations, with a heavily nitrided silicon dioxide as gate dielectric having equivalent oxide thicknesses of 2.1 and 1.6 nm, respectively.

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A Rohde & Schwarz ZVB20 VNA, generates the RF voltage. An HP4156A semiconductor parameter analyzer is used for dc biasing and measurements. All devices used were laid out in a ground–signal–ground configuration, optimized for RF measurements. The gate was connected to one signal pad, and the drain was connected to the other. The source was tied to the substrate and connected to the ground plane. The devices were connected on-wafer using Suss |Z| probes. The equipment was connected to a PC through an IEEE 488 bus. The measurement procedure was controlled using Labview software.

III. RF Hot-Carrier Degradation

A. DC and AC Models for Hot-Carrier Degradation

Hot-carrier degradation occurs in MOS transistors due to highly energetic charge carriers flowing in the MOSFET channel. The carriers cause physical damage and charge trapping, leading to a change of device parameters such as the threshold voltage. This effect has been widely discussed in literature (see, e.g., [5]). The effect can be observed in both nMOSFETs and pMOSFETs.

The hot-carrier degradation rate depends on the drain and gate voltages. For nMOSFETs with channel lengths $> 0.25\ \mu$m, hot-carrier degradation is severe in three different regions of gate bias voltage [6]. In more advanced devices with channel lengths below 0.25 μm, the maximum degradation rate shifts to high gate-voltage levels $(V_G \cong V_D)$, as experimentally demonstrated in [7].

The occurrence of different modes of hot-carrier degradation at different gate-voltage signals makes the lifetime prediction of ac and RF circuits challenging. In [8], a theoretical analysis is given of RF-to-dc lifetime ratios under such stressing conditions. When comparing ac hot-carrier degradation with dc degradation, Mistry and Doyle showed that use can be made of quasi-static assumptions [9]. The same work shows how all occurring hot-carrier degradation mechanisms can be considered to accumulate following a Matthiesen-like relation. No frequency dependence would be expected in that case.

Early reports indicating that ac hot-carrier degradation rises with increasing frequency were explained by Bellens *et al.* [10] as a measurement artifact. They showed that the self-inductance in the measurement cables can cause large voltage overshoots. This finding stresses the importance of generating well-defined voltage levels for performing ac reliability experiments. For ac hot-carrier experiments up to 10 MHz, this signal distortion due to cable inductance can be overcome by adding a large parallel capacitor to the drain [10]. For higher frequencies, additional effects such as signal distortion due to impedance mismatch come forward.

To circumvent these measurement issues, several research groups use integrated circuits to generate on-chip frequencies exceeding 100 MHz to stress a device [11]–[14]. These self-stressing structures typically contain oscillator and inverter circuits to generate on-chip high-frequency stress signals. Using these structures, hot-carrier experiments with inverter switching frequencies up to 369 MHz were already reported as early as 1994 [14]. None of these experiments revealed unexpected

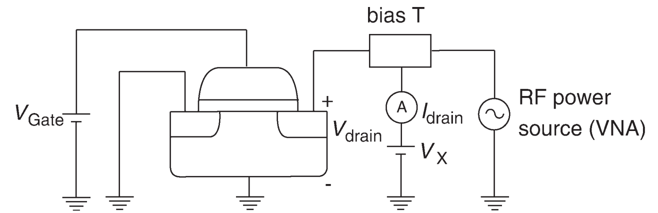

Fig. 1. Schematic drawing of the RF hot-carrier measurement setup.

effects occurring during ac stress. Presti *et al.* [15] recently showed hot-carrier degradation results for an nMOS transistor operating at 1.9 GHz. However, while effective for evaluating the given exemplary PA, the approach of Presti *et al.* prevents an accurate comparison with lower frequency signals.

When performing RF hot-carrier experiments, it is important to realize that the highest voltage signals occur at the drain side of the devices if the devices are used in PAs. We therefore investigate RF hot-carrier degradation with an alternating drain voltage while keeping the gate voltage constant. This is different from earlier ac hot-carrier experiments where the behavior of digital circuits was mimicked. For these experiments, an alternating gate voltage with constant drain voltage could better describe actual circuit behavior.

Of course, in real RF PAs, the gate voltage will not be perfectly constant, as otherwise no amplification of any RF signal would take place. This effect may be neglected to first order because the gate-voltage amplitude is relatively low combined with the fact that maximum damage occurs at maximum drain voltage.

B. Measurement Setup for Hot-Carrier Degradation

In Fig. 1, a schematic illustration of the measurement setup is shown. The instrument details are given in Section II. Measurements were performed on devices in two different technologies. The type A devices were 90-nm process devices, and the type B devices were fabricated in a 0.13-μm process. The type A devices have a channel length of 0.10 μm, and the total gate width is 120 μm, consisting of four identical cells, each having six gate fingers of 5 μm wide. The type B devices have a channel length of 0.13 μm. The total gate width is 192 μm, consisting of eight identical cells, each having eight gate fingers of 3 μm wide.

In the experiments, a dc voltage was applied to the gate, while an RF voltage was generated at the drain port. The devices are biased in inversion. This poses an extra difficulty in generating well-defined RF voltage signals: The impedance seen by the RF power source can become very low and has a strong dependence on the drain voltage.

It is important to guarantee that the hot-carrier degradation during stress cannot be attributed to the dc component of the stress signal. This can be guaranteed with a large-amplitude drain voltage. Very little degradation is then expected at the low part of the drain-voltage cycle, while fast degradation may occur when the drain voltage is high. This approach was verified by testing the dc hot-carrier degradation of same-type devices at several drain biases.

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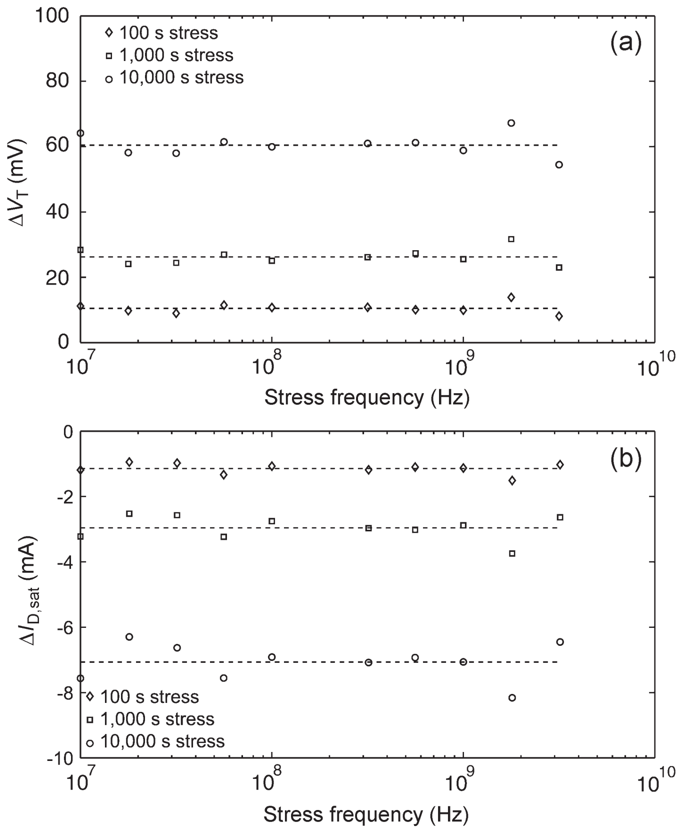

Fig. 2. Hot-carrier degradation of (top) V_T and (bottom) $I_{D,\mathrm{sat}}$ as a function of frequency for the type A devices. The drain-voltage signal is sinusoidal between 1.5 and 2.5 V. The gate voltage was 2.5 V during all stress measurements. Degradation levels are plotted after 100, 1000, and 10,000 s of stress. The dashed lines are meant as a guide to the eye.

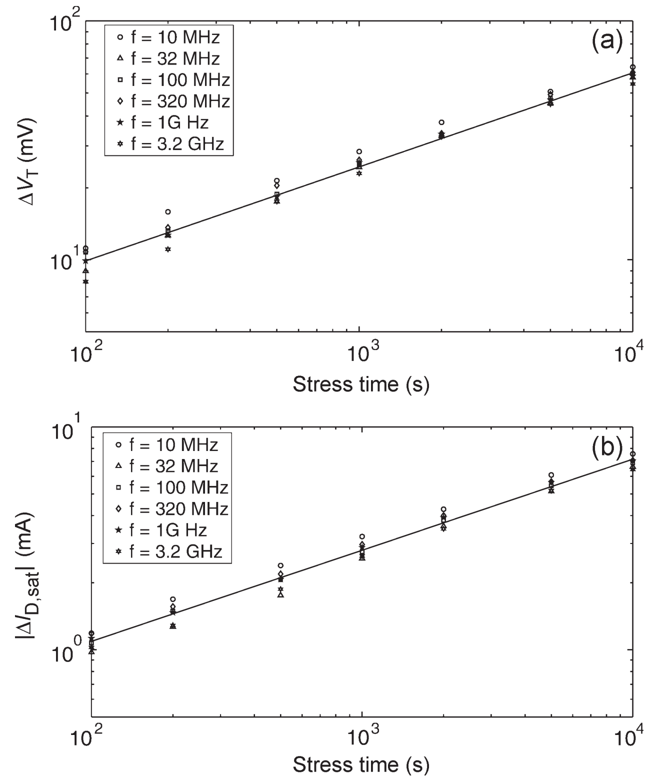

Fig. 3. Hot-carrier degradation as a function of time for the type A devices. The stress consisted of a constant gate voltage of 2.5 V, and the drain-voltage signal varied between 1.5 and 2.5 V. The frequency of the drain-voltage signal was varied. (a) V_T degradation. (b) $I_{D,\mathrm{sat}}$ degradation. The solid lines show the degradation as a function of time using the average time exponent of 0.41 and 0.39 for (a) and (b), respectively.

The drain-voltage amplitude is limited by harmonic distortion, originating because the impedance seen at the drain depends strongly on the drain voltage. Therefore, a signal integrity analysis, as discussed in Section II, was done before any RF hot-carrier experiment was performed, at the highest frequency used in the experiments, i.e., 3.2 GHz. The amplitude was kept low enough to keep harmonic distortion at a negligible level.

The bias conditions lead to a considerable dc drain current. Fig. 1 shows that the dc component of the drain voltage is set using V_X, which is connected to a bias tee. The bias tees used during the measurements were the internal bias tees of the VNA, connected at its dc biasing ports. This connection caused an extra parasitic series resistance of approximately 7 Ω. With dc drain currents flowing on the order of 100–300 mA, this may cause a dc voltage drop between V_X and V_{Drain} of 0.7–2.1 V. To account for this, we measure the dc relation between V_X and V_{Drain} prior to any measurement, and use this to apply a corrected V_X bias.

C. Hot-Carrier Measurement Results

In Fig. 2, device parameter degradation is shown against the frequency of the stress signal for the type A devices. The stress signal consisted of a dc gate voltage of 2.5 V, while the drain-voltage signal was sinusoidal between 1.5 and 2.5 V. The hot-carrier stress was periodically interrupted to measure V_T and $I_{D,\mathrm{sat}}$. V_T was obtained by measuring I_{Drain} as a function of V_{Gate}, with V_X being set to 0.1 V and using the maximum-derivative extrapolation method of Tsuno *et al.* [16]. $I_{D,\mathrm{sat}}$ was defined as the dc drain current, with V_{Gate} being set to 1.2 V and V_X being set to a value corresponding to a V_{Drain} of 1.2 V. Fig. 2 shows that between 10 MHz and 3.2 GHz, the frequency of the stress signal has no influence on device parameter degradation for the type A devices.

The results shown in Fig. 3 show the device parameter degradation as a function of stress time for the type A devices. The solid lines in Fig. 3 show the best fit over all data points assuming a power-law relation. For this technology, the values of time exponent n were found to be 0.41 and 0.39 for the average degradation in V_T and $I_{D,\mathrm{sat}}$, respectively. These values are typical for the time dependence of hot-carrier degradation.

Similar experiments were performed on the type B devices where the stress signal consisted of a gate voltage of 1.5 V and the drain-voltage signal varied sinusoidally between 1.0 and 2.6 V. The frequency was varied from 10 MHz to 3.2 GHz. Again, no frequency dependence is found, and the values of power-law time exponent were found to be 0.45 and 0.42 for V_T degradation and $I_{D,\mathrm{sat}}$ degradation, respectively.

From RF hot-carrier measurements on 90- and 130-nm nMOS transistors, we conclude that no frequency dependence exists in the amount of hot-carrier degradation, as monitored in V_T and $I_{D,\mathrm{sat}}$. This is in line with the existing physical models of hot-carrier degradation. The experimentally validated range

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of the existing models is as such extended with an order of magnitude, from the earlier 369 MHz [14] up to 3.2 GHz. This verification is very important for predicting circuit lifetime based on known voltage waveforms, such as the work presented in [8].

IV. RF NBTI DEGRADATION

A. DC and AC Models for NBTI

NBTI is a degradation mode of MOS transistors under negative gate stress at elevated temperatures. It leads mainly to a gradual threshold voltage shift, related to charge trapping in the gate dielectric. The phenomenon is recently reviewed [17]. It is more disturbing in pMOS than in nMOS transistors. Its characterization and modeling are troubled by recovery effects occurring directly after stress. The translation of dc to ac degradation is not straightforward due to these recovery effects.

Similar to hot-carrier degradation, NBTI parameter shift as a function of time follows a power law. Recent literature has revealed a typical value for the time exponent n of 0.16–0.17. This value can be obtained if parameter degradation is measured without removal of the stress signal, using, for instance, the on-the-fly technique of Huard *et al.* [18]. If recovery effects are not properly taken care of, like in conventional stress–measure–stress approaches, higher values of n around 0.25 may be found.

NBTI degradation under ac stress conditions has been discussed in various papers. Controversy exists on the presence of a frequency-dependent component in NBTI. Alam *et al.* [19] argue that on the basis of the reaction–diffusion model, no frequency dependence should be found. Other authors state that the recovery mechanism can be completely or partly be attributed to the detrapping of holes in deep oxide traps [18], [20]. Under this assumption, some frequency dependence may be expected.

Experimental results concerning ac NBTI degradation reflect a similar disagreement on the frequency dependence of ac NBTI degradation. Different papers show a clear frequency dependence of NBTI degradation [21]–[26]. It has also been claimed that only the formation of positive oxide charge contributes to any frequency dependence, while interface state generation is frequency independent [27]. Others have experienced no frequency dependence at all for ac NBTI degradation [28]–[30].

The frequency range discussed in these papers generally does not exceed the megahertz range. Only in [26] and [30] NBTI degradation under RF stress conditions is discussed. In [26], use is made of a ring oscillator circuit, and device parameter degradation is indirectly monitored using degradation in the oscillation frequency. The approach in [30], on the other hand, allows direct extraction of V_T shifts. In [30], no frequency dependence of NBTI degradation was reported in the entire frequency range from 1 Hz to 2 GHz. On the contrary, in [26], degradation at 100 MHz and 3 GHz was found to differ. In this section, additional experimental results will be presented that may shed more insight on any frequency dependence of NBTI under RF stress conditions.

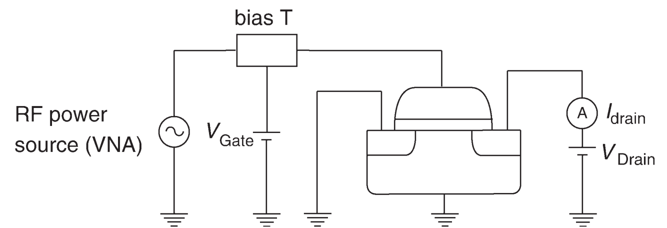

Fig. 4. Schematic drawing of the RF NBTI measurement setup.

B. Measurement Setup for NBTI

RF NBTI measurements were performed using the measurement setup, as shown in Fig. 4. The instrument details are given in Section II. RF voltage signals were superimposed on the dc voltage V_{Gate} through the use of a bias tee. During stress, V_{Drain} was set to 0 V.

Measurements were performed on pMOSFETs in two different technologies. The type C devices were processed in a 90-nm-node process, and the type D devices were pMOSFETs processes in a 0.13-μm process. The type C devices have a gate channel length of 0.10 μm, and the total gate width is 120 μm, consisting of 12 identical cells, each having one gate finger of 10 μm wide. The type D devices have a gate channel length of 0.13 μm, and the total gate width is 192 μm, consisting of eight identical cells, each having eight gate fingers of 3 μm wide.

RF NBTI measurements were performed using a stress–measure–stress procedure in which the sinusoidal stress voltage signal is periodically interrupted. V_T was obtained following [16] from a dc $I_{\mathrm{Drain}}-V_{\mathrm{Gate}}$ curve, with V_{Drain} being set to 0.1 V. The time delay between the removal of the stress signal and the start of the V_T measurement was 16 s. We avoided any prestress on the devices prior to the first V_T measurement in order to prevent any effect of the initial measurement on the extracted time exponent, as observed in [31] and [32]. For this purpose, the tuning process of setting the appropriate power level, as explained in [2], was performed on a separate device from the devices used for the stress experiments.

The chuck temperature used in the experiments was 125 °C. The stressing gate voltage V_{pp} was 3 V for the type C devices and 2.5 V for the type D devices. The dc bias V_{Gate} was -1.5 V for the type C devices and -1.25 V for the type D devices.

C. Measurement Results for NBTI

The frequency dependence of NBTI degradation is investigated in the frequency range from 10 MHz to 3.2 GHz. In Fig. 5, V_T degradation is shown against stress frequency for the type C and type D devices.

Although both figures show some spread on the data, a clear trend is visible: NBTI degradation has no observable frequency dependence. This observation is in agreement with the theory of Alam *et al.* [19] and the experimental results presented in [28]–[30].

The time dependence of NBTI degradation under RF stress is shown in Fig. 6 for the type C devices. The exponential time dependence reported before can be clearly recognized. The solid line shown in this figure is the average value of

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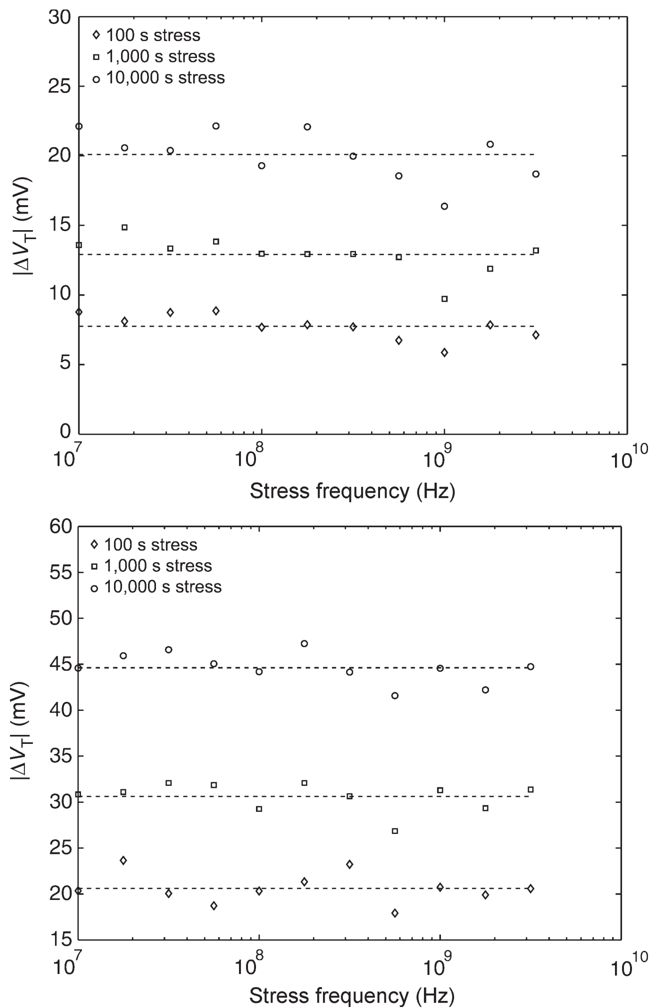

Fig. 5. (Top) V_T degradation plotted against the frequency for RF NBTI stress on the type C devices. The stress signal consisted of a constant gate voltage of -1.5 V superimposed on a sinusoidal voltage signal with $V_{\mathrm{pp}} = 3$ V. (Bottom) V_T degradation for the type D devices after RF NBTI stress. The gate stress is biased at -1.25 V superimposed on a sinusoidal voltage signal with $V_{\mathrm{pp}} = 2.5$ V. All measurements were performed at 125 °C. The dashed lines are drawn to guide the eye.

$|V_T|$ degradation over all frequencies. The time exponent for the measurements performed for the various frequencies varies randomly between 0.19 and 0.27. The average value of this time exponent was found to be 0.22. As a comparison, we also measured NBTI degradation after a dc stress by using the same stress–measure–stress procedure but without any RF component superimposed on this dc voltage. The gate voltage used for this experiment was set to -1.5 V. The time exponent found in this dc experiment was 0.24, with $|\Delta V_T|$ ranging from 1.1 mV (after 10 s) to 5.3 mV (after 10 000 s of stress). From these results, no significant difference in time exponent between dc NBTI and RF NBTI degradation can be observed.

Our results are obtained with sinusoidal waveforms. The NBTI degradation under other waveforms might prove to be very insightful. Generating these waveforms at frequencies exceeding 10 MHz might be cumbersome. Based on the observed frequency independence, it may suffice to perform these experiments below 10 MHz. These low-frequency data can then also be applied in describing RF NBTI degradation.

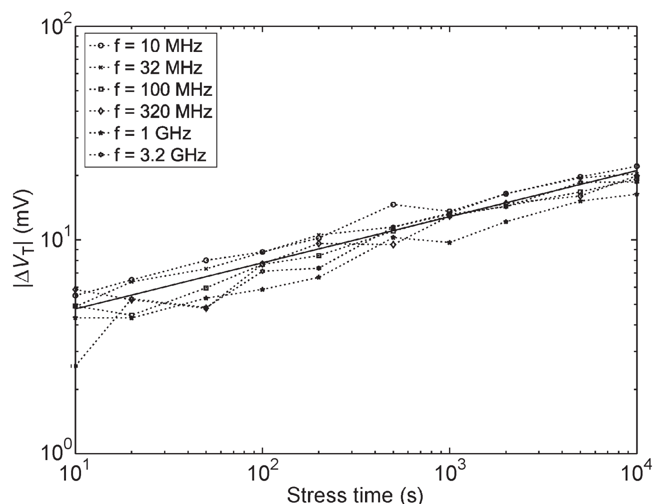

Fig. 6. V_T degradation as a function of stress time for the type C devices after an RF NBTI stress. The RF stress consisted of a sinusoidal dc gate voltage of -1.5 V superimposed on a sinusoidal voltage signal with V_{pp} of 3 V. This was done for various frequencies ranging from 10 MHz to 3.2 GHz. The measurements were performed at 125 °C. The solid line is a power-law fit yielding a time exponent of 0.22.

V. Gate Oxide Breakdown Under RF Stress

A. DC and AC Models for Oxide Breakdown

Gate oxide breakdown is the event of a sudden increase in the gate current when a high electric field is applied across the gate dielectric (or when a large current is forced through it). It is the manifestation of a conducting channel formed inside the gate dielectric. Dielectric breakdown is reviewed by Lombardo *et al.* [33]. In this section, oxide breakdown under RF stress conditions will be discussed.

Gate oxide breakdown is typically characterized using the time-to-breakdown t_{bd} measured in an accelerated test (with voltage or current stress being higher than real-life conditions). For devices with an oxide thickness below 5 nm, gate oxide breakdown is voltage driven [34]. The time-to-breakdown can be described using a power-law model [35]. For ultrathin oxide devices, t_{bd} can therefore be written as

$$t_{\mathrm{bd}} \propto V_G^{-m}. \tag{1}$$

In this expression, V_G is the gate voltage, and m is the power-law exponent. The reported m values are between 30 and 40. This expression reveals that a minor increase in the gate voltage may dramatically decrease device lifetime.

Lifetime enhancement under ac stress has been observed by several authors [36]–[41]. This effect is most pronounced under bipolar stress conditions. It has been attributed to frequency-dependent hole trapping kinetics and the detrapping of holes during zero- or negative-bias stress [38]. These experiments have only been reported with frequencies up to 10 MHz. In [4], oxide breakdown under RF stress conditions was investigated by designing RF PA circuits and recording t_{bd} values. The presented results revealed no difference in t_{bd} values between PAs operating at 80 MHz or 1.8 GHz. This approach very accurately mimics device operation under RF circuit conditions, but it is laborious to properly investigate any frequency

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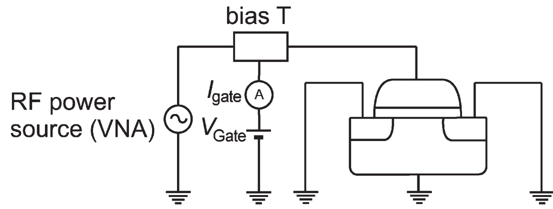

Fig. 7. Schematic drawing of the measurement setup used for RF oxide breakdown experiments.

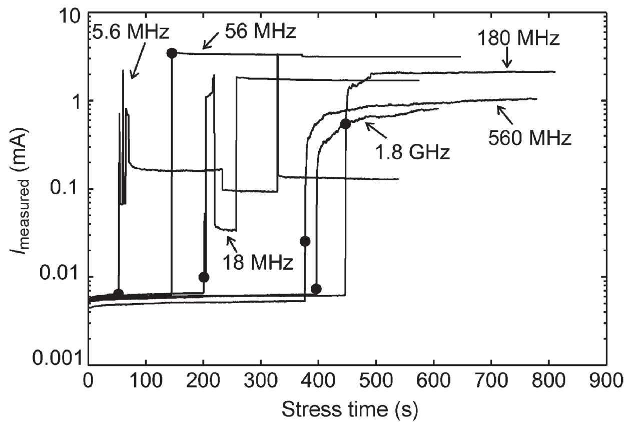

Fig. 8. Recorded I_{Gate} plotted against time. For each stress frequency, one typical example is shown. The big dots indicate the moment in time where breakdown is detected using the 5% definition.

dependence; in [4], only two stress frequencies were discussed. Our RF voltage generation approach enables the generation of equivalent voltage signals at different frequencies, allowing a more thorough investigation.

B. Oxide Breakdown Measurement Setup

RF breakdown experiments were performed on nMOS transistors using the measurement setup shown in Fig. 7. The devices were processed in a 0.13-μm process flow and have a gate channel length of 0.13 μm. The total gate width of the devices is 192 μm, consisting of eight identical cells, each having eight gate fingers of 3 μm wide.

During the experiments, the gate of the devices was stressed with a sinusoidal voltage signal. The peak-to-peak of the sinusoidal signal V_{pp} was set to 3.35 V, and the dc gate bias offset V_{Gate} was set to 1.675 V. During the experiments, the dc gate current I_{Gate} was monitored and used for the detection of breakdown events. Breakdown was defined as the time when a relative increase of $\geq$5% in I_{Gate} was found. The result of this definition is shown in Fig. 8, showing gate current versus time for typical samples with their identified breakdowns. Hard breakdown events are well identified on the given samples. Soft breakdown events may possibly be missed, but the use of the bias tee limits a more accurate measurement of I_{Gate}.

C. Oxide Breakdown Measurement Results

Measurements were performed with stress frequencies ranging from 5.6 MHz to 1.8 GHz. The measurements at 5.6 MHz were done with an Agilent 33250A signal generator that replaced the VNA. For every frequency, 20 samples were stressed, and the t_{bd} values were recorded. The samples used for the different frequencies were randomly distributed over the wafer.

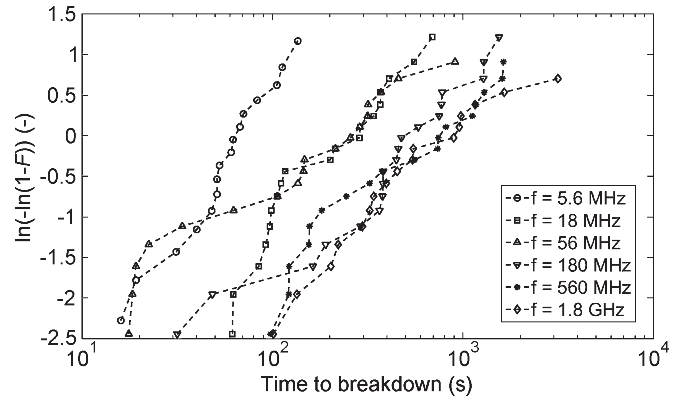

Fig. 9. Weibull plots showing the distribution of t_{bd} values for all measurement frequencies used.

In Fig. 9, the t_{bd} values are displayed in a Weibull plot for all stress frequencies. The figure reveals a gradual increase in the recorded t_{bd} values with increasing stress frequency. Fitting a monomodal Weibull distribution using the maximum-likelihood technique yields values for t_{63} (the time at which 63% of the devices have failed) and β (representing the slope of the distribution).

The fitted values of t_{63} and β are shown in Fig. 10. In this figure, a clear increase in t_{63} can be observed with increasing frequency. The corresponding value of β, on the other hand, does not show a clear trend. At the highest frequencies, it appears to remain relatively constant while it fluctuates more at lower frequencies. On the basis of the dielectric thickness (EOT $=$ 1.6 nm), a value around 1.1 is expected [42].

The lifetime enhancement is in accordance with earlier reported results at lower frequencies [36]–[41]. A striking difference with these earlier reported results is the relatively large increase in lifetime for unipolar stress signals. This (to our knowledge) has not been shown before. A possible explanation for this effect could be the increased importance of hole trapping kinetics for frequencies above 10 MHz rather than hole detrapping. This explanation is in line with the model presented in [38] where hole detrapping was regarded as the main cause of lifetime enhancement for bipolar stress signals. Hole trapping kinetics was considered a possible mechanism for lifetime enhancement for ac stress signals, but it could not explain the large difference between unipolar and bipolar stress signals. Furthermore, in [4], it was proposed that a dielectric relaxation time of 2–9 ns is needed for a trapped hole to create permanent damage. This means that if a stress signal is applied for a time shorter than this dielectric relaxation time, the stress becomes ineffective. With the use of sinusoidal stress voltages, it is to be expected that the maximum stress level (in terms of gate voltage) that is effective for creating damage decreases with increasing frequency. This is in line with our observations. Further studies are required to gain a complete understanding.

A lifetime increase of a factor of 14 can be observed between 5.6 MHz and 1.8 GHz. Taking $m = 35$ in (1), this would result in an increase in the allowable V_{pp} from, for instance,

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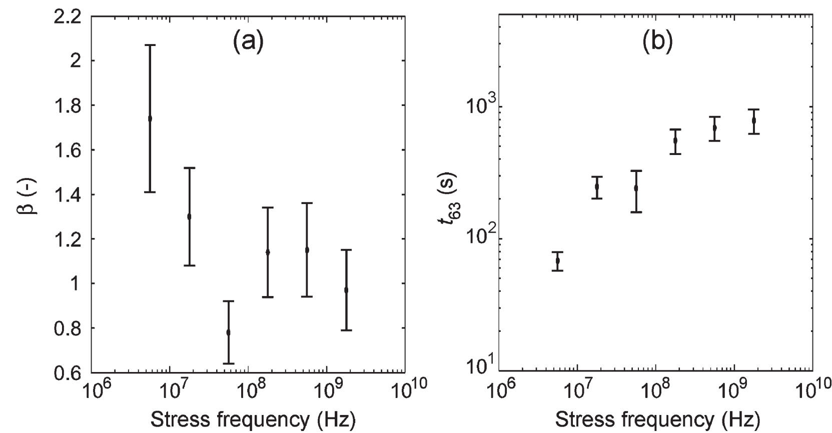

Fig. 10. Weibull parameters as obtained using a maximum-likelihood estimation. The parameters are plotted against stress frequency with the standard deviation of the likelihood function included. A clear increase in t_{63} can be observed as a function of frequency; β appears to remain constant.

1.2 to 1.28 V. This is an increase of 80 mV—or 10% headroom for an analog designer. Our results suggest that gate voltage constraints based on dc dielectric breakdown evaluations may be relaxed for RF CMOS applications.

VI. Conclusion

Using a previously reported RF voltage generation technique, the degradation of deep-submicrometer MOS transistors under RF stress is investigated. This technique allows the assessment of RF CMOS reliability for a variety of degradation modes, using one basic set of instruments and devices.

Hot-carrier stress on nMOS devices proves to follow existing models up to 3.2 GHz, while this was only confirmed up to 369 MHz until now. The hot-carrier degradation models are thus applicable for the reliability estimation of RF CMOS circuits.

RF NBTI experiments showed no considerable frequency dependence between 10 MHz and 3.2 GHz. Modeling of ac NBTI degradation is complicated by recovery effects; hence, no accurate models are available at present. Based on the observed frequency independence, it may, however, be sufficient to make use of ac NBTI experiments with frequencies below 10 MHz, making it easier to perform the necessary measurements for the development of accurate RF NBTI degradation models.

Dielectric breakdown measurements indicate a considerable frequency dependence, suggesting that increased headroom is available for RF CMOS design. This effect is known for bipolar stress, but has not been reported before on unipolar stress, which occurs more commonly in typical CMOS designs.

Existing models will give a conservative, but reasonably accurate, prediction of the reliability of RF CMOS circuits. Higher operating voltages may be allowed when the dominant failure mechanism is gate oxide breakdown. A technology-specific evaluation should be made to quantify the available headroom in order to offer designers the full potential of their technology.

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Guido T. Sasse (S'01) received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2003 and 2008, respectively.

He performed his Ph.D. research at the MESA+ Institute for Nanotechnology, University of Twente, where he studied RF CMOS reliability, reliability simulation, and the development of advanced CMOS characterization techniques. After obtaining his Ph.D. degree, he has been with NXP Semiconductors, Nijmegen, The Netherlands, as a Senior Reliability Engineer, where he continues to work on the topic of RF CMOS reliability.

Fred G. Kuper received the M.Sc. degree from the University of Twente, Enschede, The Netherlands, and the Ph.D. degree from the University of Groningen, Groningen, The Netherlands.

In 1987, he was with Philips Research to work on CMOS wafer-level reliability. In 1991, he moved to Philips Semiconductors, Nijmegen, The Netherlands, and broadened his scope to include ESD. In 1995, he became the Group Leader of the reliability group of a new 8" CMOS wafer fab. His scope currently includes product and nonvolatile reliability. In 2002, he became the Quality Manager of the automotive business line of Philips Semiconductors. Since 2008, he has been the Automotive Quality and Reliability Specialist of the Business Unit Automotive and Identification, NXP Semiconductors, Nijmegen, and has been an Extraordinary Professor with the University of Twente in the field of integrated circuit reliability.

Dr. Kuper has been a member of the technical program committees of various conferences, among which IEDM and IRPS. In 1996, he received the Outstanding Paper Award of IRPS for his paper on the relation between yield and reliability.

Jurriaan Schmitz (M'02–SM'06) received the M.Sc. (*cum laude*) degree in experimental physics from the University of Amsterdam, Amsterdam, The Netherlands, in 1990 and the Ph.D. degree in experimental physics from the same university in 1994.

He was then with Philips Research as a Senior Scientist, studying CMOS transistor scaling, characterization, and reliability. Since 2002, he has been a Full Professor with the University of Twente, Enschede, The Netherlands, where he currently heads the Group of Semiconductor Components, MESA+ Institute for Nanotechnology. He has authored or coauthored over 140 journal and conference papers and holds 16 U.S. patents.

Dr. Schmitz is or was a TPC member of the International Electron Device Meeting, the International Reliability Physics Symposium, and the European Solid-State Device Research Conference. He acted as the Technical Program Chair of the 2008 International Conference on Microelectronic Test Structures.

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