Estimation of the impact of electrostatic discharge on density of states in hydrogenated amorphous silicon thin-film transistors

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The objective of this letter is to give an estimation of the impact of an electrostatic discharge (ESD) stress on the density of states (DOS) within the energy gap of hydrogenated amorphous silicon (a-Si:H) thin-film transistors. ESD stresses were applied by means of a transmission line model tester. The DOS in the a-Si:H was determined by Suzuki's algorithm using field-effect conductance measurements. A comparison of stressed and unstressed devices shows that there is a threshold ESD stress voltage, below which there is no damage. Above the threshold stress level, first an increase of the deep gap states is found and when stress is increased further, also in the tail states. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1476394]

The hydrogenated amorphous silicon (a-Si:H) based thin-film transistor (TFT) is the dominant switching element in active matrix liquid crystal displays. As such, it is often subjected to an electrostatic discharge (ESD) stress. The worst effect of the ESD stress is a catastrophic breakdown, but it also can produce a "soft" prebreakdown degradation of the electrical characteristics. In this letter, the impact of the ESD stress on the gap density of states (DOS) of the a-Si:H TFT's is investigated. A field-effect based method for DOS determination, developed on the basis of a so-called incremental formula for sheet resistance, is applied to calculate the DOS in the upper part of the band gap before and after ESD stress.

The TFT's are grown in a standard plasma enhanced chemical vapor deposition system using amorphous silicon nitride as a gate insulator. The device has a top-gate staggered configuration. The intrinsic a-Si:H channel is 80 nm thick and the thickness of the silicon nitride layer is 350 nm. Samples with a variety of channel widths ($W = 4-100\ \mu$m) and lengths ($L = 4-100\ \mu$m) were measured and give consistent results. In order to apply ESD stresses, a transmission line model (TLM) setup is used (as shown in Fig. 1).[1] In contrast to the usual way of using a TLM system, due to the high resistivity of TFT's, the TLM ESD stress is a voltage stress instead of a current stress. We have used transmission line lengths in the range from 30 to 100 m, giving ESD pulses with durations ranging from 300 ns–1 μs. The stress pulse was applied on the drain, while the source and the gate were grounded (i.e., the common grounded gate configuration of a ESD protection device was tested). The positive stress voltage was stepped from 10 V up to breakdown. Negative voltages were not considered as some initial experimental results showed no difference between positive and negative stress voltage. The breakdown voltage varies with both the stress duration and the channel length in the range from 150 to 400 V.[2] Transfer characteristics are monitored before and after applying each ESD stress pulse. From each transfer characteristic, electrical parameters like threshold voltage and subthreshold slope are extracted. The main experimental results will be described only qualitatively. After applying an ESD stress higher than a certain "threshold of degradation" (~ 130 V), the threshold voltage starts to decrease and the subthreshold slope starts to increase. A more detailed description of the experimental results can be found in Ref. 2. The question is whether the origin of this deterioration of the transfer characteristics is due to the creation of the gap states in a-Si or due to charge trapping in the nitride. To answer this question, the density of band-gap states in the amorphous silicon is estimated from measured transfer characteristics.

An analytical method, which correlates the DOS within the energy band gap and field-effect conductivity measurements, was first proposed in the 1970's.[3] Since then, the method has been enhanced by many authors.[4–8] Powell[9] gave an overview of different variations of this method, and a discussion of the approximations introduced in them, such as constant space-charge density and zero-temperature statistics. It was shown that from field-effect conductance measurements only the broad features of the DOS can be determined and a unique DOS is not identifiable. Later on,[10] it was shown by Fortunato *et al.* that a class of methods called approximate methods of directly extracting the DOS[4,11] re-

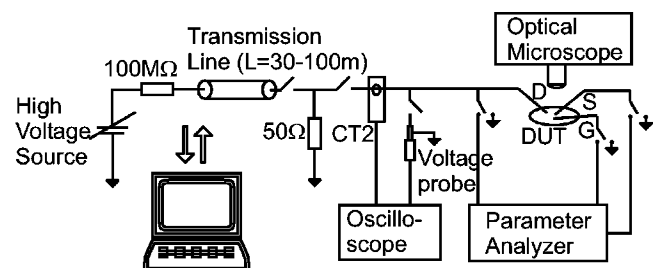

FIG. 1. TLM experimental setup.

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tain a reasonable degree of accuracy. In this letter, Suzuki's method is used[11] for an estimation of the DOS. The method will be described just briefly. An approximation of the relation between the gap states $N(E)$ and the band bending $u(x)$ is obtained using zero-temperature statistics and starting from the Poisson's equation

$$N(E_F+qu)=\frac{\varepsilon}{2}\frac{\partial^2}{\partial(qu_s)^2}\left[\frac{du}{dx}\bigg|_{x=0}\right]^2, \quad (1)$$

where x is the depth in the bulk of amorphous silicon, ϵ is dielectric constant of amorphous silicon, u_s is surface potential in the amorphous silicon, E_F is Fermi level, and q is elementary electron charge. The electric field is given by

$$\frac{du}{dx}\bigg|_{x=0}=-\frac{\varepsilon_{\text{diel}}}{\varepsilon}\frac{V_{\text{diel}}}{d_{\text{diel}}}=-\frac{\varepsilon_{\text{diel}}}{\varepsilon}\frac{V_G-V_{\text{FB}}}{d_{\text{diel}}}, \quad (2)$$

where $\varepsilon_{\text{diel}}$ represents the dielectric constant of the gate insulator and d_{diel} is its thickness. The voltage across the gate dielectric V_{diel} is expressed by the gate voltage V_G and the flat band voltage V_{FB}. Substituting Eq. (2) into Eq. (1), the gap density of states can be calculated if the relation between the gate voltage and the surface potential in the semiconductor is known. This relation is obtained from the measured sheet conductance $G=(I_{DS}/V_{DS})(1/W/L)$

$$\partial G=\frac{G_0}{q^2(V_G-V_{\text{FB}})}\frac{\varepsilon}{\varepsilon_{\text{diel}}}\frac{d_{\text{diel}}}{d}\left\{\exp\left(\frac{qu_s}{kT}\right)-1\right\}q\,\partial u_s. \quad (3)$$

This method can be validated in an original way by using Silvaco numerical simulator[12] as a reference: It is applied on a Silvaco's simulated transfer characteristic and the result is later compared with the DOS from the Silvaco's input file. In this way, the translation from DOS to transfer characteristics and the approximated reverse process can be compared. From this comparison, it is concluded that this method yields a correct result for the tail states but not for the deep states. In other words, some DOS parameters can be extracted from the calculated curve, such as the slope of the tail states distribution, the DOS at the conduction band edge and the position of the tail states peak. However, the deep states concentration is underestimated. The reason for that is that a zero-temperature approximation is used for the local space-charge density giving an error in the DOS around Fermi level, which is near the deep states. Zero-temperature approximation assumes that all DOS states are charged, and that is not the case for work at the finite temperature. The actual number of states is bigger than the number of charged states, which is extracted from the transfer characteristic. Another difficulty with field-effect based DOS calculations is that for calculating the DOS over the band gap, below, and above Fermi level, one must have both p-channel and n-channel data.[13] The problem is also that the range of energies within which the DOS is calculated is normally much smaller then the energy gap itself. In spite of these uncertainties, the model appears to be useful for a rough DOS estimation, especially if only a comparison of DOS before and after stressing is needed.

The calculation of the DOS from field-effect conductance measurements is very sensitive to the value of the flat band voltage. In our letter, the flat band voltage at the surface was defined as the gate voltage at which the onset of the field-effect conductance occurs,[11] as we assume that current conduction occurs in the very shallow layer at the amorphous silicon/silicon nitride interface. The flat band voltage at the interface is by definition the difference between metal work function (gate) and amorphous silicon work function in case when the energy bands further in the system are flat. However, it is known from the defect pool model that energy bands deep in the amorphous silicon are never flat.[6] Consequently, the "flat band voltage" at the interface is here defined as the difference between metal work function (gate) and amorphous silicon work function under the condition that the surface potential is equal to zero. If the surface potential is equal to zero, there are no surface charges and consequently the field-effect conductance is also equal to zero. When the gate voltage exceeds the flat band voltage, the surface potential increases, which means that current conduction sets in. In TFT's with silicon nitride as gate dielectric, the flat band voltage is negative assuming that there is no presence of fixed charges.

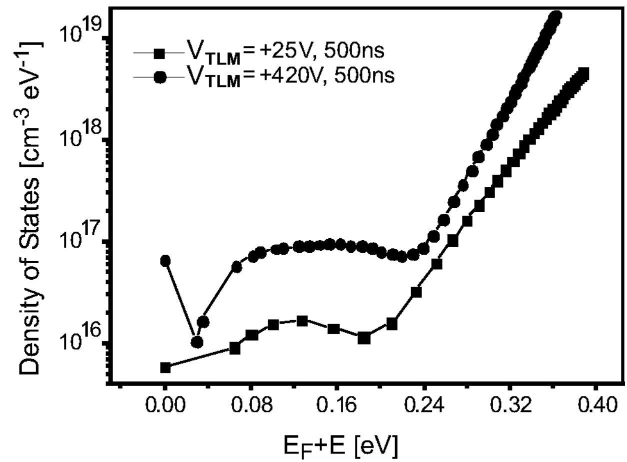

FIG. 2. DOS in the upper band gap calculated before and after ESD stressing (positive voltage on the drain $V_{\text{TLM}}=25$ V and 500 ns, and $V_{\text{TLM}}=420$ V and 500 ns).

In Fig. 2, the calculated DOS after an initial TLM pulse and the calculated DOS after a series of stepped 500 ns TLM stress pulse up to 420 V is plotted. Figure 2 shows the in-

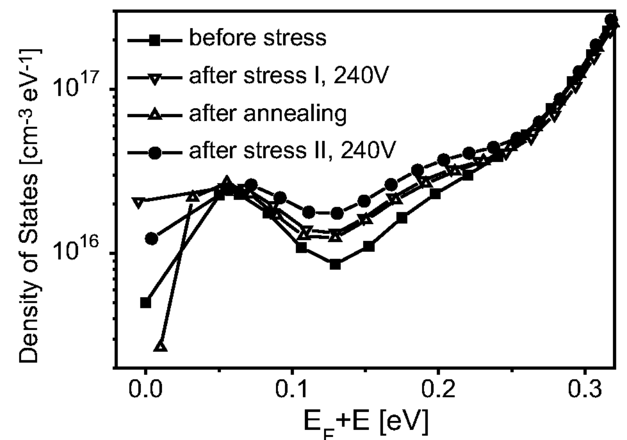

FIG. 3. DOS calculated in order to show the effect of annealing on the states created due to moderate ESD stress (positive voltage on the drain $V_{\text{TLM}}=240$ V and 500 ns).

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crease in the density of deep gap states and tail states in the upper part of the band gap after an ESD stress pulse on the drain, just one step before breakdown occurred. Therefore, it represents the largest change in the density of states. In contrast, in Fig. 3 the states created when the ESD stress just exceeds the stress threshold is presented. In Fig. 3, the calculated DOS after the initial TLM pulse is compared to the calculated DOS after a series of 500 ns TLM pulse up to 240 V. It can be noted that only the number of the deep states is slightly enhanced, whereas the number of tail states is not changed at all. Thus, it can be concluded that deep states are more sensitive to ESD stress then the tail states. Figure 3 also shows the DOS calculated after an annealing experiment. Next to the plots previously explained are two DOS curves calculated before and after another series of TLM stress (up to 240 V), repeated after an annealing cycle. The TFT is annealed in a vacuum at 250 °C for 2 h and cooled down in the air to room temperature without applying bias. Apparently annealing did not change the density of states.

It is shown in this letter that positive ESD stresses applied to the drain of a-Si:H TFT's can induce damage in the DOS of amorphous silicon already below catastrophic breakdown level assuming that the DOS is spatially homogenous. It appears that above a certain threshold ESD stress level, both the number of deep states as well as the number of tail states in the upper part of the band gap increases. The threshold level for deep states generation is lower than the threshold for tail states. The states created due to ESD stress could not be removed by annealing to 250 °C.

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