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Si–C Linked Organic Monolayers on Crystalline Silicon Surfaces as Alternative Gate Insulators

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Herein, the influence of silicon surface modification via Si–C_nH_{2n+1} (n=10,12,16,22) monolayer-based devices on p-type ⟨100⟩ and n-type ⟨100⟩ silicon is studied by forming MIS (metal–insulator–semiconductor) diodes using a mercury probe. From current density–voltage (J–V) and capacitance–voltage (C–V) measurements, the relevant parameters describing the electrical behavior of these diodes are derived, such as the diode ideality factor, the effective barrier height, the flatband voltage, the barrier height, the monolayer dielectric constant, the tunneling attenuation factor, and the fixed charge density (N_f). It is shown that the J–V behavior of our MIS structures could be precisely tuned via the monolayer thickness. The use of n-type silicon resulted in lower diode ideality factors as compared to p-type silicon. A similar flatband voltage, independent of monolayer thickness, was found, indicating similar properties for all silicon–monolayer interfaces. An exception was the C_{10}-based monolayer device on p-type silicon. Furthermore, low values of N_f were found for monolayers on p-type silicon ($\approx 6\times10^{11}$ cm^{-2}). These results suggest that Si–C linked monolayers on flat silicon may be a viable material for future electronic devices.

1. Introduction

The ongoing downscaling of metal-oxide semiconductor field-effect transistors (MOSFETs) in the semiconductor industry has strongly stimulated the research of both new insulating materials on silicon and well-controlled silicon–insulator interfaces. The demand for new insulators has divided the research into two categories. The demand for thinner gate oxides has driven the SiO_2 gate oxide thickness towards its fundamental limits,[1] which resulted in a search for a replacement of the thus far commonly used SiO_2 insulator by alternative materials with sometimes opposite, specific requirements. To decrease the leakage currents through the gate, a thicker insulator is required. Since at the same time the capacitance of the gate insulator needs to remain constant, this has resulted in an intensive search for materials with high dielectric constants or high-K dielectrics.[2]

Alternatively, the continuous downscaling of structural dimensions, leading to a higher density of interconnect lines and thinner insulating layers between them, has increased the capacitive coupling between the lines. Replacing the current SiO_2 insulating layer with, in this case, a low-K dielectric layer is imperative to lower this capacitive coupling, resulting in a quest for low-K dielectrics.[3]

One of the recently explored, new insulating materials on silicon are covalently bound organic monolayers. Various features of these monolayers, such as synthesis routes, comparison with monolayers on other surfaces, and electrical properties have already been investigated.

Two categories of other, well-known monolayers on silicon are self-assembled monolayers on oxidized silicon surfaces and those formed by the Langmuir–Blodgett technique. Modification and properties of these types of monolayers have been well studied so far.[4] The third category, organic alkyl monolayers covalently bound to oxide-free hydrogen-terminated silicon surfaces, has been under investigation for approximately ten years. Nevertheless, this research field has expanded dramatically since the first papers by Linford et al.[5] Different preparation methods have been developed,[5b,6] and the (nonelectrical) properties of these monolayers have been investigated and discussed in several reviews.[7]

From both a chemical and electrical point of view, passivation of the silicon surface via directly bound monolayers offers better possibilities as compared to other monolayer preparation techniques. The monolayers are bound via strong, covalent Si–C bonds, which provide a well-defined monolayer, shown to be stable in hot solvents, acids, and bases.[5b,7a] Thermal stability up to 615 K was observed under ultrahigh vacuum conditions.[8] The chemical, mechanical, and thermal stability of these types of layers is thus better as compared to monolayers on silica or gold, or monolayers prepared via the Langmuir–Blodgett method.[4,9] By the construction of metal–insulator–semiconductor (MIS) devices, the electrical behavior of organic monolayers prepared on silicon surfaces with a thin native oxide was studied by the groups of Vuillaume and Cahen.[10,11] They showed that the insulating properties of the

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native oxide were greatly improved by the organic monolayer, indicating the outstanding insulating properties of these layers. The Si–O-C bonds are, however, susceptible towards hydrolysis and are thermally labile.[5b,12] Additionally, the presence of a thin oxide layer makes it impossible to investigate the direct influence of the alkyl monolayer on the silicon surface properties.

Organic monolayers on oxide-free surfaces offer a promising alternative, owing to the formation of real monolayer–silicon interfaces and a well-defined surface morphology, and may serve as new insulating materials in molecular electronic devices. The fabrication method via "wet-bench chemistry" is relatively easy and cheap,[7a] as compared to insulators made under clean-room conditions. Moreover, the Si–C linked monolayer has a similar thickness as current state-of-the-art gate oxides, and has outstanding electrical properties, as has been explored in a number of studies. One example of such a device is, for instance, the MIS diode,[13] in which the monolayer acts as insulating barrier, and precisely tunes the desired current–voltage behavior.[14a–c] The influence of substrate doping on the quality of Si–$C_{18}H_{37}$|Al MIS-structures was recently investigated by Miramond and Vuillaume.[14d] They found that organic monolayers bound to heavily doped n-type (n^+) wafers showed a lower electrical performance as compared to similar monolayers on p^+-, p-, and n-doped wafers. Furthermore, Kar et al. focused on the insulating and passivation properties of these monolayers via the determination of the interface state density,[15a] while Sieval et al. and Webb and Lewis established this via lifetime measurements.[15b,c] Dielectric properties of such monolayers have been studied by Zhao and Uosaki using current sensing atomic force microscopy (AFM).[15d] They found a dielectric strength of 2.0 GV m^{-1} for alkyl monolayers on n-type ⟨111⟩ silicon. In a review by Salomon et al.,[16] current transport mechanisms through such thin monolayers (amongst others alkane thiols on gold and the system described herein) are discussed, and a comparison of electronic transport measurements on organic molecules has been made. More general examples of metal–monolayer–semiconductor devices and more complex molecular devices are described in the literature.[17]

The work of Liu and Yu comprises the characterization of n-Si|C_nH_{2n+1} (n=6,8,10, and 12)|Hg MIS structures;[14a] n-Si|$C_{12}H_{25}$|Hg MIS structures compared with n-Si|native oxide|Hg;[14b] p-Si|$C_{12}H_{25}$|Hg MIS structures compared with p-Si|native oxide|Hg, p-Si|native oxide-$SiO_3C_{12}H_{25}$|Hg and pSi-H|Hg.[14c] A study concerning thicker monolayers on oxide-free silicon surfaces is still absent, however. Herein, the focus is on Si|C_nH_{2n+1} (n=10,12,16, and 22)|Hg structures made on both n-type Si⟨100⟩ and p-type Si⟨100⟩, each with moderate doping (10^{15} cm^{-3}). From current density–voltage (*J–V*) and capacitance–voltage (*C–V*) measurements, the typical parameters describing the electrical behavior of such MIS diodes are derived using the thermionic emission theory. For the longer alkyl chains (n=16 and 22), a direct analysis from the *C–V* curves is possible resulting in an evaluation of the dielectric constant. Whether the electrical behavior for longer alkyl chains can still be precisely tuned as a function of the chain length is investigated. As a reference, we used both H-terminated samples and samples with a thin, thermally grown oxide of approximately 2 nm.

2. Theory

The Theory Section is divided into two parts. The current–voltage behavior is treated in Section 2.1, and the theory used to analyze the capacitance–voltage behavior is discussed in Section 2.2.

2.1. Current–Voltage Behavior

The commonly used transport mechanism that describes the *J–V* behavior of metal–very thin insulator (< 3.5 nm)–moderately doped silicon structures is the thermionic emission theory.[13] In this theory, the transport mechanism is governed by a thermionic emission process in which the electrons or holes tunnel directly through the insulator, as is generally the case for an insulator thickness < 3.5 nm. An expression for the *J–V* relation, in which the series resistance of the device under test does not play a role yet, is given in Equation (1) (for the metal positively biased with respect to n-type silicon):[13b]

$$J = J_0 e^{\left(\frac{qV}{nkT}\right)}\left(1 - e^{-\frac{qV}{kT}}\right) = A^* T^2 e^{\left(\frac{-q\phi_{eff}}{kT}\right)} e^{\left(\frac{qV}{nkT}\right)}\left(1 - e^{-\frac{qV}{kT}}\right) \qquad (1)$$

where J [A cm^{-2}] is the measured current density, V [V] is the applied bias voltage, A^* is the Richardson constant (110 and 32 A K^{-2} cm^{-2} for n-type and p-type silicon, respectively),[13a] T [K] is the absolute temperature, kT/q is the thermal voltage (25.7 mV at 298 K), and n is the diode ideality factor which accounts for the nonidealities in the diode behavior. In the ideal case, n=1. If the transport mechanism is not governed exclusively by a thermionic emission process, n>1. $q\phi_{eff}$ [eV] is the effective barrier height. In Figure 1 an energy band diagram of an n-type Si|insulator|metal structure is drawn to elucidate the formulas used throughout this section. Note that Figure 1 is not to scale and is displayed for illustrative purposes only.

For metal–(n-type) semiconductor junctions, the barrier height $q\phi_B$ is defined as: $q\phi_B = q\phi_M - q\chi$. $q\phi_M$ is the workfunction of the metal and $q\chi$ is the electron affinity of silicon (4.05 eV).[13a] In the case of a thin insulator, an extra barrier term is introduced, hereby increasing the total barrier height $q\phi_{eff}$. Selzer et al. and Liu and Yu expressed $q\phi_{eff}$ by Equation (2):[11d,14a–c]

$$q\phi_{eff} = q\phi_B + kT\beta l \qquad (2)$$

$kT\beta l$ [eV] describes the additional barrier height imposed by the thin insulator; β [Å^{-1}] is the tunneling constant, which is dependent—amongst other things—on the type of insulator and charge carrier (holes for p-Si or electrons for n-Si); l [Å] is the thickness of the insulator. We note that this β parameter, which is generally used to describe the efficiency of electronic tunneling through metal–organic monolayer–metal or semiconductor–organic monolayer–metal structures, normally

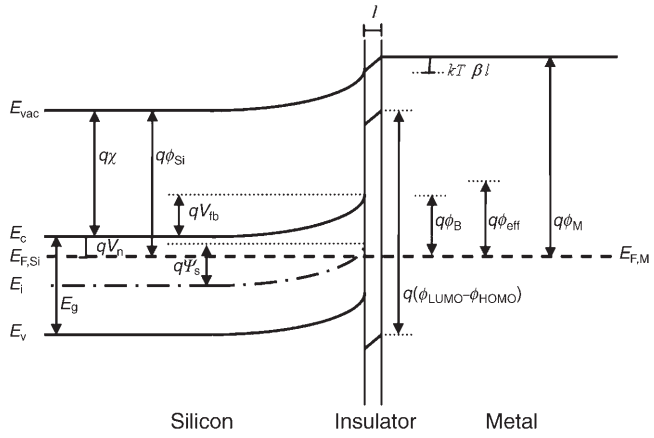

Figure 1. Simplified and ideal energy-band diagram of n-type silicon, covered with an interfacial thin insulating layer, in thermal equilibrium with a metal. E_{vac} = vacuum level; E_c = bottom of conduction band; E_v = top of valence band; E_g = bandgap of silicon; E_i = intrinsic Fermi level; $E_{F,Si}$ ($=q\phi_{Si}$) = Fermi level (workfunction) of silicon; $E_{F,M}$ ($=q\phi_M$) = Fermi level (workfunction) of metal; $q\chi$ = electron affinity of silicon, qV_n = energy difference between E_c and $E_{F,Si}$, $q\psi_s$ = energy difference between surface and bulk intrinsic Fermi level; ψ_s = surface potential; $q\phi_B$ = barrier height of metal–semiconductor junction; $q\phi_{eff}$ = effective barrier height, including the contribution of the interfacial layer; qV_{fb} = amount of band bending due to workfunction difference between silicon and metal at zero bias (ideal case); $q(\phi_{LUMO}-\phi_{HOMO})$ = energy difference between the lowest unoccupied molecular orbital and the highest occupied molecular orbital of the organic insulator.

shows a voltage dependency.[11d,16] This is not investigated herein, since our extraction method in the voltage range of 0 V to 0.2 V (n-type silicon) or 0 V to −0.2 V (p-type silicon) did not give rise to a strong bias dependence of β. Therefore, β determined for all samples modified with a monolayer is thus, in fact, an "effective" β, as compared to literature values, that take into account the voltage dependency.

Using Equation (1), $q\phi_{eff}$ and n can be derived. Rewriting Equation (1) into a function of $\ln(J/(1-e^{-qV/kT}))$ versus V results in Equation (3):

$$\ln\left(\frac{J}{\left(1-e^{-qV/kT}\right)}\right) = \ln(A^*T^2) - \frac{q\phi_{eff}}{kT} + \frac{qV}{nkT} \quad (3)$$

A plot of $\ln(J/(1-e^{-qV/kT}))$ versus V should give a straight line from zero bias.[13b] The ideality factor n can now be derived from the slope and the effective barrier height $q\phi_{eff}$ can be obtained via the $\ln(J/(1-e^{-qV/kT}))$-axis intercept.

For higher forward bias voltages, the series resistance R_s plays a role and Equation (1) can be adapted to Equation (4):

$$J = A^*T^2 e^{\left(\frac{-q\phi_{eff}}{kT}\right)} e^{\left(\frac{q(V-JR_s)}{nkT}\right)} \quad (4)$$

where R_s [$\Omega\,cm^2$] is the total series resistance of the device under test. One way to derive R_s from Equation (4) is via Equation (5):[13b,14c]

$$\frac{dV}{d\ln J} = JR_s + n\frac{kT}{q} \quad (5)$$

This plot should give a straight line from which the total series resistance R_s can be derived from the slope.

2.2. Capacitance–Voltage Behavior

2.2.1. Dielectric Properties of the Organic Monolayer

In ideal *C–V* measurements, the capacitance in accumulation equals the insulator capacitance, and hence the thickness or dielectric constant of the insulator can be calculated via the well-known formula: $C=\varepsilon_0\varepsilon_r A l^{-1}$, where ε_0 [$F\,cm^{-1}$] is the permittivity of vacuum, ε_r is the dielectric constant of the insulating layer, A [cm^2] is the surface area, and l [cm] is the insulator thickness. For a given thickness and area, the dielectric constant can be evaluated. In the case of thin insulators, however, the capacitance in accumulation often does not reach a constant value, which can be attributed—amongst other things—to a voltage-dependent accumulation capacitance in series with the insulator capacitance.

If this causes a tilted capacitance in the accumulation regime of the *C–V* curve, the series circuit can be written as Equation (6):[18]

$$\frac{1}{C} = \frac{1}{C_{ins}} + \frac{1}{C_s} = \frac{1}{C_{ins}} - \frac{2kT}{qC_{ins}}\frac{1}{(V_{bias}-V_{fb}-\psi_s)} \approx \frac{1}{C_{ins}} - \frac{2kT}{qC_{ins}}\frac{1}{(V_{bias}-V_{fb})} \quad (6)$$

where C_{ins} and C_s are the insulator and accumulation capacitance, respectively; V_{bias} and V_{fb} are the applied voltage and the flatband voltage, respectively; and ψ_s is the silicon surface potential (also indicated in Figure 1). $q\psi_s$ is the energy difference between the surface intrinsic Fermi level and the bulk intrinsic Fermi Level E_i. $\psi_s = 0$ V denotes the flatband condition. The flatband voltage can be determined from Mott–Schottky plots. Under strong accumulation conditions, $(V_{bias}-V_{fb}) \gg \psi_s$ and therefore ψ_s can be neglected. A plot of C^{-1} versus $(V_{bias}-V_{fb})^{-1}$ should then give a straight line with a C^{-1}-axis intercept of C_{ins}^{-1}. The dielectric constant can consequently be derived from C_{ins}.

2.2.2. Mott–Schottky Theory

The flatband voltage is a very important parameter in the analysis of metal–insulator–silicon structures, since it provides directly measurable, quantitative data on the silicon–insulator interface. The flatband voltage is usually derived from *C–V* curves. However, since *C–V* plots of thin insulators are often distorted, it is often difficult to obtain V_{fb} analytically. Fortunately, the Mott–Schottky relation provides a solution, since it only considers the silicon in the depletion regime. In this regime, the voltage drop over the thin insulator is considered negligible compared to the drop over the depletion layer, and the dominating depletion capacitance can be expressed in the Mott–Schottky form as given in Equation (7) (mercury positive-

ly biased with respect to n-type silicon):[13a]

$$\frac{1}{C_{sc}^2} = \frac{2(V_{fb} - V_{bias})}{q\varepsilon_0\varepsilon_r N_D A^2} \quad (7)$$

where C_{sc} [F] is the measured depletion capacitance; ε_r is now the dielectric constant of silicon and N_D [cm^{-3}] is the doping concentration. In the linear part of the C^{-2} versus V_{bias} plot, the doping N_D can be calculated from the slope and V_{fb} from the voltage-axis intercept.

Since V_{fb} is not influenced by the presence of a very thin insulator (only by the silicon–insulator interface properties), the barrier height $q\phi_B$ (see Figure 1) can be evaluated according to Equation (8) (for n-type silicon):[19]

$$q\phi_{B,n} = qV_{fb} + qV_n = qV_{fb} + kT\ln\left(\frac{N_C}{N_D}\right) \quad (8)$$

where qV_n is the energy difference between the bottom of the conduction band and the Fermi level of silicon (Figure 1); N_C is the number of effective states in the conduction band (2.8×10^{19} cm^{-3} for silicon),[13a] and N_D [cm^{-3}] is the silicon donor doping as calculated from Equation (7).

With the values for $q\phi_{eff}$ [Eq. (3)] and $q\phi_B$ [Eq. (8)], the barrier height $kT\beta I$ of the insulator [Eq. (2)] can be evaluated, and subsequently the tunneling constant β, if the insulator thickness is known. All parameters and their derivation routes mentioned in this section are summarized in Figure 2.

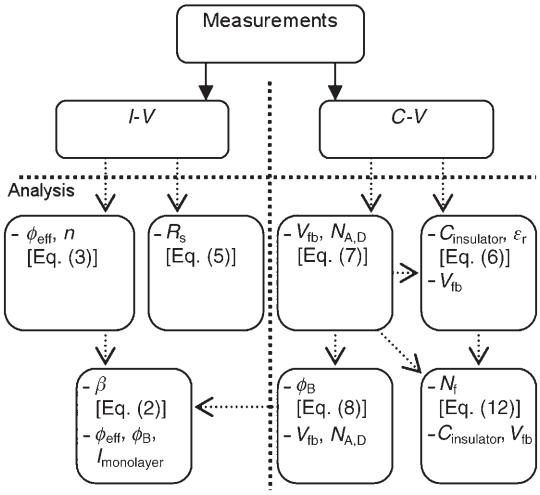

Figure 2. Parameter extraction route from *I–V* and *C–V* measurements. The analysis boxes show the parameter and the equation number, followed by any additional parameters needed from other extraction routes.

3. Results and Discussion

3.1. Mercury Area Verification

The area of the mercury contact on the samples was determined via high frequency *C–V* measurements on several p-type samples with approximately 100 nm thermal oxide (the exact oxide thickness *l* on each sample was separately measured by ellipsometry). An *I–V* measurement was performed before each *C–V* measurement, to make sure the oxide was not leaking. The leakage current of all the samples stayed well below 50 pA. From the measured capacitance in accumulation (see Figure 3), the area of the mercury drop was determined. A constant capacitance in accumulation equals the insulator capacitance and hence the area can be simply evaluated via: $C_{acc} = \varepsilon_0\varepsilon_r A l^{-1}$.[13a] Several spots on different samples gave for the area: $A = (3.7 \pm 0.1)\times10^{-3}$ cm^2.

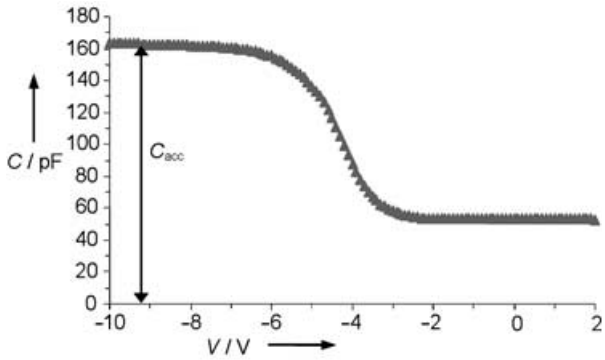

Figure 3. Typical example of a high-frequency capacitance–voltage plot of an Hg | SiO_2 (100 nm) | p-Si reference sample.

To investigate the wetting properties of the mercury on the contact area, the area determination was verified by testing samples with a 100 nm thick oxide hydrophobically coated with hexamethyldisilazane (HMDS), showing a static water contact angle of 84°. No significant changes in the calculated area were found. The influence of the wetting properties of the mercury is probably rather small, since the mercury is sucked against the insulator using a vacuum. Therefore, we have assumed a constant area in all our investigated samples. The determination of the silicon doping as shown in Table 3 supports this assumption, since the doping determination is very sensitive towards fluctuations in the area ($N_{A,D} \sim A^{-2}$ [Eq. (7)]) and the average doping values were all similar except for the $nSiO_2$ samples.

3.2. Current–Voltage Data

The average leakage current density *J–V* data for different insulators on p-type and n-type silicon samples are displayed in Figures 4 A and B, respectively. The curves shown for the C_{10}, C_{12}, C_{16}, and C_{22} monolayers and for bare hydrogen-terminated silicon and oxidized silicon are typical of at least five different junctions.

Starting with the hydrogen-terminated samples, it can be seen that there is an intrinsic difference in *J–V* behavior of mercury in contact with hydrogen-terminated n- or p-type silicon. This can be rationalized by considering the difference in barrier heights for a metal in contact with n- or p-type silicon. The ideal barrier height for n-type silicon is: $q\phi_B = q\phi_M - q\chi$ and for p-type silicon: $q\phi_B = E_g + q\chi - q\phi_M$.[13a] Using the literature value

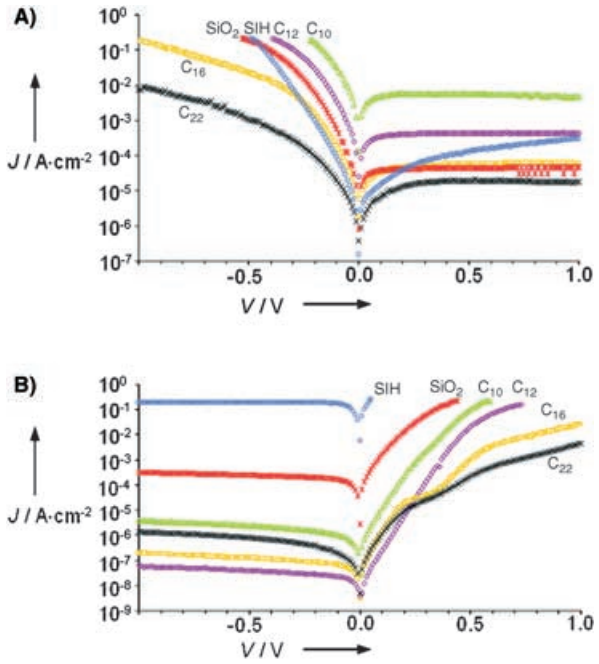

Figure 4. Current density versus bias voltage data for different insulators on A) p-type silicon (left side is accumulation, right side is depletion), and B) n-type silicon (left side is depletion, right side is accumulation).

of $q\phi_M = 4.49$ eV as the workfunction of mercury,[20] this results in $q\phi_{B,n} = 0.44$ eV and $q\phi_{B,p} = 0.67$ eV, that is, the workfunction of mercury is closer to the bottom of the conduction band than to the top of the valence band. This gives a huge difference in *J*–*V* behavior. As an example, the ideal J_0 (the diode reverse current density) for n- and p-type silicon is calculated via Equation (1). This gives: $J_{0,n} \approx 60\ A\,cm^{-2}$ and $J_{0,p} \approx 2 \times 10^{-3}\ A\,cm^{-2}$. Obviously, it concerns ideal values, since in real cases $q\phi_B$ is also influenced by surface states and imperfections in the (surface of the) silicon lattice,[13a] but nevertheless it gives a good indication in the expected difference in current densities. Mercury in contact with n-Si gives a very poor Schottky diode, or even an ohmic contact,[14a,21a,21b] while via mercury in close contact with p-type silicon, good Schottky diodes are obtained.[14c,21] This is in agreement with the data of Figure 4, where the nSiH samples show a much worse diode behavior than the pSiH samples. A distinct feature that can be seen immediately in Figure 4 A is the low current density measured for pSiH as compared to the pSi samples with different insulators. Several studies on mercury–silicon interfaces have been reported, in which it is shown that mercury forms an atomically flat contact to the silicon surface and that mercury does not chemically interact with the silicon.[21] This rules out the existence of any defects at the mercury interface, and indicates that the electronic behavior of these junctions is totally determined by the surface structure of the silicon and the number of defects at this surface. $q\phi_{B,p}$ values over 0.9 eV have been reported for mercury in contact with p-type ⟨111⟩ silicon.[21c,d]

Next, the influence of the 2 nm thick SiO_2 layer is discussed. It can be seen that passivating the p-type silicon surface with a thin oxide layer does not alter its *J*–*V* characteristics in a dramatic way. This behavior was observed before, on *I*–*V* measurements of mercury in close contact with hydrogen-terminated p-type silicon and with p-type silicon with an interfacial, chemically prepared oxide.[21b] The behavior is, however, more like a Schottky diode, since a more constant value of J_0 is now obtained in the reverse bias regime. An explanation for the high forward currents at the $pSiO_2$ samples may be the cancellation of the extra energy barrier introduced by the oxide as a result of additionally induced surface states at the silicon–SiO_2 interface. For the n-type silicon samples, passivation of the nSiH surface with a 2 nm oxide changes its *J*–*V* behavior dramatically. This is also reported in the literature, where a thin interfacial layer can change the behavior of mercury–n-type silicon structures from ohmic to Schottky contacts.[14a,21a,21b] Here, the oxide does provide an additional barrier that lowers the current density through the structure.

The effect of modifying p-type silicon surfaces with an organic monolayer on the *J*–*V* behavior is clearly visible. The *J*–*V* curves all have the same Schottky diode characteristic shape, indicating a similar transport mechanism through all alkyl insulators. The magnitude of the current density can be precisely tuned by varying the length of the 1-alkene, as was also observed by various other researchers via electrical means.[11d,14a,14c] Despite the fact that the C_{16} layer is thinner than the oxide layer (1.78 ± 0.02 nm versus 1.99 ± 0.06 nm) the organic monolayer displays better insulating behavior. This is a clear indication for the good insulating properties of these layers. As compared to the pSiH data, however, the MIS-structures formed with organic monolayers apparently also had net lower barrier heights, just as the oxide had. For layers $> C_{12}$, the current density values are lower than for pSiH.

The modifying n-type silicon surfaces with an organic monolayer displays a different trend. As compared to both the bare H-terminated and the oxidized samples, all monolayers clearly display better insulating properties. Even the thinnest monolayer under present study—C_{10} (1.21 nm)—insulates better than the $nSiO_2$ samples (layer thickness: 2.03 ± 0.11 nm). For the C_{10} and C_{12} monolayers, the *J*–*V* curves have their usual shape. Also, the trend in current density magnitude is in accordance with expectations. The C_{12} layer is a better insulator than the C_{10} layer.

The nC_{16} and nC_{22} samples, however, showed an unanticipated result. Two different regimes can be distinguished in the *J*–*V* plot of the n-type silicon data: $V < 0.4$ V and $V > 0.4$ V. In the first-mentioned regime—reverse and small forward bias voltages—the current densities of both the nC_{16} and nC_{22} layer are higher compared to the nC_{12} and nC_{16} layers. In other words, the order of *J* for the different monolayers on n-type silicon is $C_{10} > C_{22} > C_{16} > C_{12}$. This is—in contrast to the data of p-type silicon were we observed $C_{10} > C_{12} > C_{16} > C_{22}$—not in line with the monolayer thickness. For higher forward bias voltages (> 0.4 V), the insulating properties of the longer chains changed, and were more in line with the expectations. In this voltage regime, the series resistance of the monolayer starts to play a significant role [Eq. (4)], and this could be the reason for the strong current decrease that is observed.

Four possible reasons are now discussed to explain the observed *J–V* behavior of the nC_{16} and nC_{22} layer in the regime of $V < 0.4$ V. The first one is related to the presence of charges at the monolayer—silicon interface (for example, surface states). Effects arising from the silicon–monolayer interface, however, are believed to be of no significant influence on the shape of the *J–V* curves, since the delay time between voltage step and actual voltage measurement was 0.2 s, thereby excluding the effect of measuring a charging current due to interface states with short lifetimes.

The second explanation focuses on the properties of the monolayer, since a change in the geometry of the monolayers during the voltage scan could explain the observed, relatively high, current densities. The monolayer tilt angle dependency on current transport has been investigated by Yamamoto and Waldeck by investigating systems with a variety of alkane thiols on different semiconductor substrates.[22] They found an increase in tunneling current with increased tilt angle. If the C_{16} and C_{22} monolayers on n-type silicon are more tilted compared to C_{12} and C_{10} during the voltage scan, owing to (for instance) electrostatic interactions, this could explain the increase in tunneling current. However, a bias-voltage-induced tilting of monolayers $> C_{14}$ is in contrast with the findings of Selzer et al.[11d] They investigated current transport through alkane thiols on mercury in contact with oxidized p-type silicon and showed that only thinner ($< C_{14}$) layers are likely to tilt under applied bias voltages. Furthermore, for C_{12} and C_{16} layers on Si⟨100⟩, tilt angles of 26° have been reported,[30b] and also the reported value of the C_{22} layer (15–26°) is comparable.[30c]

The third explanation is related to the mechanism of the transport of current and can, to some degree, be associated with the aspect of geometry. Different mechanisms have been extensively treated in a review by Salomon et al.[16] In order to say something about the most likely current transport mechanism through the nC_{16} and nC_{22} layers, more detailed structural information of the used monolayers is required, such as the degree of packing and defects.

The fourth explanation for the deviating *J–V* results of nC_{16} and nC_{22} may be related to leakage currents. If pinholes are present, the mercury can directly contact the silicon surface. If this were the case, this would suggest that, in our study, thinner layers (nC_{10} and nC_{12}) were more densely packed than the thicker layers (nC_{16} and especially nC_{22}) and form blocking layers for the mercury.

To conclude, if the different *J–V* behavior of the nC_{16} and nC_{22} samples can be explained by deviating structural layer properties, as discussed in the last two explanations, the *J–V* data in its totality (both n-type and p-type) reveal different structural properties for C_{16} and C_{22} layers on n-type and p-type silicon. More research is needed to explore the observations of the *J–V* data.

Note that there is some parallel in the analysis presented below and the studies performed in the 1970s on metal-oxide–silicon structures with oxides of comparable thickness as the organic monolayers.[23] The analysis of the J–V plots starts by deriving the diode ideality factor *n* and effective barrier height $q\phi_{eff}$ [Eqs. (1) and (3)] from $\ln(J/(1-e^{-qV/kT}))$ versus *V* plots (Figure 5). In order to exclude any influence of the series resistance R_s, only the linear parts from 0 to 0.2 V (all samples on n-type silicon apart from nSiH, for which data from 0 to only 0.05 V was available) or 0 to −0.2 V (all samples on p-type silicon) were considered for this analysis.

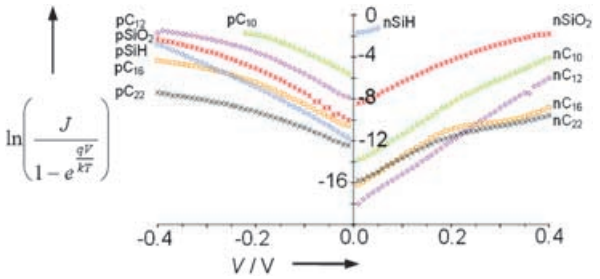

Figure 5. $\ln(J/(1-e^{-qV/kT}))$ versus *V* for all insulators. The plots on the left-hand side are for insulators on p-silicon. Plots for insulators on n-silicon are depicted on the right-hand side. The data is only displayed for the forward bias regime.

Subsequently, the series resistance R_s was derived from $dV/d\ln(J)$ versus *J* plots [Eqs. (4) and (5)]. The *J–V* data for $V > |0.2|$ V were used for analysis, to include the effects of the series resistance. This analysis was, however, not possible for C_{16} and C_{22} monolayers on n-type silicon, owing to the nonexponential behavior in the forward direction (see above). The results are given in Table 1.

The observed difference in ideality factor (*n*) for pSiH ($n = 1.49 \pm 0.05$) and nSiH ($n = 3.40 \pm 0.30$) can be explained by the different barrier heights (both $q\phi_{eff}$ and $q\phi_B$) for the two types of contact. Consequently, it can be concluded that mercury in contact with p-type silicon gives much better Schottky diodes compared to n-type silicon. A more qualitative examination of the diode quality factor for samples with modified surfaces can be given via Equation (9). In the case of an ideal metal–interfacial layer–silicon structure (that is, no surface states) the ideali-

Table 1. Parameters derived from thermionic emission theory.

insulator	*n*	$q\phi_{eff}$ [eV]	R_s [Ω cm^2]
pSiH	1.49 ± 0.05	0.695 ± 0.003	–
pC_{10}	1.78 ± 0.05	0.528 ± 0.002	0.49 ± 0.04
pC_{12}	1.57 ± 0.01	0.593 ± 0.001	0.99 ± 0.03
pC_{16}	1.69 ± 0.02	0.663 ± 0.001	4.14 ± 0.05
pC_{22}	2.16 ± 0.07	0.709 ± 0.002	22.84 ± 0.05
$pSiO_2$	1.43 ± 0.04	0.649 ± 0.007	1.31 ± 0.03
nSiH	3.40 ± 0.30	0.461 ± 0.003	–
nC_{10}	1.22 ± 0.07	0.806 ± 0.005	–
nC_{12}	1.34 ± 0.04	0.880 ± 0.003	–
nC_{16}	1.34 ± 0.02	0.837 ± 0.001	–
nC_{22}	1.63 ± 0.03	0.827 ± 0.002	–
$nSiO_2$	1.67 ± 0.07	0.644 ± 0.003	–

ty factor n is given by Equation (9):[23a]

$$n = 1 + \frac{l\varepsilon_{r,\mathrm{Si}}}{W\varepsilon_{r,\mathrm{insulator}}} \text{ with : } W = \sqrt{\frac{2\varepsilon_0\varepsilon_{r,Si}}{qN_\mathrm{D}(V_\mathrm{fb} - V_\mathrm{bias})}} \quad (9)$$

Two things can be noticed from this equation. Firstly, the ideality factor n increases with increasing length l of the insulator, that is, worse diodes are expected when the interfacial layer gets thicker. Secondly, n is dependent on the bias voltage. In Table 1, it can be noticed that n indeed increases with monolayer thickness, for both n- and p-type silicon, with the exception of pC_{10}, which shows a worse diode behavior than pC_{12} and pC_{16}. Modifying the pSiH surface with a thin oxide leads to a similar ideality factor, whereas modification of this surface with organic monolayers renders less good diodes in this case. This is in contrast with results reported by Liu and Yu, who obtained lower values for C_{12} layers on p-type $\langle 111 \rangle$ silicon (1.33 ± 0.10 versus 1.57 ± 0.01 in this case).[14c] A direct comparison is not possible, since n generally varies over the J–V range of a diode [Eq. (9)] and a different current regime and different method for the derivation of n were used in this study (see above). We used a low current regime for our analysis in which n is normally higher than for high forward currents. Modifying the nSiH surface with a thin oxide layer obviously leads already to a much better diode.[21a,b] All monolayers on nSi gave better diode ideality factors than the oxidized nSi samples. Another trend visible in Table 1 is that modifying n-type silicon surface with an organic monolayer renders a more ideal diode behavior as compared to p-type silicon.

The calculated effective barrier height $q\phi_{\mathrm{eff}}$ increases with increasing monolayer thickness on p-type silicon, which is in line with expectations [Eq. (2)]. Quite remarkable is the high $q\phi_{\mathrm{eff}}$ of the pSiH samples compared to the modified samples. This would indicate that the charge carriers have to cross a lower barrier for p-type silicon modified with an organic monolayer, as compared to pSiH junctions. On n-type silicon, however, the silicon surfaces with organic monolayers give higher barriers than nSiH and $nSiO_2$ samples. The calculated effective barrier heights of the monolayers are in line with observations in the J–V curves. The barrier height increases from nC_{10} to nC_{12}. Then it decreases for nC_{16} and nC_{22} but still remains larger than for $nSiO_2$. If the deviations for the longer alkyl chains are not caused by leakage of mercury through the layer, then the apparent lowering of $q\phi_{\mathrm{eff}}$ can have two origins according to the model used. Equation (2) shows that $q\phi_{\mathrm{eff}}$ depends on a barrier term that is a function of the monolayer thickness, and also on the barrier height $q\phi_\mathrm{B}$, which is influenced by the interface properties but not by the monolayer thickness. In the next section, $q\phi_\mathrm{B}$ and its possible influence on the observed $q\phi_{\mathrm{eff}}$ values are investigated.

The series resistance as calculated for p-type silicon samples shows a very clear exponential increase with monolayer thickness, as depicted in Figure 6. It must be noted, however, that there were only four data points in this analysis.

This exponential dependence of R_s on the monolayer thickness clearly indicates that the forward current at high bias voltages is not only influenced by the effective barrier height, $q\phi_{\mathrm{eff}}$ [Eq. (2)], but also by the length of the insulator path through which the charge carriers have to travel in the form of the series resistance R_s. Both $q\phi_{\mathrm{eff}}$ and R_s are influenced by the monolayer thickness. This also correlates to the trend seen in Figure 4A. The J–V plots of the pSiH samples have a much steeper slope until higher bias voltages than the pSi samples with insulators. This also indicates that the series resistance is mainly determined by the interfacial layer and not by the (back) contact resistance, since all samples on p-type silicon had the same back contact.

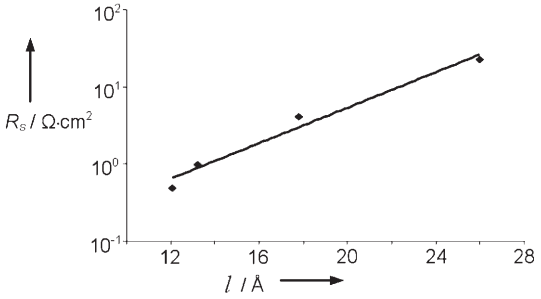

Figure 6. Series resistance as a function of monolayer thickness on p-type silicon. The exponential best-fit function is: $R_\mathrm{S} = 2.7 \times 10^{-2} e^{0.27l}$ ($R^2 = 0.973$).

3.3. Capacitance–Voltage Data

The results for the C–V measurements are depicted in Figure 7. The Figure shows typical curves from at least five different junctions.

The C–V curves for all H-terminated samples and samples with C_{10}, C_{12}, and SiO_2 insulators on both types of silicon are typical for metal–semiconductor junctions where the capacitance in accumulation increases sharply with the applied voltage.[13b] In contrast to $pSiO_2$, pC_{12}, pC_{16}, and pC_{22}, an additional peak at -0.2 V was observed for pC_{10}. The origin of this peak might be related to the presence of interface charges that are present at the silicon–monolayer interface of pC_{10}. In that case, the interface charge is contributing to the total charging current and consequently a peak appears in the C–V plot. The presence of a larger amount of interface charge at the pC_{10} sample correlates with the deviating flatband voltage for pC_{10} as compared to the flatband voltage for layers $> C_{10}$. A larger number of interface states may also be the cause of the higher diode ideality factor n of pC_{10} (1.78 ± 0.05) as compared to pC_{12} and pC_{16} (1.57 ± 0.01 and 1.69 ± 0.02, respectively), since a large number of interface states will lead to an increase in n.[23a] The C–V curves for samples with C_{16} and C_{22} insulators on both types of silicon display a plateau in the accumulation regime around $|1\text{ V}|$ and increase strongly again for higher voltages. This plateau indicates the formation of a real capacitance. The tilted capacitance in the plateau of the accumulation regime is further analyzed in the next section.

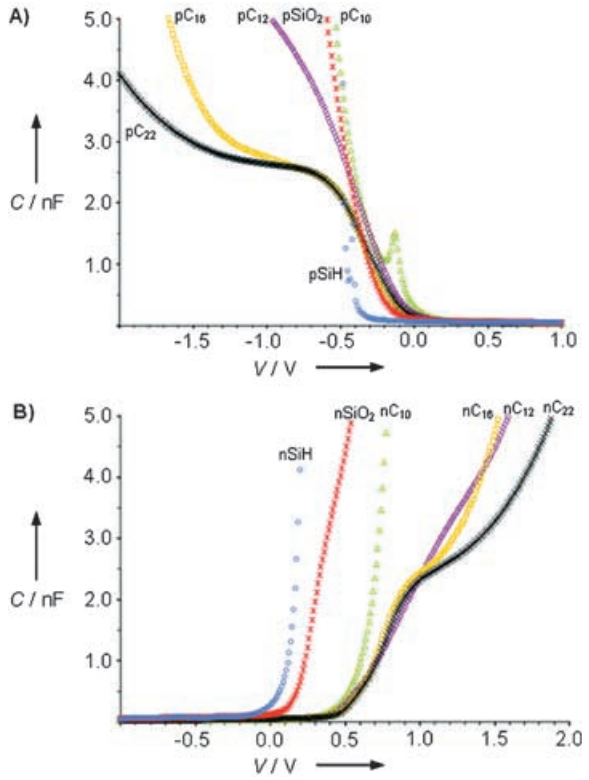

Figure 7. Capacitance–voltage plots of different insulators on A) p-type silicon and B) n-type silicon.

3.3.1. Dielectric Properties of the Organic Monolayer

At first it was verified whether the measured capacitance in the *C–V* curves displayed any frequency dependence. During the measurements, R_s was compensated for, to exclude frequency distortion in the *C–V* curve as a result of the series resistance. A frequency distortion can occur when measuring samples with a high series resistance while a parallel circuit of a capacitor and resistor is used as a *C–V* impedance model.[13b] Figure 8 gives the typical *C–V* curves for a pC_{22} sample measured at 10, 40, 100, and 400 kHz. No significant capacitance shift occurred in the accumulation regime at any of the samples.

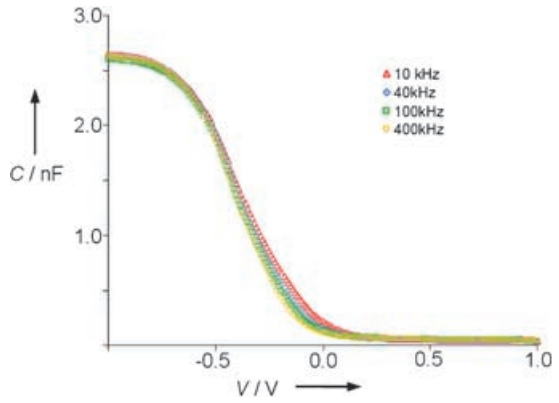

Figure 8. Capacitance–voltage curves of a $pSi|C_{22}H_{45}|Hg$ MIS structure at different frequencies. No frequency dispersion was observed in the accumulation regime.

Next, the *C–V* data measured at 400 kHz was used for analysis. A typical plot of C^{-1} versus $(V_{bias}-V_{fb})^{-1}$ for pC_{16} and pC_{22} samples is depicted in Figure 9. The linear extrapolation of the curve with the C^{-1} axis intercept yields the inverse insulator capacitance C_{ins}^{-1}, as can be seen from Equation (6).

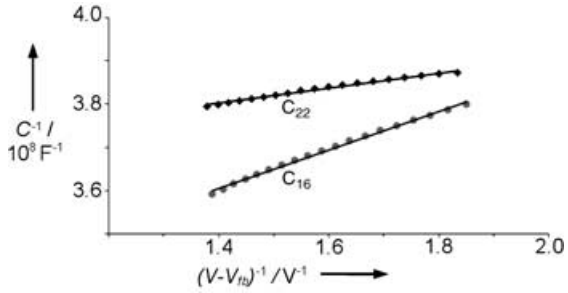

Figure 9. C^{-1} versus $(V-V_{fb})^{-1}$ plot for C_{22} and C_{16} insulators on p-type silicon.

With the thickness and area known, the dielectric constant can be graphically evaluated (Table 2).

Table 2. Dielectric constant for C_{16} and C_{22} monolayers.

Insulator	*C* [nF]	ε_r
pC_{16}	3.2 ± 0.2	1.7 ± 0.1
pC_{22}	2.8 ± 0.2	2.2 ± 0.2
nC_{16}	3.6 ± 0.2	1.9 ± 0.1
nC_{22}	3.5 ± 0.1	2.8 ± 0.1

These values are in close agreement with value $\varepsilon_r=2$ found for alkane thiol monolayers on mercury hanging drop electrodes and $\varepsilon_r=2.7\pm0.3$ for Hg–alkane thiol/alkane thiol–Hg junctions.[24a,b] Kar et al. reported a value of 2.13 for a C_{18} monolayer on $Al|C_{18}H_{37}|$p and n-Si devices,[15a] which is within the experimental error of the value for the pC_{22} samples (2.2 ± 0.2). The values are, however, much lower than the reported value of $\varepsilon_r=3.3\pm0.6$ from Yu et al.,[24c] apart from the nC_{22} samples. It is expected that a large amount of oxide would increase the effective dielectric constant, since $\varepsilon_r=3.9$ for SiO_2. This implies that there is more oxide present inside the C_{22} layers than the C_{16} layers, which could be an indication for the lower static water drop contact angles on these layers (100–102° for C_{22} and 108–109° for C_{16}). Also, the low water drop contact angles, $90.6\pm3.0°$ up to $101\pm7.5°$, combined with the high dielectric constant found in ref. [24c] are in line with these observations.

3.3.2. Mott–Schottky Measurements

The *C–V* data plotted in the Mott–Schottky form is given in Figure 10. The measurements shown here were performed at 400 kHz. The measurements were also carried out at 10, 40,

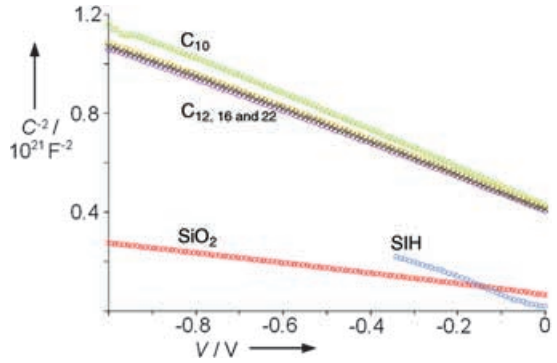

Figure 10. Mott–Schottky plots for different insulators on n-type silicon.

and 100 kHz to check whether there is a large frequency dependency on the calculated doping and flatband voltage. A frequency dependency in the Mott–Schottky plots is often encountered in electrochemistry on semiconductors, and can be attributed to numerous causes, such as—amongst others—surface states.[25] The calculated doping did not show any frequency dependency for all organic monolayers. The flatband voltage showed a maximum difference of 17% between 10 and 400 kHz for the C_{12} layer on p-type silicon. Flatband voltages compared between 10 and 400 kHz for the other monolayers showed a difference of less than 10%.

The plots are linear in the region -1.0 to $+0.2$ V for n-type silicon samples, except for the SiH samples, which gave deviations for voltages more negative than -0.35 V. The plots for the insulators on p-type silicon are all linear in the region $+1.0$ V to $+0.2$ V. The flatband voltage V_{fb} and doping density were calculated using Equation (7), and the barrier height $q\phi_B$ was calculated using Equation (8). Hereafter, the barrier term $kT\beta I$ from the insulator was calculated via Equation (2). The results are given in Table 3. The theoretical flatband voltage for ideal cases is shown in the third column, for comparison.

Table 3. Parameters derived from the Mott–Schottky analysis.

insulator	V_{fb} [V]	$V_{fb,theory}$ [V]	Doping [10^{15} cm^{-3}]	$q\phi_B$ [eV]	$kT\beta I$ [eV]
pSiH	-0.58 ± 0.01	-0.45	2.0 ± 0.1	0.80 ± 0.01	–
pC_{10}	-0.22 ± 0.01	-0.45	2.2 ± 0.1	0.44 ± 0.01	0.09 ± 0.01
pC_{12}	-0.34 ± 0.03	-0.45	2.3 ± 0.2	0.56 ± 0.03	0.04 ± 0.03
pC_{16}	-0.34 ± 0.02	-0.45	2.0 ± 0.1	0.56 ± 0.02	0.10 ± 0.02
pC_{22}	-0.32 ± 0.04	-0.45	2.1 ± 0.2	0.53 ± 0.04	0.18 ± 0.04
$pSiO_2$	-0.36 ± 0.01	-0.45	1.9 ± 0.1	0.58 ± 0.01	0.07 ± 0.01
nSiH	0.05 ± 0.03	0.18	1.6 ± 0.2	0.30 ± 0.03	–
nC_{10}	0.61 ± 0.01	0.18	1.2 ± 0.1	0.87 ± 0.01	-0.06 ± 0.01
nC_{12}	0.63 ± 0.02	0.18	1.3 ± 0.1	0.88 ± 0.02	0.00 ± 0.02
nC_{16}	0.63 ± 0.01	0.18	1.3 ± 0.1	0.89 ± 0.01	-0.05 ± 0.01
nC_{22}	0.63 ± 0.01	0.18	1.3 ± 0.1	0.88 ± 0.01	-0.06 ± 0.01
$nSiO_2$	0.34 ± 0.01	0.18	2.9 ± 0.1	0.58 ± 0.01	0.07 ± 0.01

The flatband voltages for C_{12}, C_{16}, and C_{22} layers on p-type silicon and for all the organic monolayers on n-type silicon are in close agreement with each other. This indicates that the properties of the silicon–monolayer interfaces are influenced in a similar way for all these monolayers. A similar flatband voltage for different monolayer thickness was also noticed by Yu et al. and Bansal and Lewis, who observed this in their electrochemical experiments on n-type ⟨111⟩Si electrodes covered with organic monolayers.[26] They ascribed such independence of V_{fb} towards monolayer thickness to the neutral character of an adsorbate bound to the silicon surface involving covalent Si–C bonds. The deviating flatband voltage for the pC_{10} sample indicates a change in surface properties, which correlates with the deviating value of n and the peaks in the C–V curve (Figure 7A) for pC_{10}.

All the calculated doping levels are in line with the specifications given by the wafer supplier (p-type silicon: 1.4×10^{15} cm$^{-3}\leq N_A\leq2.8\times10^{15}$ cm^{-3} and n-type silicon: 4.3×10^{14} cm$^{-3}\leq N_D\leq4.3\times10^{15}$ cm^{-3}). The doping levels for all pSi samples were similar, whereas for the nSi samples, $nSiO_2$ gave an N_D twice as high as the other nSi samples. The calculated doping results indicate that the area of the mercury dot was not influenced strongly by the wetting properties of the different surfaces, since the doping $N_{A,D}$ scales with A^{-2}, as can be seen from Equation (7).

Regarding the barrier height, it is noticed that $q\phi_B$ for pSiH is very high (0.80 ± 0.01 eV) as compared to theory (0.67 eV). $q\phi_B$ values over 0.9 eV have been reported for Hg–pSiH junctions.[21c,d] The barrier height for the nSiH sample (0.30 ± 0.03 eV) is lower than expected (0.44 eV). A validity of the used method, however, is the fact that for a given combination of a metal and semiconductor, the barrier heights for both (n-type) semiconductor–metal and (p-type) semiconductor–metal junctions are related according to: $q\phi_{B,n}+q\phi_{B,p}=E_g$, where E_g is the semiconductor bandgap energy (for silicon $E_g=1.12$ eV).[13a] For the Hg–SiH junctions measured in this study, this results in: $q\phi_{B,n}+q\phi_{B,p}=1.10\pm0.03$ eV, which is in perfect agreement with theory. The results for pC_{12} and pSiH samples are in close agreement with the results obtained by Liu and Yu.[14c] The results showed a similar $q\phi_B$ for the n-type samples modified with an organic monolayer. This is in line with the assumption that the low values of $q\phi_{eff}$ for nC_{16} and nC_{22} (Table 1) are not caused by a difference in interface properties for these layers as compared to the thinner layers.

3.4. Evaluation of Insulator Properties, Effective Barrier Height, and Tunneling Constant

Table 3 gives the calculated values for the barrier $kT\beta I$ imposed by the insulators. These values are far too low, or even negative, compared to the values found in the literature of 0.16 eV for ⟨111⟩ nSi-$C_{10}H_{21}$ samples,[14b] and 0.24 eV for ⟨111⟩ pSi-$C_{12}H_{25}$ samples.[14c] In the following discussion about the $q\phi_{eff}$ and $q\phi_B$ values, it is as-

sumed that a theory normally applied to silicon surfaces covered with thin oxide layers is also applicable to these silicon junctions with organic monolayers.[23a] This is rationalized by the fact that the current transport mechanisms through both types of insulators are equal, and both insulators are densely packed structures. Regarding Equation (2), a number of things can be said about $q\phi_{eff}$. First, in ideal cases (that is, the silicon surface structure is not changed by contact with the insulator) the barrier height $q\phi_B$ determined for modified samples should be equal to the barrier height $q\phi_B$ of SiH samples. Second, $q\phi_B$ and $q\phi_{eff}$ for SiH samples should be equal, since they contain no contribution from an insulating layer. This was also noticed by Liu and Yu who attributed such deviations to fixed charges located at the silicon–insulator interface.[14c] Since mercury forms an atomically flat and chemically stable contact, it is expected to form an ideal contact with the insulator;[21] so all fixed charges should be located at the silicon–insulator interface. The fixed charge at Si–SiO_2 systems often originates from ionic silicon near the interface. Together with incomplete silicon bonds (for example, Si–Si or Si–O bonds) at the surface, they may result in a fixed charge Q_f. For Si–SiO_2 systems, Q_f is usually positive.[13a]

In order to give an analysis of the fixed charge, a comparison is needed with the ideal flatband voltage. In an ideal metal–semiconductor interface, the flatband voltage is given by Equation (10):

$$qV_{fb} = q\phi_M - q\phi_{Si} = q\phi_{MSi} \quad (10)$$

The silicon workfunction $q\phi_{Si}$ is dopant dependent, and for n-type silicon is given by Equation (11)[13a,27]:

$$q\phi_{Si} = q\chi + qV_n = q\chi + kT\ln\left(\frac{N_C}{N_D}\right) \quad (11)$$

where N_C is the number of effective states in the conductance band (2.8×10^{19} cm^{-3} for silicon).[13a] Using the average value of $N_D = 1.2\times10^{15}$ cm^{-3} and $q\phi_M = 4.49$ eV for mercury,[20] this gives $V_{fb,theory} = \phi_{MSi,n} = 0.18$ V for n-type silicon. In a similar way, using $N_A = 2.0\times10^{15}$ cm^{-3}, it can be calculated that for p-type silicon $V_{fb,theory} = \phi_{MSi,p} = -0.45$ V.[27]

Positive charges in the insulator will shift ideal *C*–*V* and Mott–Schottky curves to more negative values, resulting in a more negative V_{fb}, and vice versa. If these theoretical values are compared with the measured values (see Table 3), the following can be said about p-type silicon. The hydrogen-terminated sample has a more negative value of V_{fb}, indicating the presence of positive charges at the Hg|SiH interface. All the insulators, however, have their flatband voltage shifted in the positive direction, even beyond the theoretical V_{fb}, indicating the presence of negative charges at these interfaces. The number of negative charges is the largest for pC_{10}, followed by the oxidized samples and then comparable values for the other monolayers. For n-type silicon, the hydrogen-terminated samples also have a more negative value of V_{fb}, indicating the presence of positive charges at the Hg|SiH interface. All the other insulators again have their flatband voltage shifted in the positive direction beyond the theoretical V_{fb}, indicating the presence of negative charges at these interfaces. The $nSiO_2$ samples now give a lower number of fixed charges.

From a comparison between the measured and ideal flatband voltage, the total fixed charge at the C_{16} and C_{22} layers can be estimated via Equation (12):

$$N_f = \frac{C_{ins}(\phi_{MSi} - V_{fb})}{qA} \quad (12)$$

where N_f [cm^{-2}] is the total number of fixed charges; C_{ins} [F] is the insulator capacitance as determined from the C^{-1} versus $(V-V_{fb})^{-1}$ plots; ϕ_{MSi} and V_{fb} are the theoretical and measured flatband voltages, respectively. This gives the values of N_f in Table 4. By definition, however, $N_f = |Q_f q^{-1}|$, and is always positive. To show that in all the cases listed in Table 4 the fixed charges are negative, this is denoted by $-Q_f$.

Table 4. N_f calculated for different monolayers.

Insulator	Total insulator charge N_f [cm^{-2}]
pC_{16}	$(5.8\pm1.0)\times10^{11}$ $(-Q_f)$
pC_{22}	$(6.2\pm2.0)\times10^{11}$ $(-Q_f)$
nC_{16}	$(2.7\pm0.2)\times10^{12}$ $(-Q_f)$
nC_{22}	$(2.7\pm0.1)\times10^{12}$ $(-Q_f)$

State-of-the-art MOS-structures have values of N_f of the order of 10^9–10^{11} cm^{-2} for ⟨100⟩ oriented silicon.[28] The samples with monolayers on p-type silicon have a remarkably low amount of fixed charge, especially if one takes into account that these monolayers were fabricated using wet-bench chemistry at low temperatures, as compared to temperatures that are used in the fabrication of MOS-structures. A distinct influence of dopant type on the amount of fixed charge can be observed in this case. The number of fixed charges in the n-type silicon samples is more than four times higher than in the p-type silicon samples. Another type of interface charge from which the physical origin is suggested to be similar to Q_f is the interface trapped charge, or surface states charge Q_{it}.[28] Kar et al. studied the density of these interface traps (D_{it}) at p- and n-type Al|$C_{18}H_{37}$|Si structures and found also a substantially higher value of D_{it} at n-silicon structures compared to p-type silicon structures.[15a] They attributed this to the influence of the silicon surface potential and the position of the surface Fermi level during monolayer formation.

Next, the J–V data can be compensated for the shift in V_{fb} due to fixed charge in the samples.[23a] The influence of the fixed charge can be eliminated by multiplying Equation (1) with a normalization factor $e^{-\frac{kT}{q}(V_fb-\phi_{MSi})}$ and re-plotting the normalized *J*–*V* graphs. From these, the normalized effective barrier heights can be calculated. The results with normalized values for $q\phi_{eff}$ and the β values can be found in Table 5 (see Figure 2 for derivation routes; $q\phi_{eff}$ is derived from the *J*–*V* curves and $q\phi_B$ is derived from the *C*–*V* measurements). β is ex-

Table 5. Results of the barrier-height analysis via normalized *J–V* plots.

insulator	$q\phi_{eff}$ [eV]	$q\phi_B$ [eV]	$KT\beta I$ [eV]	β [Å^{-1}]	β [per CH_2 group]
pSiH	0.563 ± 0.003	0.80 ± 0.01	−0.24 ± 0.01	–	–
pC_{10}	0.751 ± 0.001	0.44 ± 0.01	0.31 ± 0.01	1.00 ± 0.05	1.21 ± 0.06
pC_{12}	0.701 ± 0.001	0.56 ± 0.03	0.15 ± 0.03	0.43 ± 0.09	0.47 ± 0.10
pC_{16}	0.771 ± 0.001	0.56 ± 0.02	0.21 ± 0.02	0.46 ± 0.04	0.52 ± 0.04
pC_{22}	0.840 ± 0.001	0.53 ± 0.04	0.31 ± 0.04	0.46 ± 0.06	0.54 ± 0.07
$pSiO_2$	0.739 ± 0.002	0.58 ± 0.01	0.16 ± 0.01	–	–
nSiH	0.324 ± 0.001	0.30 ± 0.03	0.03 ± 0.03	–	–
nC_{10}	1.230 ± 0.006	0.87 ± 0.01	0.37 ± 0.01	1.18 ± 0.04	1.42 ± 0.04
nC_{12}	1.330 ± 0.003	0.88 ± 0.02	0.44 ± 0.02	1.30 ± 0.06	1.43 ± 0.06
nC_{16}	1.290 ± 0.001	0.89 ± 0.01	0.40 ± 0.01	0.87 ± 0.02	0.97 ± 0.02
nC_{22}	1.270 ± 0.002	0.88 ± 0.01	0.39 ± 0.01	0.58 ± 0.02	0.69 ± 0.02
$nSiO_2$	0.801 ± 0.003	0.58 ± 0.01	0.23 ± 0.01	–	–

pressed in two different units in order to facilitate comparison with the values reported in the literature.

It can be seen that the normalized values for the effective barrier height $q\phi_{eff}$ are much higher as compared to Table 3. Especially for the n-type samples with the higher amount of fixed charge, a very large increase in effective barrier height was obtained. Starting with the comparison of the values of $q\phi_{eff}$ and $q\phi_B$ for the SiH samples, it can be seen that for the nSiH sample $q\phi_{eff}$ and $q\phi_B$ are similar. The pSiH samples, however, showed a deviation between these two values. The extra barrier term introduced by the SiO_2 was for p-type silicon of the same order as the C_{12} layer, whereas, for n-type silicon, the monolayers yielded much higher barriers. This indicates the good insulating properties of the organic monolayers on n-type silicon.

While discussing the β parameter, it must be recalled that the samples with deviating behavior were pC_{10} (high diode ideality factor, shifted V_{fb}), and nC_{16} and nC_{22} (deviating *J–V* curves). When establishing a general view of the behavior of a monolayer on n- and p-type silicon, they are treated as exceptions. Table 5 shows that a larger dependency is found for electron tunneling than for hole tunneling. This has also been found in the literature, where hole tunneling is thought to be a more efficient process than electron tunneling.[11d,16] Theoretical values mentioned for hole and electron tunneling through alkyl layers are 0.4–0.8 Å^{-1} and 0.8–1.0 Å^{-1}, respectively.[11d] In the literature, β has been derived for many different metal–monolayer–metal or metal–monolayer–semiconductor systems and the β values all lie in the above-mentioned range.[16,29] Apart from pC_{10}, all p-type samples modified with an organic monolayer gave low β values. Such low values indicate that hole tunneling through these layers is very efficient.[11d,16] β values determined for nC_{10} and nC_{12} samples, however, are very high, indicating that electrons do not tunnel efficiently through these layers on n-type silicon. Such high values have not been reported before in the literature. β values for the nC_{16} and nC_{22} samples are much lower, which is the result that $q\phi_{eff}$ for these samples was derived from already deviating *J–V* curves.

β can also be determined via an alternative route. Plotting $q\phi_{eff}$ versus the monolayer thickness leads to a graphical determination of β via Equation (2). This was done for the monolayers on p-type silicon. This method presumes that $q\phi_B$ is equal for all samples. pC_{10} was not included in this analysis, given its deviating value of $q\phi_B$. The n-type samples were also not analyzed in this way, since nC_{16} and nC_{22} both showed deviating behavior. Figure 11 shows the two graphs of $q\phi_{eff}$ derived from the non-normalized *J–V* plots ($q\phi_{eff1}$) and normalized *J–V* plots ($q\phi_{eff2}$).

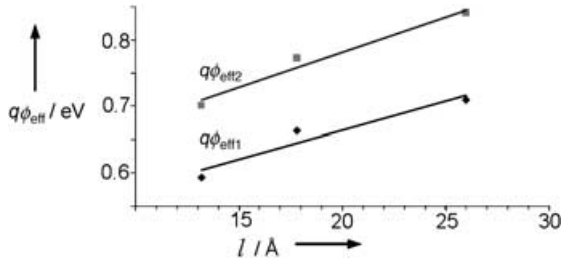

Figure 11. $q\phi_{eff}$ versus monolayer thickness for $q\phi_{eff1}$ and $q\phi_{eff2}$.

From these data, the following values for β were calculated using Equation (2): $\beta_1 = 0.34 \pm 0.10$ Å^{-1} using the $q\phi_{eff1}$ values, and $\beta_2 = 0.41 \pm 0.07$ Å^{-1} using the $q\phi_{eff2}$ values. Repeating this analysis for $q\phi_{eff}$ versus the thickness expressed as the number of carbon atoms gives: $\beta_1 = 0.44 \pm 0.11$ per CH_2-group and $\beta_2 = 0.53 \pm 0.07$ per CH_2-group. The latter results exclude any errors made in the monolayer thickness determination. β_2 is in close agreement with the values derived in Table 5. It can be seen that this method is very sensitive towards differences in the silicon–monolayer interface structure ($q\phi_B$) between the samples, which, if not taken into account, may have led to an underestimation of the β parameter in this case.

4. Conclusions

Organic monolayers covalently bound to p- and n-type silicon were successfully characterized via *J–V* and *C–V* measurements and the results were compared with H-terminated samples and samples with 2 nm SiO_2. It was demonstrated that all layers showed insulating behavior and behaved as Schottky diodes. All monolayers on n-type silicon and monolayers $> C_{12}$ on p-type silicon showed better insulating properties than silicon oxide.

Results from *J–V* measurements for p-silicon samples showed that the effective barrier height $q\phi_{eff}$ increased clearly as a function of monolayer thickness. Not only was the effective barrier height affected by the chain length, but also the series resistance R_s was strongly affected in an exponential way. Samples of n-type silicon modified with alkyl monolayers did not display this clear dependence. It was found that $q\phi_{eff}$

increased for nC_{10} and nC_{12} as compared to nSiH and $nSiO_2$, but a decrease was found for the longer chains. An unambiguous explanation for this phenomenon cannot yet be given; further investigation is necessary. Organic alkyl monolayers on n-type silicon form more ideal diodes than these monolayers on p-type silicon.

Results from *C–V* measurements showed typical metal–semiconductor *C–V* behavior for SiH, SiO_2, C_{10}, and C_{12} covered silicon. For C_{16} and C_{22} layers, a plateau in accumulation was observed, and this indicated the formation of a real capacitance. Analysis of this plateau yielded the dielectric constant, which varied from 1.7 ± 0.1 to 2.8 ± 0.2. Mott–Schottky analysis gave similar values for the flatband voltage for different chain lengths, apart from pC_{10} samples. This suggests similar interface properties for all investigated monolayers other than pC_{10}. For the C_{16} and C_{22} layers, the amount of fixed charge was evaluated. This gave remarkably low values of fixed charge density for monolayers on p-type silicon ($\approx 6 \times 10^{11}$ cm^{-2}), as compared to samples on n-type silicon ($\approx 3 \times 10^{12}$ cm^{-2}). Evaluation of the tunneling constant β gave higher values for n-type silicon, $\beta = 0.58$–1.30 Å^{-1}, as compared to p-type silicon, $\beta = 0.43$–0.46 Å^{-1}, excluding the pC_{10} samples. This confirms that holes tunnel more efficiently than electrons.

From the above results, we conclude that from an electronic point of view, organic monolayers covalently bound to silicon offer a promising insulating and passivating material for molecular electronic devices. Moreover, given the numerous possibilities for chemical modification of the properties of the organic monolayers and the formation of true silicon–molecule interfaces, we believe that such layers are very promising for future nanodimensioned silicon devices.

Experimental Section

Materials: Silicon ⟨100⟩ 4-inch wafers (p-type: 5–10 Ω cm and n-type: 1–10 Ω cm) from Okmetic, Finland were used. PE 40/60, ethanol, and CH_2Cl_2 were distilled prior to use. Mesitylene (Fluka, 99%) was distilled and dried over $CaCl_2$. The dried mesitylene was filtered to remove traces of $CaCl_2$. 1-Decene (Fluka, 97%), 1-dodecene (Aldrich, 95%), and 1-hexadecene (Sigma, ≈99%) were distilled twice under reduced pressure. 1-Docosene (TCI, 99+%), acetone (Acros, 99+%), and n-hexane (Acros, 99+%) were used as received. HF (Fluka, 50% p.a.-plus) was diluted with demineralized H_2O. Nitrogen was dehydrated over KOH and H_2SO_4, consecutively. Mercury (Merck, 99.9999% Suprapur) was used as received. HMDS (Merck, VLSI grade) and photoresist (OLIN 907/12) (Fuji Foto Film) were used as received.

Sample Preparation: A number of wafers, both n- and p-type, were thermally oxidized with two different oxide thicknesses. The first batch had a target thickness of approximately 100 nm thermal oxide, and was made to determine and verify the area of the mercury dot (batch 1). The second batch had a target thickness of a few nanometers and was made to check the insulating properties of SiO_2 insulators with a similar thickness as the monolayer (batch 2). The wafers of both batches were first cleaned using standard wafer cleaning (5 min in 100% HNO_3, copious rinsing in demineralized water, 10 min. in boiling (69%) HNO_3 at 95 °C and again copious rinsing in demineralized water). Just prior to oxidation, the wafers received an HF dip (1%) and were again rinsed in demineralized water and spun dry. The wafers of batch 1 were oxidized in a Tempress Oven using a dry oxidation process in an O_2/N_2 mixture, and a subsequent annealing step in an N_2 atmosphere. The wafers of batch 2 were inserted via the automatic transport rail into the same Tempress Oven, which was kept at a constant temperature of 700 °C. After the wafer carrier was completely inserted, it was immediately driven outward again. In this way, a very thin SiO_2 layer of approximately 2 nm was thermally grown. Before oxidation, the oven was cleaned with a *trans*-LC (*trans*-1,2-dichloroethylene) cleaning procedure. After oxidation, the oxide thickness was measured with ellipsometry. Finally, these oxidized samples were rinsed with hexane before measurements to remove any organic contaminants.

Back Contact Fabrication and Dicing: Before back contact manufacturing, wafers without thermal oxide underwent the standard cleaning as described above, and the front side was subsequently covered with HMDS and photoresist. The wafers were then prebaked at 120 °C for 30 min. A similar procedure was used for oxidized wafers, except that they were processed without cleaning after removal from the oven. Then the wafers received a 1% HF dip to remove the native oxide from the backside. A metal contact was made to the wafer via sputtering. On n-type wafers, an interfacial layer of 50 nm Ti/W alloy was deposited before a 1000 nm layer aluminum was sputtered. This Ti/W layer lowered the ohmic resistance of the contact. On p-type wafers, a 1000 nm aluminum layer was directly sputtered. Next, a chromium layer was sputtered onto the aluminum on both types of wafer, to protect them from being etched in HF prior to monolayer formation. This was followed by an annealing step at 450 °C in an N_2 atmosphere. The photoresist was removed with acetone. Finally, the samples were diced into pieces 18 mm × 25 mm. Before monolayer modification, the samples were placed in a plasma cleaner to remove all organic contaminants. Possible traces of HMDS and photoresist (if any) were thus removed from the oxide surface.

Preparation of the Organic Monolayer: The silicon samples were first wiped with tissue saturated with chemically pure acetone. After that, the samples were sonicated for at least 15 min in demineralized H_2O and acetone, consecutively. Then the samples were dried in a stream of nitrogen and placed in a plasma cleaner/sterilizer (Harrick PDC-32G) for 1 min. Subsequently the samples were etched in 2.5% HF for 2 min. After removal from the HF solution, the sample was dry, indicating that the surface was oxide-free.

A 1-alkene solution in mesitylene (12.5 mL, 0.2 M) was placed in a small, three-necked flask fitted with a nitrogen inlet, a condenser with a $CaCl_2$ tube, and a stopper. The solution was deoxygenated for at least 45 min, by refluxing it, while slowly bubbling dry nitrogen through the solution. Subsequently a freshly etched silicon sample was added to the refluxing solution by removing and replacing the stopper quickly. After 2 h, the solution was allowed to cool and the sample was removed and rinsed extensively with distilled PE 40/60, ethanol, and CH_2Cl_2, consecutively.

Preparation of the Hydrogen-Terminated Samples: The samples were sonicated for at least 10 min in demineralized H_2O and acetone, consecutively. Then the samples were placed in a plasma cleaner/sterilizer (Tepla 300E) for 1 min. Subsequently, the samples were etched in 1% HF for 1 min, rinsed with demineralized water and dried using a nitrogen gun.

Preparation of the Samples for Verification of the Mercury Dot Area: In order to check the area of the mercury dot, both hydrophobic and hydrophilic SiO_2 surfaces of batch 1 were used. This was done to exclude any wetting effects of the mercury, and hence a possible change in effective contact area. Some of the samples of batch 1 of the oxidized wafers were therefore put in a Lab-Line vacuum oven to let the silicon oxide surface react with

Table 6. Static water contact angle and thickness measurements on different insulators.

Sample	Abbreviation	Water contact angle [°]	Thickness [Å]	Thickness determined via:
pSi-SiO_2 (2 nm)	$pSiO_2$	Not measured	19.9 ± 0.6	Ellipsometry
nSi-SiO_2 (2 nm)	$nSiO_2$	Not measured	20.3 ± 1.1	Ellipsometry
pSi-$C_{10}H_{21}$/nSi-$C_{10}H_{21}$	pC_{10}/nC_{10}	107/107	12.1	Calculated[30a]
pSi-$C_{12}H_{25}$/nSi-$C_{12}H_{25}$	pC_{12}/nC_{12}	109/108	13.2 ± 0.1	X-ray reflectivity[30b]
pSi-$C_{16}H_{33}$/nSi-$C_{16}H_{33}$	pC_{16}/nC_{16}	109/108	17.8 ± 0.2	X-ray reflectivity[30b]
pSi-$C_{22}H_{45}$/nSi-$C_{22}H_{45}$	pC_{22}/nC_{22}	102/100	26.0 ± 1.0	X-ray reflectivity[30c]
pSi-SiO_2 (100 nm)	(used for Hg- dot area verification)	< 20	1003 ± 1	Ellipsometry
pSi-SiO_2 (100 nm)–HMDS	(used for Hg- dot area verification)	84	1008 ± 2 (1006 ± 1)[a]	Ellipsometry

[a] Thickness measured before HMDS treatment.

HMDS to make it more hydrophobic. HMDS is normally used as a primer to make the hydrophilic SiO_2 surface hydrophobic for a better adhesion of photoresist. At a pressure of 25 cm Hg and at a temperature of 140 °C, the samples were put in the oven for 100 min under a constant HMDS flow. Afterwards, both the contact angle and the thickness of the HMDS-treated, as well as the non-HMDS treated, SiO_2 surfaces were determined. The thickness of the HMDS-treated SiO_2 surface increased 0.2 nm after HMDS treatment, indicating that only a small layer of HMDS was on the surface. It is not expected that HMDS-treatment of the 100 nm thick SiO_2 layer negatively influences its isolating properties, and hence normal *C–V* measurements are equally possible as for the non-HMDS treated SiO_2 samples to determine the mercury dot area.

Contact Angle and Thickness Measurements: Directly after cleaning, static water contact angles of the monolayers on the silicon samples were obtained using an Erma Contact Angle Meter G-1 (volume of the drop of demineralized $H_2O = 3.5$ μL). Two or three drops of water were placed near one of the short edges of the sample. This wetted area was not studied in the electrical measurements. The error of the contact angles is $\pm 1°$. After removing the water drops, the samples were cleaned with ethanol and CH_2Cl_2. The samples were stored under a nitrogen atmosphere or vacuum until the electrical measurements took place.

The thickness of the oxide layers was measured with an ellipsometer (Plasmos SD 2002) using a fixed refractive index of 1.465 for the SiO_2 layers. The thickness of the organic monolayers was determined earlier, via X-ray reflectivity. The thickness of the C_{10} layer was too thin to be determined via X-ray reflectivity measurements, and was therefore calculated using the model mentioned in ref. [5b]. Table 6 gives an overview of the results.

Electrical Characterization: *I–V* and *C–V* measurements were performed using a mercury probe (Material Development Corporation (MDC) MDC811-150) connected to an HP4140B pA meter and an HP4275A *C–V* meter. A schematic picture of the mercury probe and the sample structure is given in Figure 12. Note that Figure 12 is not to scale and serves only to indicate all the layers and positions of the sample in the setup. The sample was placed with the insulator faced down in the probe. Via a manually operated lever, the chuck-contact is pressed down on the back contact of the sample and fixed via a spring. As the lever is pressed down, a vacuum valve is opened and mercury in the reservoirs is sucked via the tubes against the insulator. Before the start of the measurements, the mercury was renewed. The setup was computer controlled by the MDC software package CSM/Win. For the *I–V* measurements, the bias voltage was swept from +1.0 V to −1.0 V for p-type silicon, or vice versa for n-type silicon. The mercury was positively biased with respect to the bulk silicon. The voltage was swept with a step size of 0.01 V, at long integration time, and a delay time of 0.2 s, to measure the leakage current exclusively. All measurements were repeated at least once, and in this voltage range none of the samples with organic monolayers showed breakthrough or increase in current during subsequent measurements. For the *C–V* measurements, the DC-voltage was swept in the same way as in the *I–V* measurements with a step size of 0.01 V. The ac-amplitude was 50 mV, and the measurement frequency was chosen at 400 kHz. This frequency should not be too low to prevent quasistatic behavior, and to prevent possible interface states from following the ac-signal. For half of the spots, *C–V* measurements were repeated at 10 kHz, 40 kHz, and 100 kHz for comparison purposes. The impedance model used for the *C–V* measurements was a parallel circuit of a resistor and capacitor, whereby any influence of series resistance was compensated for.

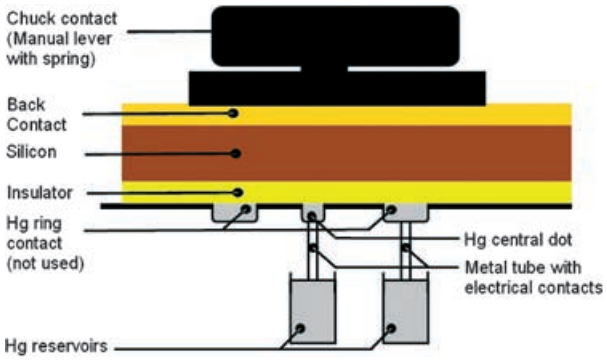

Figure 12. Schematic view of the measurement setup. Only the central mercury dot was used for measurements. The outer mercury ring was not electrically connected.

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