

# Electrical Characterization of Thin-Film Structures With Redeposited Sidewalls

Deepu Roy, Micha A. A. in 't Zandt, and Rob A. M. Wolters

**Abstract**—Accurate electrical characterization of test structures and devices requires identification and correction for parasitic current paths in the measurement network. The sidewalls formed during reactive ion etching of thin-film phase-change material layers in argon plasma can result in parasitic current paths in the structures. In this paper, thin-film structures with redeposited sidewalls are realized, and they are experimentally characterized by electrical resistance measurements on van der Pauw test structures. The impact of conducting sidewalls on contact resistance measurements and data extraction from cross-bridge Kelvin resistor structures is discussed. The error introduced in the electrical resistance measurements from these test structures is analytically modeled. The impact on the electrical performance of devices due to the formation of sidewalls is also discussed.

**Index Terms**—Contact resistance, cross-bridge Kelvin resistor (CBKR), redeposition, sidewalls, van der Pauw (VDP).

## I. INTRODUCTION

SCALING and performance requirements in memory technologies demand the integration of nonstandard materials into the device stack. An example is the introduction of phase-change materials (PCMs) in the metallization level of integrated circuits for future nonvolatile memory applications [1]. For phase-change random access memory (PCRAM) cells, these layers are patterned to form either a line cell [2] or an ovonic-unified-memory-type cell [3]. The state of a PCRAM cell is determined by resistance measurement across the cell. In the case of a line cell, the resistance in the current path of the memory cell consists of the PCM resistance and two metal-to-PCM contact resistances. The resistivity of the PCM layer can be calculated from sheet resistance measurements on van der Pauw (VDP) structures [4], [5]. The metal-to-PCM contact resistance values are extracted from the measurements on cross-bridge Kelvin resistor (CBKR) test structures [6], [11]. VDP and CBKR structures are electrically characterized by four-point current–voltage ( $I$ – $V$ ) measurements.

Manuscript received September 2, 2010; revised December 3, 2010; accepted December 21, 2010. Date of publication January 20, 2011; date of current version March 23, 2011. This work was supported by Project MC3.07298 in the framework of the Research Program of the Materials Innovation Institute ([www.m2i.nl](http://www.m2i.nl)). The review of this paper was arranged by Editor S. Deleonibus.

D. Roy and M. A. A. in 't Zandt are with the NXP-TSMC Research Center, NXP Semiconductors, 5656 AE Eindhoven, The Netherlands (e-mail: [deepu.roy@nxp.com](mailto:deepu.roy@nxp.com)).

R. A. M. Wolters is with the NXP-TSMC Research Center, NXP Semiconductors, 5656 AE Eindhoven, The Netherlands, and also with MESA+ Institute for Nanotechnology, University of Twente, 7500 AE Enschede, The Netherlands.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2010.2103318

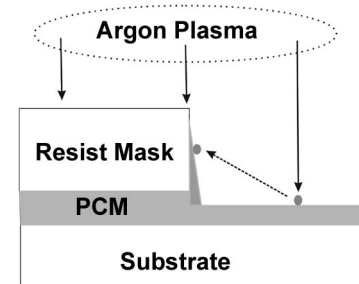


Fig. 1. Schematic showing the redeposition of the PCM layer on to the resist sidewall during etching.

Thin-film structures are patterned by reactive ion etching (RIE) with a protective mask. RIE, which is a combination of physical sputtering and chemical etching in a plasma, is the preferred etching process for achieving anisotropic etch profiles. Due to the high etch rate of PCM (doped  $\text{Sb}_2\text{Te}$  and  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ) toward commonly used etch chemistries, isotropic underetching is hazardous [7]. However, PCM devices with uniform profiles can be fabricated by optimization of the etch gas mixing ratio, tuning the process parameters [8]–[10], or by the use of a hard mask [7]. It is reported that with the inclusion of argon in the etch chemistry, physical ion bombardment becomes a dominant factor for PCM etching [8]. Ion bombardment and subsequent sputter etching in argon plasma limits the underetching of the PCM layers. However, in the case when sputtering dominates the etch rate, the fences or the sidewalls of the resputtered material can be formed either by direct redeposition onto the masking layer or by condensation from the gas phase [12]. The sidewalls formed by direct redeposition on the protective resist mask during etching of the PCM layers in argon plasma is schematically shown in Fig. 1. These sidewalls may split and stand up or fall over locally with or without breaking (electrical) connections. The standing and fallen sidewalls formed after mask removal are shown in Fig. 2(a). The sidewall formed around a PCRAM line cell is shown in Fig. 2(b). The formation of sidewalls by direct redeposition due to sputtering has been previously modeled for other layers [13]–[15]. To our knowledge, the electrical characterization of thin-film structures to study the presence of resputtered sidewalls has not been reported until now.

This paper investigates the impact of the presence of sidewalls in a thin-film device and the effects on the electrical characterization and data extraction from VDP and CBKR structures. VDP measurements on square structures with different size and thickness were performed to detect the presence of sidewalls and to characterize the inaccuracies introduced in the

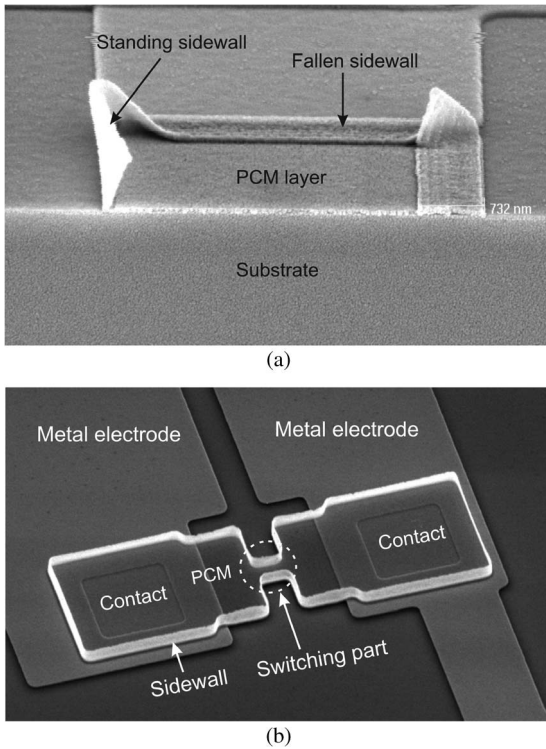


Fig. 2. SEM image of (a) standing and fallen sidewall formed around an etched PCM layer after mask removal. (b) Standing sidewall formed around the PCM layer after etching in a PCRAM line cell.

calculation of resistivity from these structures with sidewalls. The error introduced in the data extraction from metal to PCM CBKR contact resistance measurement structures with PCM sidewalls is also reported. The nature of the sidewalls formed (standing or fallen) is correlated by scanning electron microscope (SEM) inspection to the errors introduced in the measurements and data extraction. Based on these measurements, the realization and electrical performance of thin-film devices associated with the formation of sidewalls are discussed.

## II. MEASUREMENT STRUCTURES

### A. Processing

VDP structures in thin-film TiW and PCM and TiW-to-metal CBKR structures are fabricated on Si-SiO<sub>2</sub> wafers. First, a 50-nm TiW metal layer is deposited by sputtering and is patterned to form the metal VDP structure and the bottom electrode layer of the CBKR structure. Then, 50-nm plasma-enhanced chemical vapor deposition (PECVD) SiO<sub>2</sub> is deposited at 400 °C through which electrical contacts are defined between TiW and the subsequent deposited PCM layer. The PCM layer is deposited by sputtering and is patterned to form the VDP structures and the top layer of the CBKR structure. Both TiW and PCM layers are patterned by RIE using a 800-nm-thick photoresist mask. TiW layers are patterned in a chlorine-based chemistry. The chemical nature of this etching resulted in volatile components and, hence, no sidewall formation. Due to the high chemical reactivity of PCM, it had to be etched in argon plasma, which in this case led to the formation

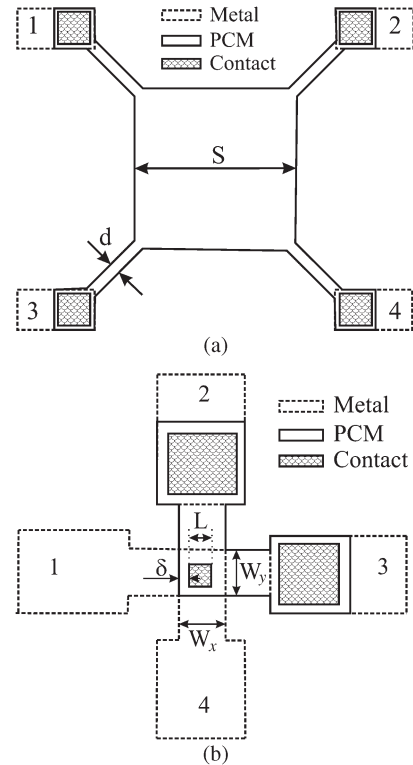


Fig. 3. (a) Layout of a VDP square of side  $S$ . (b) Layout of a CBKR structure showing the contact area ( $A = L \times L$ ) and the overlap length  $\delta$ .

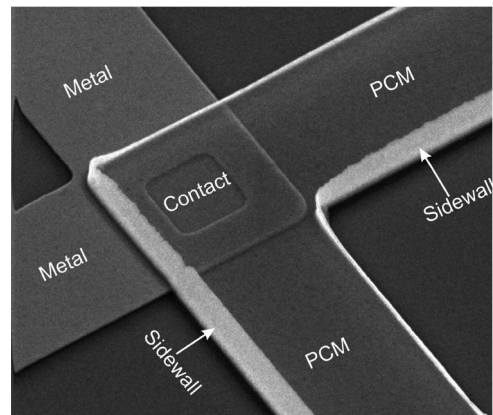


Fig. 4. SEM image (taken with sample tilted at 45°) of the standing sidewalls formed around the PCM layer after etching in a CBKR structure.

of sidewalls due to direct redeposition. After patterning the layers, the resist mask is removed in oxygen plasma. Finally, the structures are covered with a 500-nm PECVD oxide dielectric layer through which contacts are opened to the bond pads for electrical measurements.

### B. VDP Structure

The layout of a typical square VDP structure of edge length  $S$  is shown in Fig. 3(a). Structures with  $S = 2, 5, 10, 20,$  and  $50 \mu\text{m}$  were available for both the PCM layer and TiW layer on each wafer (see Fig. 4). Different wafers were fabricated with a PCM layer thickness of 20, 50, and 100 nm. To characterize these structures, a current is forced from pad 1

to 2, and a voltage is measured at pad 3 and 4, from which the resistance is calculated. In the case of a square VDP structure having a uniform layer thickness, the length of the electrical contact  $d$  should be negligibly small, compared with the edge length of the structure  $S$ . In this case, the measured resistance  $R$  of the structure is independent of the dimension of the square. From  $R$ , the sheet resistance  $R_{sh}$  of the layer is obtained by using the geometrical factor  $\pi/\ln(2)$  [4], [5], i.e.,

$$R_{sh} = \frac{\pi}{\ln(2)} \times \frac{V}{I} \approx 4.53 \times \frac{V}{I}. \quad (1)$$

$R_{sh}$  is in turn related to the resistivity of the layer  $\rho$  of thickness  $t$  as given by

$$\rho = R_{sh} \times t. \quad (2)$$

### C. CBKR Structures

The CBKR test structures are used to perform contact resistance measurements and specific contact resistance  $\rho_c$  extraction [6], [11]. The layout of a CBKR structure with a well-defined contact area ( $A = L \times L$ ) and an overlap length  $\delta$  is shown in Fig. 3(b). The structures with PCM-to-TiW contact area varying from 1 to 16  $\mu\text{m}^2$  and with  $\delta$  varying from 0.2 to 5  $\mu\text{m}$  are fabricated. To measure the metal-to-PCM contact resistance, a current is forced from the metal to the PCM (1 to 3), and the voltage is measured orthogonal to the direction of current flow (2 and 4). This allows the measurement of the average voltage at the interface [6] from which the measured resistance  $R_k$  is calculated. The measured resistance  $R_k$  of the CBKR structure includes two parts: 1) the resistance of the contact  $R_c$  and 2) the resistance due to current spreading in the overlap area  $R_d$ . To accurately extract  $\rho_c$ , the contribution of  $R_d$  needs to be subtracted from  $R_k$ . This is achieved using a 2-D analytical model [11], taking into account the  $R_{sh}$  values from the associated VDP structures as given by

$$R_k = \frac{\rho_c}{A} + \frac{4R_{sh}\delta^2}{3W_xW_y} \left[ 1 + \frac{\delta}{2(W_x - \delta)} \right] = R_c + R_d. \quad (3)$$

## III. ELECTRICAL CHARACTERIZATION

### A. VDP Resistivity Measurements

Sheet resistance and resistivity values were calculated for PCM and TiW layers from the resistance measurements on the VDP structures using (1) and (2). These measurements were performed on structures with different dimensions. Fig. 5(a) shows the PCM resistivity measured on square VDP structures of different edge length  $S$ . These measurements include structures with standing and fallen sidewalls formed after etching. For the TiW structures, no sidewalls are observed, and the calculated resistivity is practically independent on the dimension of the VDP structures. Only for the smallest structure ( $S = 2 \mu\text{m}$ ) that a lower value is observed. This is due to nonideal peripheral contacts with contact length ( $d = 1 \mu\text{m}$ ), which is more than 10% of the edge length  $S$ . Then, for the calculation of  $R_{sh}$  from the square VDP structures, a correction is required for the geometrical factor  $\pi/\ln(2)$  [5]. This additional

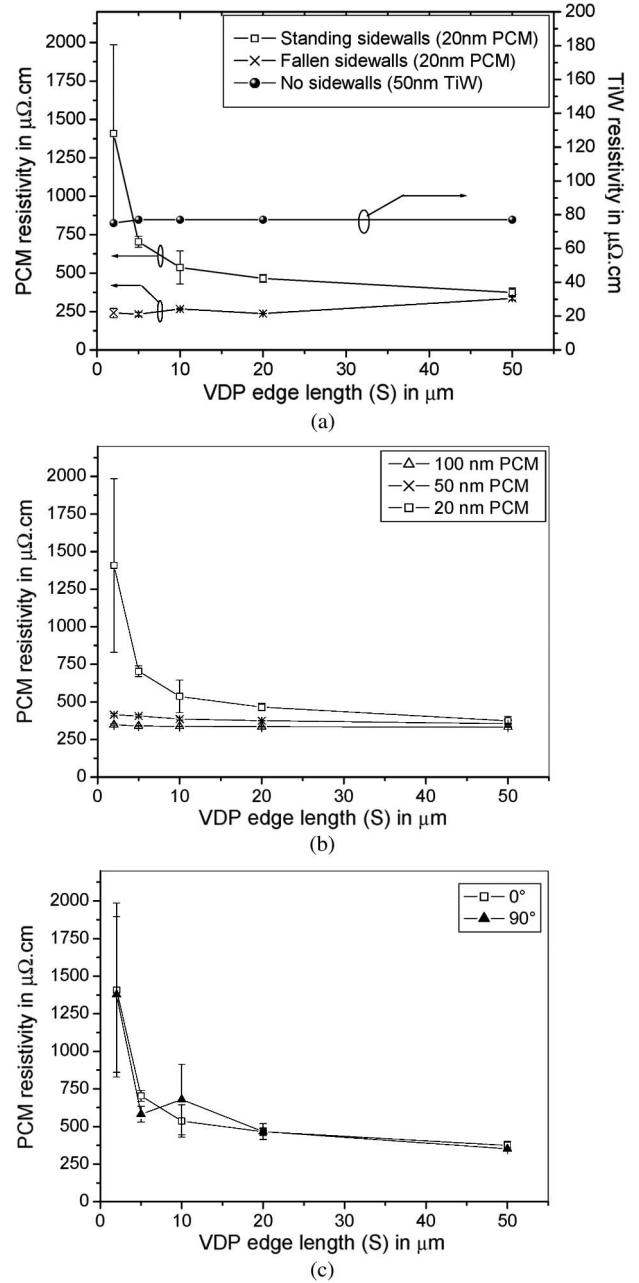


Fig. 5. Sheet resistance with the dimension of the side of the VDP square. (a) Effect of standing and fallen sidewalls for the PCM layer, compared with TiW without the sidewalls. (b) Presence of sidewalls for the PCM layers with 20, 50, and 100 nm thickness. (c) PCM van der Pauw of 20 nm, with standing sidewalls measured for two different current directions. (Error bar) The spread in measurements at each point.

correction factor is not applied for in the 2- $\mu\text{m}$  TiW structures. For the PCM structures with standing sidewalls (SEM), the measured resistance drastically increases with decreasing VDP edge length. In the case of fallen sidewalls, the resistivity of the layer decreases for smaller VDP structures. As expected, the influence of the sidewall is lowest for larger structures.

The PCM resistivity with VDP edge length for three different layer thicknesses is shown in Fig. 5(b). The resistivity deviates more in the case of thinner PCM layers, as compared with thicker layers. Additionally, a larger deviation is observed for the smaller VDP structures.

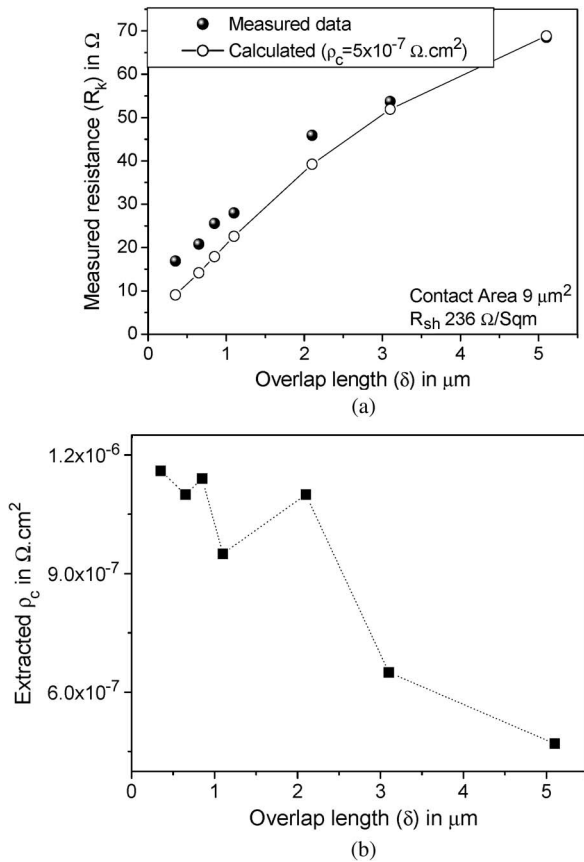


Fig. 6. (a)  $R_k$  with  $\delta$  for the CBKR structures with standing sidewalls. (● symbol) The measurement points and (○ symbol) the values calculated with  $\rho_c$  extracted for  $\delta = 5 \mu\text{m}$ . (b) Extracted  $\rho_c$  with  $\delta$  for measurement points in Fig. 6(a).

To examine the symmetry of the VDP structures with sidewalls, measurements were performed by rotating the current force and the voltage measurement terminals by  $90^\circ$  four times. Fig. 5(c) shows the PCM resistivity measured in two different directions. The measurements in opposite directions rotating the terminals by  $180^\circ$  result in the same electrical resistance.

### B. CBKR Contact Resistance Measurements

The effect of the sidewalls on the extracted  $\rho_c$  is demonstrated using the contact resistance measurements on the CBKR structures. First, consider the situation in which the standing sidewalls are formed by resputtering around the PCM layer in the CBKR structure, as shown in Fig. 3(b). The measured resistance  $R_k$  with  $\delta$  for these structures is shown in Fig. 6(a). For all these structures, the TiW-to-PCM contact length  $L$  is  $3 \mu\text{m}$ . The  $\rho_c$  extracted from these measurement points with  $\delta$  using (3) is shown in Fig. 5(b). The effect of the sidewalls on the  $R_k$  values is expected to be lower for larger  $\delta$ . The largest  $\delta$  available is  $5 \mu\text{m}$ , and the extracted  $\rho_c$  from this structure is  $5 \times 10^{-7} \Omega \cdot \text{cm}^2$ . The calculated values of  $R_k$  using (3) with  $\delta$  for this CBKR structures having a  $\rho_c = 5 \times 10^{-7} \Omega \cdot \text{cm}^2$  and PCM  $R_{\text{sh}}$  of  $236 \Omega/\text{sq}$  (from the VDP structures) is shown in Fig. 6(a). As observed in the figure, the deviation in the calculated and measured  $R_k$  values are larger for smaller  $\delta$ .

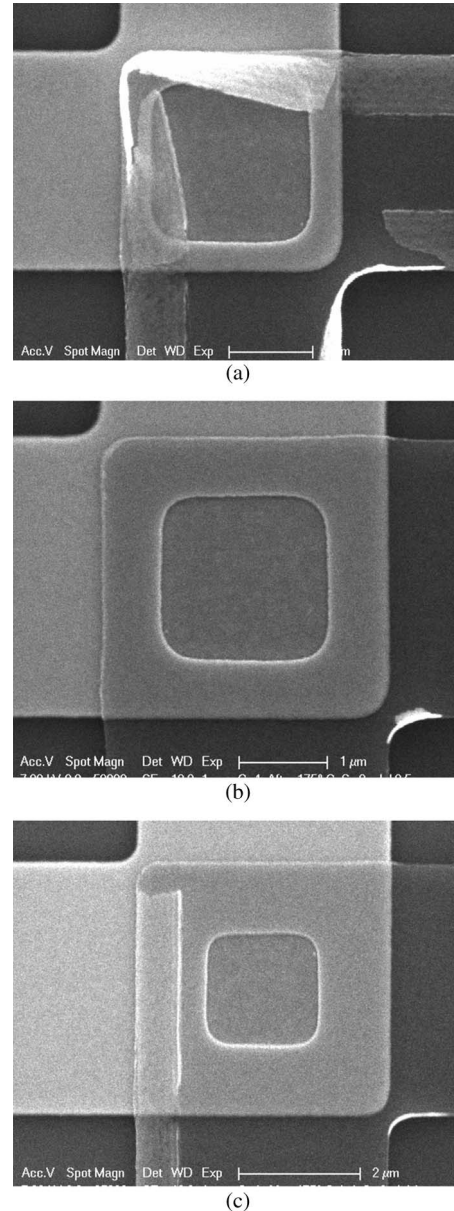


Fig. 7. SEM images of the CBKR structures showing different patterns of sidewall formation. All the structures have the same contact area of  $4 \mu\text{m}^2$  but different  $\delta$ . (a)  $\delta = 0.35 \mu\text{m}$  structure with irregularly formed PCM sidewalls on all sides. (b)  $\delta = 0.65 \mu\text{m}$  structure with no PCM sidewalls. (c)  $\delta = 1.1 \mu\text{m}$  structure with PCM sidewalls formed only on one side.

Sidewalls can be also irregularly formed on the CBKR structures. Fig. 7 shows the SEM images of three structures with the same contact length  $L$  of  $2 \mu\text{m}$  but with different  $\delta$ . Fig. 6(a) shows a CBKR structure with a  $\delta$  of  $0.35 \mu\text{m}$ , with irregular sidewalls formed around the PCM layer. Fig. 7(b) shows a CBKR structure with a  $\delta$  of  $0.65 \mu\text{m}$ , without sidewalls, and Fig. 7(c) with a  $\delta$  of  $1.1 \mu\text{m}$ , with PCM sidewalls formed on one side of the structure. The measured resistance  $R_k$  with  $\delta$  for these particular structures is shown in Fig. 8(a). The  $\rho_c$  extracted from these measurements for different  $\delta$  is shown in Fig. 8(b). The extracted  $\rho_c$  is higher for measurement points a and c, which are associated to the CBKR structures for which the sidewalls are observed from the SEM image. The actual  $\rho_c$  for the contacts is represented by the line in the graph. The

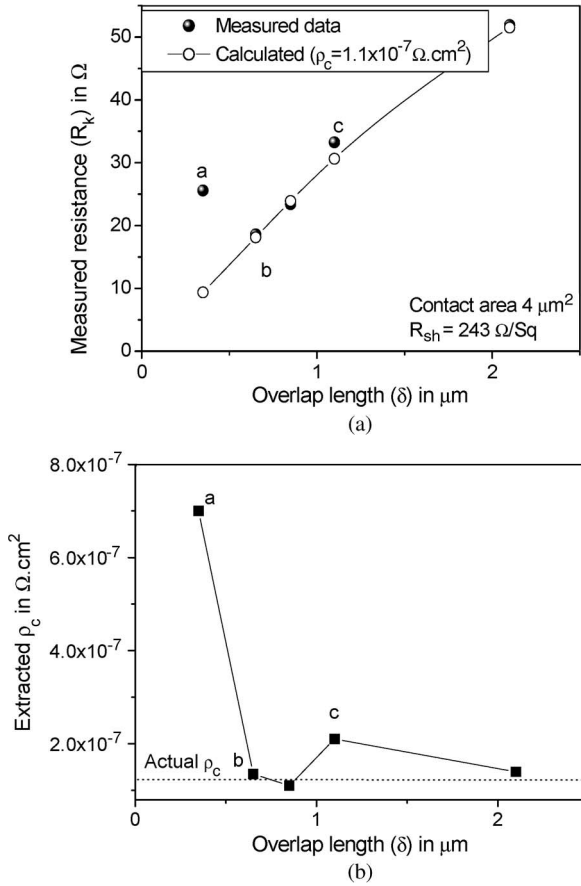


Fig. 8. (a)  $R_k$  with  $\delta$  for CBKR structures with irregularly formed sidewalls. Inset characters a, b, and c correspond to the SEM image in Fig. 6. (●) The measurement points and (○) the calculated value minimizing the effect of the sidewalls. (b) Extracted  $\rho_c$  with  $\delta$  for the CBKR structures. (Dotted line) The actual  $\rho_c$  for this contact.

deviation in  $\rho_c$  with sidewalls is larger for the structure with smaller  $\delta$ . The  $\rho_c$  extracted for these structures without sidewalls is  $1.1 \times 10^{-7} \Omega \cdot \text{cm}^2$ . Fig. 8(a) shows the calculated value of  $R_k$  using (4) for this value of  $\rho_c$  and the PCM sheet resistance of  $243 \Omega/\text{sq}$  (from VDP structure). The calculated  $R_k$  coincides with the measurement points for structures without sidewalls.

According to (3),  $R_k$  depends on PCM  $R_{\text{sh}}$ . To investigate the effect of the sidewalls with PCM  $R_{\text{sh}}$ , additional measurements were performed on TiW-to-PCM CBKR structures fabricated with a thermal budget of  $120^\circ\text{C}$ . The measured  $R_k$  with  $\delta$  of these structures is shown in Fig. 9(a). These measurements were performed on structures with the contact areas of 1, 4, 9, and  $16 \mu\text{m}^2$ . From these measurements, the average  $\rho_c$  of  $3.9 \times 10^{-6} \Omega \cdot \text{cm}^2$  is extracted. The accompanying VDP structures measure a PCM resistivity of  $12.2 \text{ m}\Omega \cdot \text{cm}$ . The PCM used in these structures is  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ , which will be in metastable state after  $120^\circ\text{C}$  of thermal treatment. The resistivity of this PCM layer can be lowered by annealing at a higher temperature [2], [3]. When subjected to a temperature anneal of  $250^\circ\text{C}$  for 5 min in  $\text{N}_2$  ambient, the resistivity of the PCM in these structures lowers to  $416 \mu\Omega \cdot \text{cm}$ . The  $R_k$  with  $\delta$  measurements for the same structures after  $250^\circ\text{C}$  anneal is shown in Fig. 9(b). The  $\rho_c$  extracted from these measurements is approximately  $1.7 \times 10^{-6} \Omega \cdot \text{cm}^2$ .

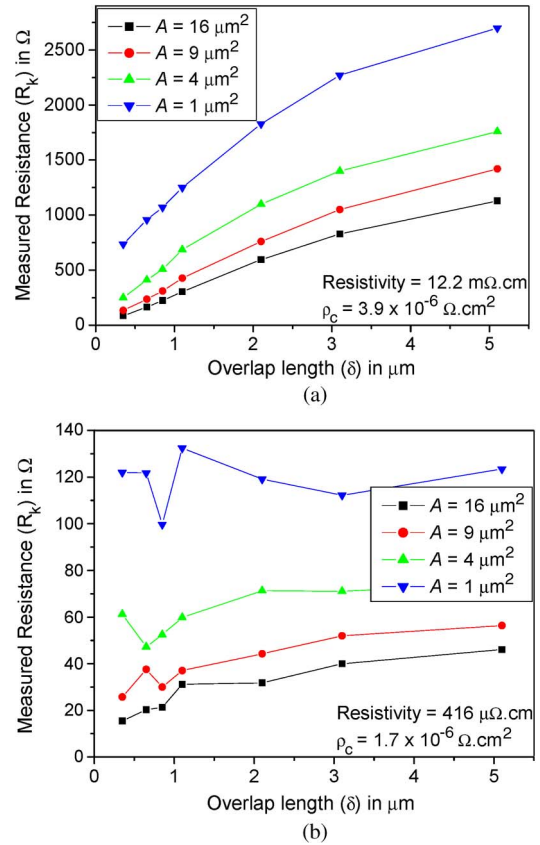


Fig. 9.  $R_k$  with  $\delta$  for the CBKR structures with contact area  $A$  of 1, 4, 9, and  $16 \mu\text{m}^2$ . (a) Before anneal. (b) After  $250^\circ\text{C}$  anneal. (Inset values) The PCM resistivity and extracted  $\rho_c$ .

## IV. DISCUSSIONS

### A. VDP Resistivity

Direct redeposition of PCM during RIE on to the vertical edge faces of the masking layer leads to the formation of PCM sidewalls around the etched structure. The height of the sidewalls formed is approximately  $1 \mu\text{m}$ , and it is mainly determined by the thickness of the resist mask. The sidewall material could have a lower density and, therefore, a higher resistivity  $\rho_s$  than the layer itself. By first-order approximation, the formation of the standing sidewalls expands the VDP square equally on all the sides. The resulting final structure will also be a square, but the expanded sidewall region of the square will have a larger resistivity. In addition, expansion of the VDP square due to the formation of standing sidewalls moves the position of the electrical contacts from the corners to the inside. As opposed to the case of having point contacts at the corners of the square, if they are moved inside, the geometrical factor used in the calculation of the  $R_{\text{sh}}$  changes. The relative error introduced in the sheet resistance due to the placement of contacts inside by a distance  $d$  for a circular structure of diameter  $D$  is given by [4]

$$\frac{\Delta R_{\text{sh}}}{R_{\text{sh}}} = \frac{d^2}{2D^2 \ln 2}. \quad (4)$$

For smaller VDP structures, the relative contribution of the sheet resistance of the sidewalls and the effect of the placement

of the contacts inside the square are larger. This explains the increase in resistivity and larger spread in the measurements for smaller VDP structures with standing sidewalls, as shown in Fig. 5(a). In the case of the PCM structures with sidewalls fallen on to the layer itself, the thickness of the PCM layer is locally increased around the edges. An increase in the thickness of the layer results in lower  $R_{sh}$  [using (2)], as shown in Fig. 5(a). The effect of the sidewalls is larger for smaller structures since the relative area over which the sidewalls will be fallen is larger for these structures.

The dependence of  $\rho$  and  $R_{sh}$  on layer thickness is given in (2). The error introduced in  $R_{sh}$ , by moving the contacts inside, is proportional to the  $R_{sh}$  of the layer (4). As a result,  $\Delta R_{sh}$  is inversely proportional to the thickness of the layer. This results in a more pronounced influence on resistivity measurements for thinner PCM layers with standing sidewalls, as shown in Fig. 5(b). In practice, the sidewalls do not exhibit a regular shape or uniform resistivity by nature of its formation. They may split, stand up, or fall over locally with or without breaking (electrical) connections. This means that, due to these inhomogeneities, the structure can become electrically asymmetric, as shown in Fig. 5(c). This will be more pronounced for the smaller structures or thinner layers, and it also results in a larger spread in measurements. In this sense, this can be used as an indicator for the presence of the sidewalls. It will be most sensitive to smaller structures.

### B. Metal PCM Contact Resistance

As shown in (3), the measured  $R_k$  includes contact resistance  $R_c$  and the contribution of overlap  $R_d$ , which depends on PCM  $R_{sh}$  and  $\delta$ . Ideally, the extracted  $\rho_c$  is a property of the interface and should be independent on the  $\delta$  around the contact. As observed in Fig. 6(b), in the case of standing PCM sidewalls for the contacts with the same area extracted,  $\rho_c$  decreases with  $\delta$ . The extracted  $\rho_c$  for  $\delta$  of  $0.35 \mu\text{m}$  is  $1.1 \times 10^{-6} \Omega \cdot \text{cm}^2$  and for  $\delta$  of  $5 \mu\text{m}$  is  $5 \times 10^{-7} \Omega \cdot \text{cm}^2$ . The formation of the standing sidewalls expands the  $\delta$  by its height, which directly influences  $R_d$  and  $R_k$ , resulting in the inaccurate extraction of  $\rho_c$  from the CBKR structures. It is reported that, due to current spreading effects around the contact the extracted,  $\rho_c$  increases with delta [16], [17]. The PCM sidewalls shown in Fig. 4 could be considered as an asymmetric  $\delta$  or a misalignment around the contact. The effect of these sidewalls is only on one side of the measurement current path. Misalignments in  $\delta$  in one direction have been reported to have a similar decrease in the extracted  $\rho_c$  [18]. As observed in Fig. 6(a), with standing sidewalls, the deviation in the calculated and measured  $R_k$  values are larger for smaller  $\delta$ . The effect of the sidewalls will be smallest for the structure with a  $\delta$  of  $5 \mu\text{m}$ , and the obtained value of  $\rho_c$  approximates almost the actual value. In this case, the  $R_k$  values for the smallest delta structures ( $\delta$  of  $0.35 \mu\text{m}$ ) are overestimated by approximately 50% and the extracted  $\rho_c$  by more than 60% of the actual values.

## V. CONCLUSION

In this paper, we have identified the presence and modeled the influence of redeposited PCM sidewalls in a thin-film device

by electrical measurements and data extraction from VDP and CBKR test structures. The presence of sidewalls is indicated by electrical resistance measurements on the VDP structures with a wide range of dimensions. When the height of the sidewalls in these structures is in the same order as the dimensions of the structure, the measured resistance values deviates more from its ideal value. The effect of the sidewalls on the calculated resistivity values will be more pronounced for smaller structures and for thinner layers. CBKR structures with standing sidewalls lead to underestimation of extracted  $\rho_c$  due to inaccurate estimation of  $R_{sh}$  and  $\delta$ . The error introduced in extracted  $\rho_c$  from CBKR structures with sidewalls is larger for CBKR structures with smaller contact area or for smaller  $\delta$  or for lower  $\rho_c$  or for lower PCM resistivity. For both these structures, the error introduced in the electrical measurements is correlated to the pattern of the sidewall formation by SEM inspection.

The redeposited sidewalls formed during etching result in the creation of parasitic current paths in the structure or device. As a result, the estimation of layer resistivity from the VDP structures and contact resistance extraction from the CBKR structures will be inaccurate. The redeposited sidewalls in these thin-film structures also result in an increase in the spread in the measured resistance values indicating its presence.

## ACKNOWLEDGMENT

The authors would like to thank D. Gravesteijn, K. Reimann, and H. Tuinhout from NXP Semiconductors and J. Klootwijk from Philips Research for fruitful discussions.

## REFERENCES

- [1] S. R. Ovshinsky, "Reversible electrical switching phenomenon in disordered structures," *Phys. Rev. Lett.*, vol. 21, no. 20, pp. 1450–1453, Nov. 1968.
- [2] M. H. R. Lankhorst, B. W. S. M. M. Ketelaars, and R. A. M. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nat. Mater.*, vol. 4, no. 4, pp. 347–352, Apr. 2005.
- [3] S. Raoux and M. Wuttig, *Phase Change Materials: Science and Application*. New York: Springer-Verlag, 2009.
- [4] L. J. van der Pauw, "A method of measuring specific resistivity and Hall Effect of discs of arbitrary shape," *Philips Res. Rep.*, vol. 13, no. 1, pp. 1–9, Feb. 1958.
- [5] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ: Wiley-Interscience, 2006, ch. 1.
- [6] S. J. Proctor and L. W. Linholm, "A direct measurement of interfacial contact resistance," *IEEE Electron Device Lett.*, vol. EDL-3, no. 10, pp. 294–296, Oct. 1982.
- [7] S.-M. Yoon, K.-J. Choi, Y.-S. Park, S.-Y. Lee, N.-Y. Lee, and B.-G. Yu, "Dry etching of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films into nanosized patterns using TiN mask," *Jpn. J. Appl. Phys.*, vol. 45, no. 40, pp. L1 080–L1 083, Oct. 2006.
- [8] S.-M. Yoon, N.-Y. Lee, S.-O. Ryu, Y.-S. Park, S.-Y. Lee, K.-J. Choi, and B.-G. Yu, "Etching characteristics of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  using high-density helicon plasma for the nonvolatile phase-change memory applications," *Jpn. J. Appl. Phys.*, vol. 44, no. 27, pp. L869–L872, Jun. 2005.
- [9] G. Feng, B. Liu, Z. Song, S. Feng, and B. Chen, "Reactive ion etching of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  in  $\text{CHF}_3/\text{O}_2$  plasma for nonvolatile phase-change memory device," *Electrochem. Solid-State Lett.*, vol. 10, no. 5, pp. D47–D50, 2007.
- [10] K.-Y. Yang, S.-H. Hong, D.-K. Kim, B.-K. Cheong, and H. Lee, "Patterning of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change material using UV nano-imprint lithography," *Microelectron. Eng.*, vol. 84, no. 1, pp. 21–24, Jan. 2007.
- [11] T. A. Schreyer and K. C. Saraswat, "A two-dimensional analytical model of the cross-bridge Kelvin resistor," *IEEE Electron Device Lett.*, vol. EDL-7, no. 12, pp. 661–663, Dec. 1986.
- [12] L. Stafford, J. Margot, S. Delprat, M. Chaker, and S. J. Pearton, "Influence of redeposition on the plasma etching dynamics," *J. Appl. Phys.*, vol. 101, no. 8, pp. 083 303-1–083 303-6, Apr. 2007.

- [13] C. Y. Chang, J. P. McVittie, K. C. Saraswat, and K. K. Lin, "Backscattered deposition in Ar sputter etch of silicon dioxide," *Appl. Phys. Lett.*, vol. 63, no. 16, pp. 2294–2296, Oct. 1993.
- [14] S. Delprat, M. Chaker, and J. Margot, "Investigation of the gas pressure influence on patterned platinum etching characteristics using a high-density plasma," *J. Appl. Phys.*, vol. 89, no. 1, pp. 29–33, Jan. 2001.
- [15] J. Saussac, J. Margot, L. Stafford, and M. Chaker, "Simulation of redeposition during platinum etching in argon plasma," *J. Appl. Phys.*, vol. 107, no. 6, pp. 063 306-1–063 306-5, Mar. 2010.
- [16] M. Finetti, A. Scorzoni, and G. Soncini, "Lateral current crowding effects on resistance measurements in four terminal resistor test patterns," *IEEE Electron Device Lett.*, vol. EDL-5, no. 12, pp. 524–526, Dec. 1984.
- [17] N. Stavitski, J. H. Klootwijk, H. W. Van Zeijl, A. Y. Kovalgin, and R. A. M. Wolters, "Cross bridge Kelvin resistor structure for reliable measurement of low contact resistances and contact interface characterization," *IEEE Trans. Semicond. Manuf.*, vol. 22, no. 1, pp. 146–152, Feb. 2009.
- [18] R. L. Gillenwater, M. J. Hafich, and G. Y. Robinson, "The effect of lateral current spreading on the specific contact resistivity in D-resistor Kelvin devices," *IEEE Trans. Electron Devices*, vol. ED-34, no. 3, pp. 537–543, Mar. 1987.



**Deepu Roy** was born in India in 1982. He received the B.tech. degree in instrumentation from Cochin University of Science and Technology, Cochin, India, in 2004 and the M.Sc. degree in microelectronics from the Technical University of Delft, Delft, The Netherlands, in 2007. He is currently working toward the Ph.D. degree at NXP Semiconductors, Eindhoven, The Netherlands, with the Chair of the Semiconductor Components, University of Twente, Enschede, The Netherlands.

His current research is focused on electrical characterization and modeling of contacts in a phase-change memories.



**Micha A. A. in 't Zandt** was born in Eindhoven, The Netherlands, on January 12, 1973. In 1997 he received the B.Sc degree in physics from Hogeschool Eindhoven, The Netherlands.

In 1998, he was with Philips Research Laboratories (currently the NXP Semiconductors), Eindhoven, where he was involved in the research of fast-switching SiGe power diodes. Since 2000, he has been working on process integration of trench-gate power metal–oxide–semiconductor field-effect transistors. This work moved from Eindhoven to Leuven, Belgium, in 2001. In January 2004, he moved back to Eindhoven and started to work on the process integration of phase-change memory cells. Since 2009, he has been working on process integration of microelectromechanical system devices for all kinds of applications.



**Rob A. M. Wolters** received the M.Sc. degree in inorganic chemistry from the University of Twente, Enschede, The Netherlands, in 1974 and the Ph.D. degree based on the work on uranium carbonitrides at the Reactor Centrum Nederland, Petten, The Netherlands, in 1978.

He has been with Philips Research (currently the NXP Semiconductors), Eindhoven, The Netherlands, where he covers a large number of subjects related to the processing of Si integrated circuits. He has been involved in the introduction of chlorine-based plasma etching processes for gates and interconnects. He has vast knowledge of the application of silicides, barrier materials, and metals in the Si technology area. Since 2004, he has been a Part-time Professor with MESA+ Institute for Nanotechnology, University of Twente, where he is the Chair of the Semiconductor Components.