

Spatial Interferer Rejection In a 4-Element Beamforming Receiver Frontend with a Switched-Capacitor Vector Modulator

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Abstract—A 1-4GHz 4-element phased array receiver frontend demonstrates spatial interferer rejection using null steering. Element phase and amplitude control are performed by a switched-capacitor vector modulator with integrated downconversion, utilizing a rational sine/cosine approximation. The 65nm CMOS receiver achieves more than 20dB of spatial interferer rejection up to an angular separation of 15°.

Index Terms—beamforming, phased arrays, vector modulator, phase shifter, mixer, switched-capacitor, interference nulling, spatial filtering, receivers

I. INTRODUCTION

Phased arrays receivers use multiple antennas and electronic beamforming to shape the antenna pattern. The principle of a linear phased array beamforming is shown in Fig. 1a. Multiple antennas, typically spaced half a wavelength apart on a line, receive signals arriving with different phases according to angular direction. Phase shifters aim to align the signals in phase for one specific direction, rendering constructive signal summing in the main beam of the antenna pattern. For this direction, the Signal-to-Noise-Ratio (SNR) increases with 3dB per doubling in antennas, in accordance with the larger aperture. Partial summing also occurs, resulting in local maxima defined as sidelobes. For a number of directions, complete destructive summing occurs, i.e. signal nulling. This spatial filtering of interferers outside the main beam, provides an extra selectivity mechanism beside frequency filtering, which is particularly useful when interferers are located close to the desired signal in the frequency spectrum. Fig. 1 shows an example of the antenna gain for different angular directions for a 4-antenna phased array, showing main beam, sidelobes and nulls. This plot only shows the array factor [1], due only to beamforming, *without* considering the radiation pattern of antenna elements¹.

Most applications for phased arrays concentrate on the X-band (8-12GHz) or higher, where due to the small wavelength, a reasonable aperture can be filled by a large number of antenna elements. With respect to a high gain single antenna (like a dish), these arrays benefit from the same SNR improvements, but with electrical instead of mechanical steering. For high performance radar systems, the spatial filtering is also of concern and the rejection of signals outside of the small main beam is improved by suppressing the sidelobes with an amplitude taper [2]. Research has been focused on providing

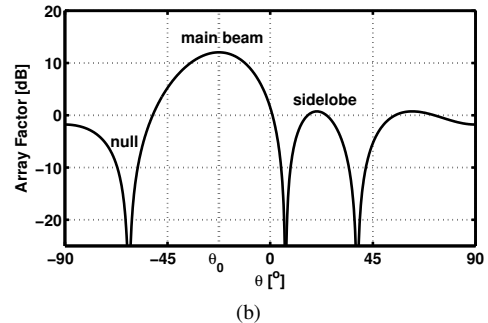
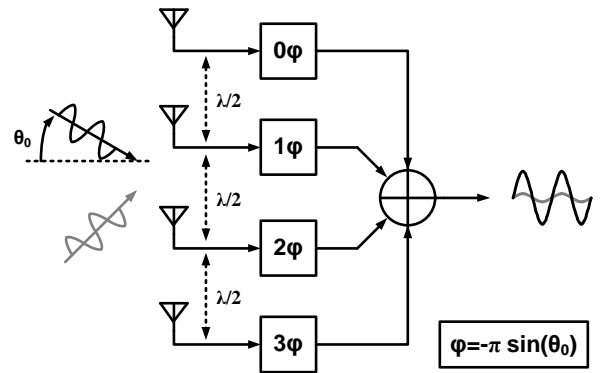


Fig. 1. A phased array (a) with only phase shifters can (b) steer the main beam, but nulls will be steered by the same amount.

phase shifters for these systems, based on injection locking [3], phase selection [4] and vector modulation [5][6][7].

On the other hand, for frequency bands associated with consumer electronics (roughly in the 1-6GHz frequency range), the wavelength is so large that reasonable apertures can only support a few antenna elements. This results in a wide main beam and limited possibilities of suppressing the sidelobes, although the SNR boost and limited spatial rejection are recognized as being beneficial [8]. However, there is still room for implementing adaptive beamforming algorithms [9][10] that modify the array factor with the goal of steering nulls toward interferer positions. To support such algorithms, each element needs both amplitude control and phase control.

Previously, a phased array receiver architecture with a

¹Equivalent to assuming an isotropic antenna element.

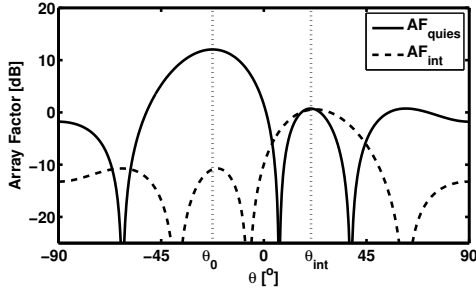


Fig. 2. Modifying the quiescent pattern by subtracting a small cancellation pattern results in a null in direction θ_{INT} .

discrete-time vector modulator, which takes advantage of the high linearity and good matching of switched-capacitor circuits, was proposed [11]. This paper extends the functionality of the proposed vector modulator to include the amplitude control needed for null steering. Furthermore, we will present additional measurements and demonstrate that 20dB of interference rejection is feasible with only 4 antenna elements.

II. INTERFERENCE NULLING BEAMFORMING

The effect of beamforming in a phased array is captured in the array factor: the sensitivity of the array for the different angles from which signals can be received. Like the response of a filter in the *frequency* domain, the array factor is the transfer function of the system in the *spatial* domain. For an N -element linear phased array with $\lambda/2$ antenna spacing, steered with phase shifters, the resulting array factor as a function of direction-of-arrival θ can be expressed as [1]:

$$AF(\theta) = \sum_{n=0}^{N-1} \left[e^{-j\pi \cdot n \sin(\theta_0)} \cdot e^{j\pi \cdot n \sin(\theta)} \right] \quad (1)$$

where θ_0 is the direction of the main beam. The first factor in the sum is due to the phase shifters, the second factor due to the spatial separation of the antennas. An example array factor with the main beam steered to -22° is plotted in Fig. 1b. As the phase shift increases linearly, uniform phase steps are required in the phase shifter.

When an interferer with direction-of-arrival outside of the main beam is present, it will be attenuated compared to the signal in the main beam. Best case rejection is reached when the interferer is present in the direction of a pattern null, while worst case rejection is reached when the interferer is on a pattern sidelobe. For a 4 antenna array, the sidelobe is -10dB below the main beam, resulting in a modest rejection. The rejection can be significantly increased if a null would be adaptively steered on the direction of the interferer, by adding additional amplitude control to the phased array elements in Fig. 3a [9]. It is assumed that the direction of the interferer is known a priori or determined by an additive steering algorithm.

A graphical representation of the beam pattern modification to enable null steering is illustrated in Fig. 2. The goal is to adapt the regular beam pattern AF_{quies} , steered towards the location of the signal-of-interest θ_0 , such that it has a null on the location of the interferer, θ_{int} . In order to do so, we rely on the linear properties of the array factor, i.e. a linear

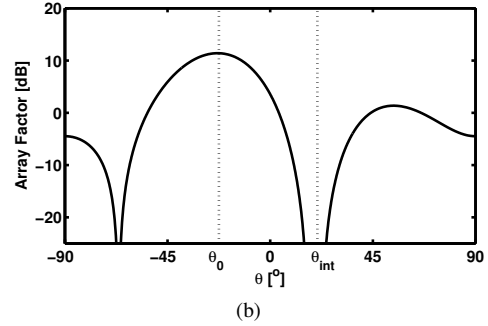
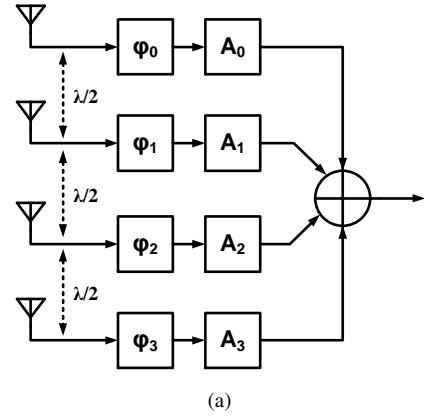


Fig. 3. A phased array with (a) both phase control φ_n and amplitude control A_n can (b) steer the main beam and null independently.

combination of *array factors* is equal to a single array factor with the same linear combination of the *weights*. If two array factors can be created such that their subtraction creates a null on the desired location, then the subtraction of the weights for these array factors will result in new weights for a single array factor with the same nulling.

The cancellation array factor, AF_{int} , is introduced with main beam at the location of the interferer, θ_{int} , and scaled to the height of the quiescent array factor at θ_{int} . Therefore, subtraction of the quiescent and cancellation array factor will result in a new array factor with a null at the interferer location, as shown in Fig. 3b. This new array factor is:

$$AF(\theta) = \sum_{n=0}^{N-1} \left[e^{-j\pi \cdot n \sin(\theta_0)} \cdot e^{j\pi \cdot n \sin(\theta)} \right] - \frac{1}{N} \cdot AF_{quies}(\theta_{int}) \sum_{n=0}^{N-1} \left[e^{-j\pi \cdot n \sin(\theta_{int})} \cdot e^{j\pi \cdot n \sin(\theta)} \right] \quad (2)$$

By taking the two sums together, the antenna factor becomes of a form that can be implemented by the system of Fig. 3a:

$$AF(\theta) = \sum_{n=0}^{N-1} \left[A_n \cdot e^{j2\pi \cdot \varphi_n} \cdot e^{j\pi \cdot n \sin(\theta)} \right] \quad (3)$$

where the element complex weight with amplitude scaling A_n and phase shift φ_n is:

$$A_n \cdot e^{j2\pi \cdot \varphi_n} = e^{-j\pi \cdot n \sin(\theta_0)} - \frac{1}{N} \cdot AF_{quies} \cdot e^{-j\pi \cdot n \sin(\theta_{int})} \quad (4)$$

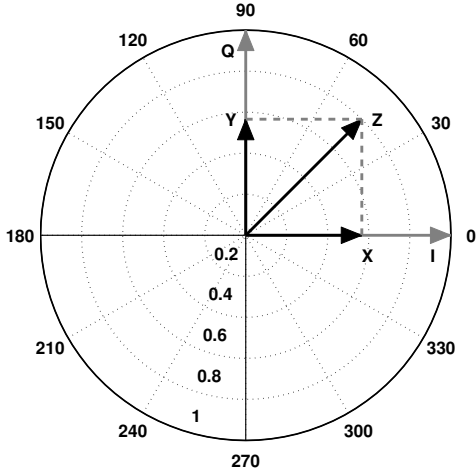


Fig. 4. Phasor diagram illustrating the principle of a vector modulator.

From Fig. 2, it can be deduced that the main beam remains largely unaffected as long as the interferer has a sufficiently different angle-of-arrival, as the main beam is in the sidelobe of the cancellation pattern. In a worst case scenario the interferer is at a quiescent pattern sidelobe, being scaled 10dB below the main beam to ensure nulling. At the main beam, the cancellation sidelobe is another 10dB lower, resulting after subtraction in a modest -1dB gain loss.

Similarly, from (4) it can be deduced that the resulting complex weights for null steering are a small perturbation of the original weights for beam steering. The scaling of the cancellation pattern results in the second part of the subtraction having an amplitude between zero and -10dB, whereas the first part of the subtraction has unity amplitude. Therefore, the amplitudes A_n are close to unity themselves. As opposed to the phase shift quantization, this calls for *non-uniform* amplitude steps.

III. SWITCHED-CAPACITOR VECTOR MODULATOR

In this section we will introduce the vector modulator for performing the phase shift and amplitude scaling, and show how it can be implemented based on a switched-capacitor principle.

A. Vector Modulator Principle

The principle of a vector modulator is outlined in the phasor diagram in Fig. 4, spanned by the real and imaginary axis. The vector to a point Z in the phasor diagram corresponds to a phase shifted and amplitude scaled version of the input phasor. Z can be decomposed into a contribution on the real axis (X vector) and imaginary axis (Y vector) with different lengths according the desired amplitude A_n and phase φ_n :

$$\begin{aligned} Z &= X + Y \\ X &= I \cdot A \sin(\varphi) \\ Y &= Q \cdot A \cos(\varphi) \end{aligned} \quad (5)$$

Thus, X is a scaled version of I , the original In-phase input signal and Y is a scaled version of Q , the Quadrature (90

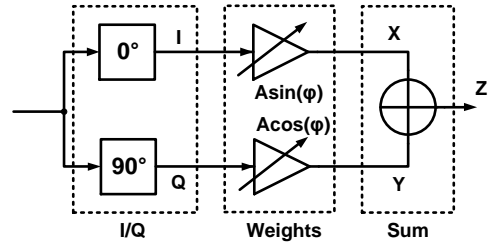


Fig. 5. Vector modulator block diagram.

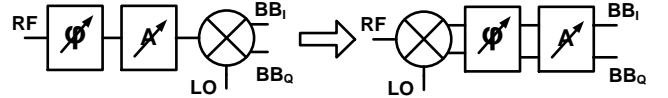


Fig. 6. IF phase shifting equivalency to RF phase shifting.

degree out-of-phase) version of the input signal. The steps in forming the amplitude scaled, phase shifted output Z from the input are given in the block diagram in Fig. 5. First, In-phase and Quadrature versions of the input are obtained. Then each is weighted to X and Y respectively with two variable gain blocks. Finally, the output Z is formed by summing X and Y .

B. Phase Shift through Sine/Cosine Approximation

An elegant way of obtaining the I and Q signal is to include downconversion into the vector modulator. As downconversion is a multiplication in the time domain, a mixer is transparent for phase and amplitude information. A phase shift and amplitude scaling at the RF port is therefore equivalent to the same phase shift and amplitude scaling at the IF port, as illustrated in Fig. 6. For image rejection in a zero-IF architecture, a quadrature mixer is desirable with accurate I/Q output, which can be reused as inputs for the vector modulator.

Furthermore, signals at baseband are often implemented differentially to reject common mode disturbances. From Fig. 4 it is apparent that the *negative* I and Q are also needed to address all four quadrants of the phasor diagram and get a full 0° to 360° phase shift range. This can be easily achieved by swapping the differential signal lines at baseband.

For the beam steering it was concluded that uniform phase steps are required, which require the lengths of the X and Y vector to vary according to the sine and cosine of the required phase shift (5). Such a variable gain is hard to implement in a robust fashion. Therefore it was proposed to instead implement an approximation to the sine with a rational function [11]:

$$\sin\left(\alpha \cdot \frac{\pi}{2}\right) \approx \frac{7}{4} \frac{\alpha}{\alpha + 3/4} \quad \alpha = [0, 1] \quad (6)$$

which are plotted in Fig. 7a. The α parameter ranges between zero and unity, corresponding to phase shifts from 0° to 90° degrees. The factor $3/4$ in the denominator is chosen to put the crossover point halfway, in order to minimize the approximation errors. The fraction is scaled to unity gain for $\alpha = 1$ by including the factor $7/4$. The same function can be

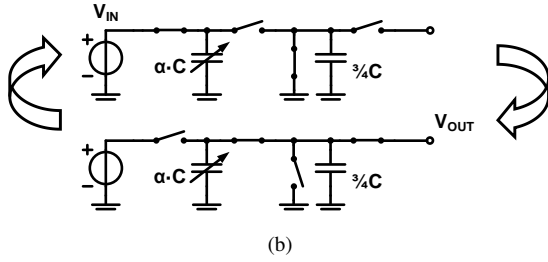
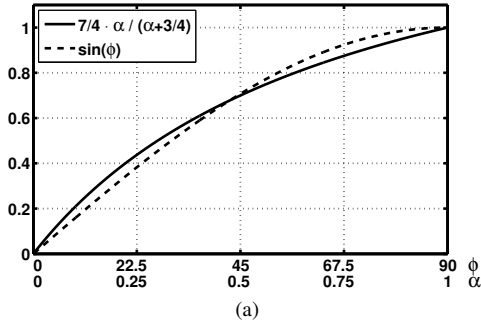


Fig. 7. Rational sine approximation (a) and implementation in a charge redistribution circuit in (b).

used to approximate the cosine, by substituting α with $1 - \alpha$:

$$\cos\left(\alpha \cdot \frac{\pi}{2}\right) = \sin\left(\frac{\pi}{2} - \alpha \cdot \frac{\pi}{2}\right) \approx \frac{7}{4} \frac{(1 - \alpha)}{(1 - \alpha) + 3/4} \quad (7)$$

The elegance of this approximation is that the rational part fits naturally on a voltage divider with variable impedance α and fixed impedance $3/4$. The implementation with a 2-phase switched-capacitor circuit is shown in Fig. 7b. In the first phase, variable capacitor αC is charged to voltage V_{IN} , creating charge $Q_1 = \alpha C \cdot V_{IN}$. At the same time, fixed capacitor $3/4C$ is emptied of its charge. In the second phase, the capacitors are connected together and charge redistributes until the capacitor voltages are equal. The charge for the second phase can be expressed as $Q_2 = (\alpha C + 3/4C) \cdot V_{OUT}$. Since charge is conserved, the transfer function evaluates to the required fraction as a function of α :

$$\frac{V_{IN}}{V_{OUT}} = \frac{\alpha}{\alpha + 3/4} \quad (8)$$

with a maximum transfer function of $4/7$ for $\alpha = 1$. Note that as long as the voltages are allowed to settle, the transfer function only depends on capacitor ratios, which can be accurately controlled in advanced CMOS. Moreover, With this rational approximation, the required *uniform* steps in phase correspond to *uniform* steps in alpha, and thus in *uniform* steps in capacitance. A simple binary scaled capacitor bank can therefore be used to implement the variable capacitance, with sine and cosine related transfer functions as a result.

As a final step, the X and Y vector have to be summed into Z. As the two-phase charge redistribution circuit produces an output for half the time, it is natural to interleave the processing of X and Y and de-interleave at Z with the configuration in Fig. 8. At the output, during clock phase A the Y signal is present and during clock phase B the X signal is present. After low pass filtering, these voltages will

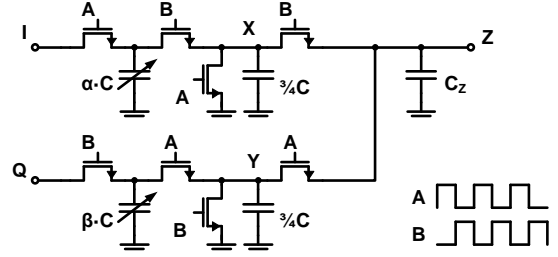


Fig. 8. Summing by interleaving.

be effectively averaged in the time domain. In the frequency domain, the interleaving can be regarded a folding of the signal around the LO harmonics. The low-pass filtering, which can already be achieved by the channel selection filter, removes these folded contributions and passes the baseband part of the spectrum.

For uniform phase steps with unity amplitude, α is set to $\varphi \cdot 2/\pi$ and β to $1 - \alpha$. Due to the approximation, systematic phase and gain errors are introduced. The gain error is rather small, but the phase error is between $\pm 4^\circ$. To ensure proper beamforming, a phase error smaller than half the smallest phase step is required. Using this criterion, the number of phase steps in this design is chosen to be 32, i.e. a total of 5 bit of phase control. This is split between 2 bits for the quadrant selection and 3 bits for the charge redistribution circuit.

The resulting constellation for the 32 phase steps is shown in Fig. 9a, together with the systematic phase and gain error. To avoid phase points from two quadrants overlapping on the real or imaginary axis, α and β are not quantized between 0 and 1, but between $1/16$ and $15/16$, i.e. a half LSB offset.

C. Balancing Phase and Gain Error

In the circuit of Fig. 8, any capacitance on node Z will introduce a memory effect. Charge from X and Y is retained on C_Z , resulting in a modification of the transfer function. The effect of this capacitance is shown in Fig. 9b for $C_Z = 3/8 \cdot C$. Compared to Fig. 9a (with $C_Z = 0$), the gain error increases while the phase error decreases.

The accuracy in phase affects the directions where constructive and destructive summing occurs, i.e. the pointing accuracy of the main beam and nulls. On the other hand, accuracy in gain affects the height of the main beam and the depth of the nulls. So the capacitance C_Z helps to balance the contributions of the phase and gain error to obtain a balanced performance. To find a proper balance, the equivalence between random gain and phase errors can be used as a criterion [1]:

$$\sigma_A = 20 \cdot \log_{10}(1 + \sigma_\varphi/180^\circ \cdot \pi) \quad (9)$$

where σ_φ is the rms phase error in degrees and σ_A is the rms gain error in dB. This equivalence is closely related to the realization that it is the error in *distance* in the phasor diagram which determines the beamforming performance, so that a distance in amplitude (axial) can be equated to a distance in phase (radial). For the case shown in Fig. 9a, the rms phase error is 1.3° and the rms gain error is 0.18dB, resulting in a balanced performance.

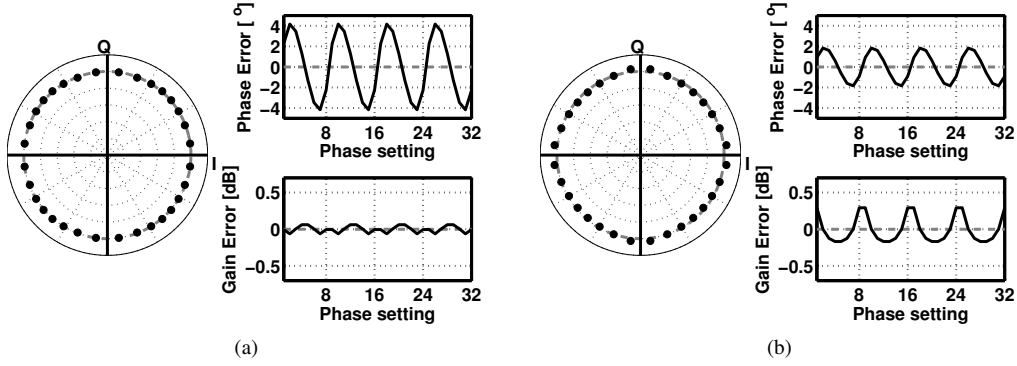


Fig. 9. Vector modulator phase and gain error for: (a) $C_Z = 0$, (b) $C_Z = 3/8C$.

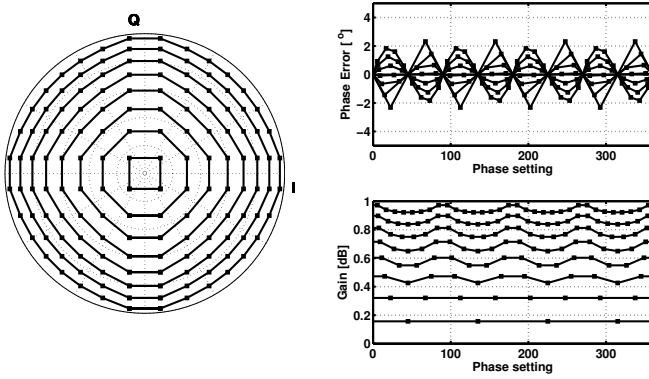


Fig. 10. Vector modulator constellation with phase and amplitude control.

D. Amplitude Control for Null Steering

In order to perform null steering, amplitude control has to be added to the vector modulator. With the proposed circuit in Fig. 7b, the amplitude A can be easily controlled by multiplying both α and β with the amplitude factor: $\alpha = A \cdot \varphi \cdot 2/\pi$ and $\beta = A \cdot (1 - \varphi \cdot 2/\pi)$. As α and β are quantized in 8 steps, 8 amplitude settings are available with decreasing number of phase steps. This is illustrated by the constellation in Fig. 10 of the vector modulator with amplitude and gain control, where phase points with equal gain settings are connected by lines. Due to the sine and cosine approximation, the amplitude control is non-uniformly quantized with more gain settings for higher amplitudes. This fits nicely to the requirements for the null steering algorithm, which produces amplitudes close to unity.

It is not trivial to calculate the effect of the non-uniform amplitude quantization on the resulting beam pattern. However, it is possible to estimate the finite null depth due to the uniform phase quantization. In the worst case, a null is needed on a direction of a grating lobe caused by the phase quantization. The height of a grating lobe below the main beam, QL , can be estimated in dB as [1]:

$$QL \approx 6M - 4 \quad (10)$$

where M is the number of bits in the phase shifter. This results in a rejection of 26dB for 5 bit phase quantization.

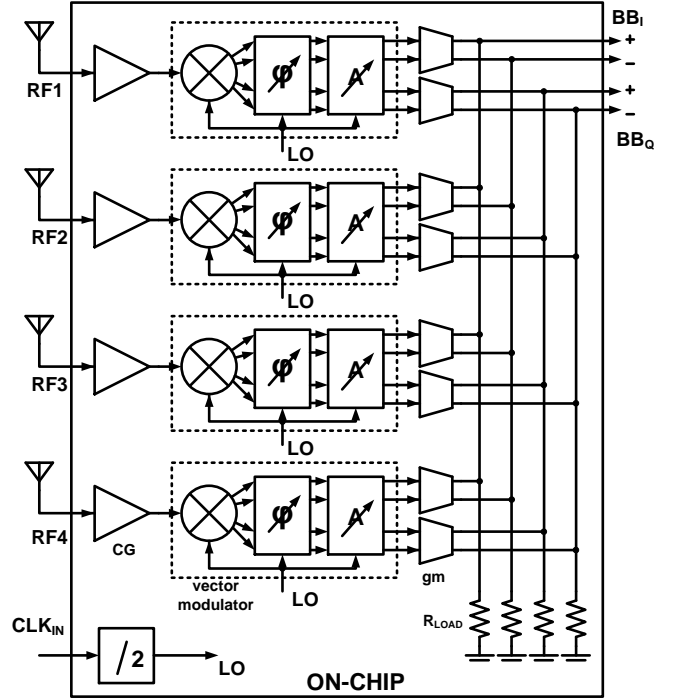


Fig. 11. Architecture of the 4-channel beamforming chip.

E. 4 Element Phased Array Receiver Architecture

To demonstrate null steering, the 4-element phased array receiver front end, depicted schematically in Fig. 11, was implemented. Each element is input matched with a common gate input stage. Downconversion takes place with an image-reject passive mixer, after which a switched-capacitor vector modulator performs the phase shifting and amplitude scaling. The vector modulator output voltages are converted to current with a gm stage and summed in the current domain. The summed current flows into the common load resistors R_{load} to provide the IC output voltages. To provide the clock for the mixer and vector modulator, a differential off-chip master clock is divided-by-two to generate a 4-phase 50% duty cycle LO.

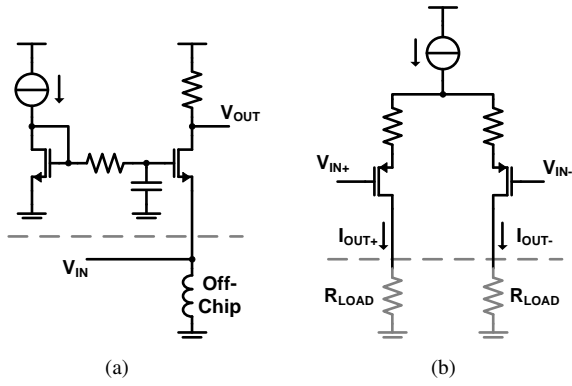


Fig. 12. Schematic of (a) common gate input match and (b) gm stage.

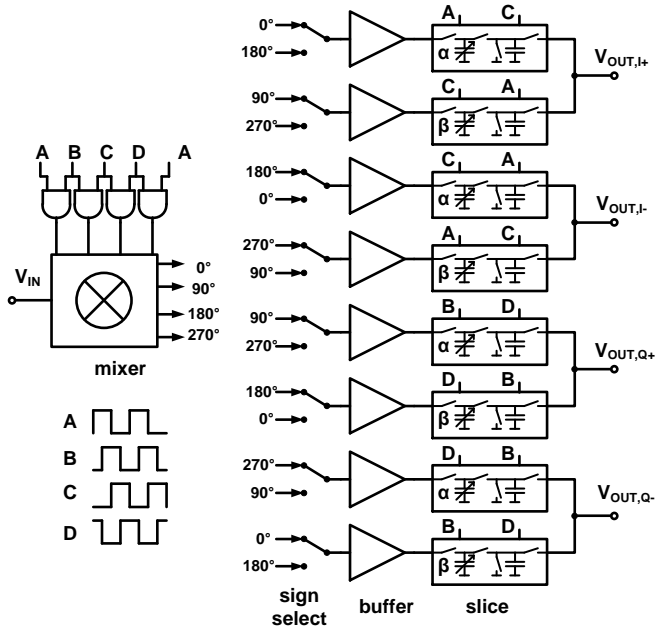


Fig. 13. Vector modulator driven by 4-phase LO.

F. Common gate and summing network

At each element input, the common gate amplifier in Fig. 12a is used to provide 50Ω input matching and give 10dB of voltage gain. After the vector modulator, a differential source degenerated differential pair with tail current source acts as a gm stage (Fig. 12b). Both stages are designed for good linearity and high gain compression point, to prevent interferers from distorting reception before they are canceled with beamforming.

G. Mixer and Vector Modulator

The block schematic of the combined mixer and vector modulator is shown in Fig. 13. For a zero-IF image rejection architecture, differential I/Q phase shifted and amplitude scaled output signals are required. Therefore, the charge redistribution circuit of Fig. 8 is repeated four times. This has the added benefit that the load to each mixer output is always the same. Eight buffers are used to drive the vector

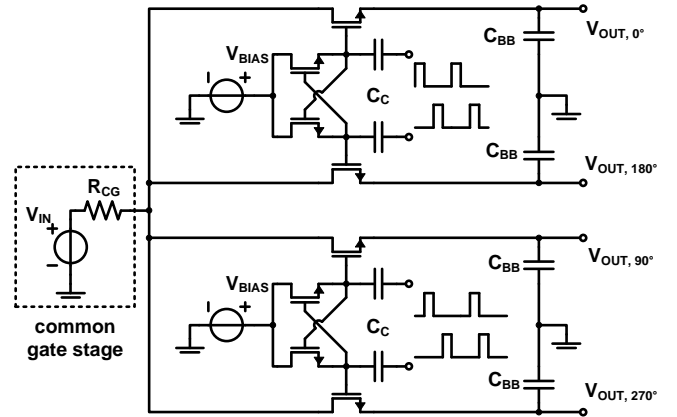


Fig. 14. 4-phase 25% duty cycle passive mixer.

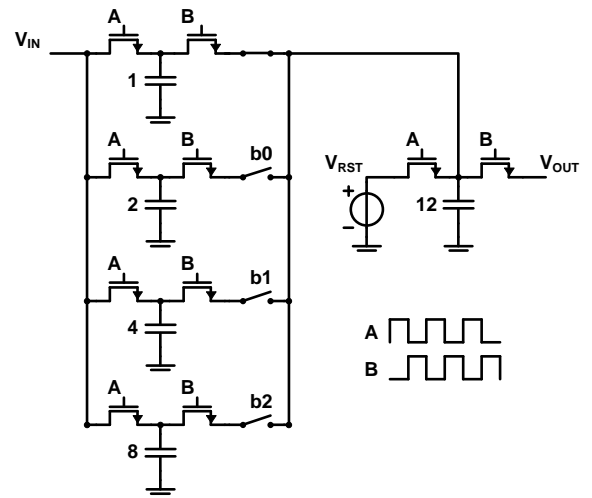


Fig. 15. Charge redistribution slice.

modulator slices, with switches at the input to select the sign of the mixer output, which in turn selects the quadrant of the phasor diagram.

Downconversion takes place with a quadrature sampling mixer [12] in Fig. 14. The input is rotated between four capacitors, requiring switches driven by a 4-phase 25% duty cycle square wave LO. This clock is obtained by performing the AND operation between 50% duty cycle clock phases. The time constant of $R_{CG} \cdot C_{BB}$ is much larger than the switch on-time, so that voltage mixing occurs with built-in baseband 1st order filter [13]. This mixer pole is the dominant baseband receiver pole and set to 65MHz. The voltage overdrive of the switches is maximized by raising the LO with V_{bias} , the bias voltage on the sources and drains of the mixer switches. This is accomplished by adding cross coupled transistors and coupling capacitors C_C . When a cross coupled transistor is turned on, the associated coupling capacitor C_C is connected to the voltage source on the left plate and to zero voltage on the right plate. This conveniently charges C_C to voltage V_{bias} when the clock is low and the switch is off.

Each vector modulator slice is implemented with the circuit in 15. A 3 bit binary capacitor bank is implemented with the

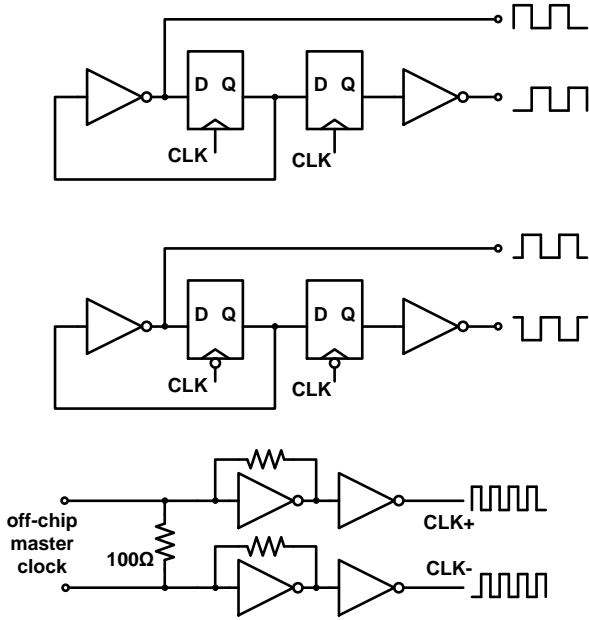


Fig. 16. Clock divider.

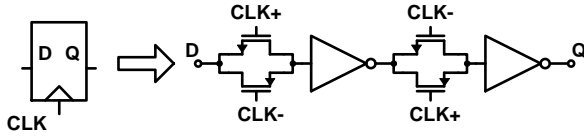


Fig. 17. Dynamic latch logic flipflop.

three lower, binary weighted parallel paths. Integer capacitor ratios are acquired by multiplying the rational function (6) with 16, with a unit capacitor of 160fF. The switches are scaled along with the capacitors to ensure binary scaling of the switch parasitic capacitance. The upper path is added for the half LSB offset (always on), which also ensures a path is always present for proper biasing of the next stage. The output capacitor is reset to the proper bias voltage of the gm stage, as to not disturb its bias. The gm stage itself is scaled to present the correct input capacitance needed for a balanced phase and gain error.

As the mixer and vector modulator run at the same frequency and process at the same sample rate, frequency folding is limited to the already present harmonic up- and downmixing of the mixer. In fact, the vector modulator re-uses the RF and channel filter, to perform anti-aliasing and sample reconstruction.

H. Clock generation

In Fig. 16 the block schematic of the clock divider is given. A sinusoidal differential master clock running at twice the LO frequency is first amplified by dual inverter stages. This drives the flipflops in two divide-by-two loops, one triggering on the rising edge and the other triggering on the falling edge. Each flipflop is implemented with transmission gated inverters, shown in Fig. 17.

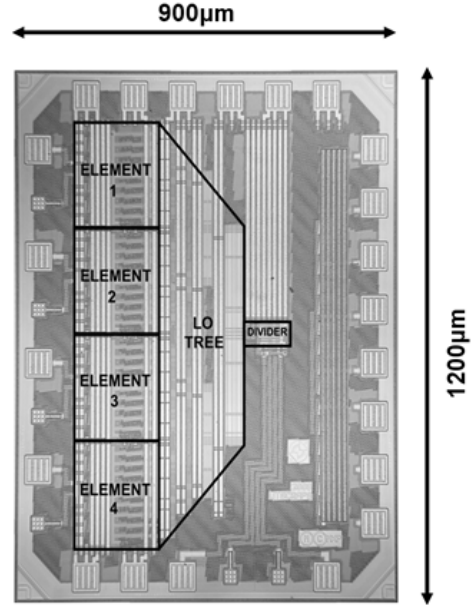


Fig. 18. Die photo.

Any mismatch in the clock phases reflects in I/Q imbalance and thus causes phase and gain errors in the vector modulator. This clock divider has a low delay from the LO to the output path, resulting in low mismatch [11]. The maximum LO frequency is limited by the speed of the CMOS logic, especially the master clock input inverters. This limits the maximum LO frequency to 4 GHz in 65nm CMOS.

IV. MEASUREMENTS

The chip is implemented in 65nm CMOS (die photo in Fig. 18) and has an active area of 0.44 mm². The beamforming receiver works up to 4 GHz with a -3dB bandwidth after downconversion of 65MHz. With a 1.2V supply, the static power consumption is 120mW, and an additional 188mW dynamic power consumption for 2.5GHz LO, which scales linearly with LO frequency.

Measurements on a single element are plotted in Fig. 19 for LO frequencies between 1 and 4 GHz. In the middle of the RF range at 2.5GHz LO, a gain of 16dB (from the input to the differential I output), DSB NF of 10dB and in-band input referred compression point of -14dBm are measured. In-band input referred IP3 is -1dBm. For the total 4 element array the SNR is improved with 6dB in the main beam, resulting in an array sensitivity equivalent to a 4-5dB NF single antenna receiver.

The measured vector modulator phasor diagram for a single element is shown in Fig. 20. Compared with the theoretical constellation in Figure 10, the rms phase error is as predicted and the rms gain error has increased to 0.4dB. This is probably due to the parasitic layout capacitance on node Z in Fig. 8 and capacitive coupling between source and drain of the switches.

Thanks to the good matching of capacitor ratios in the proposed vector modulator and the accurate LO generation, the mismatch of vector modulator constellations between different dies is very low (Fig. 21). Random rms phase and gain

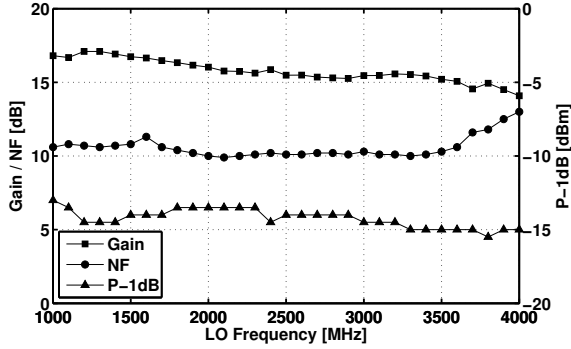


Fig. 19. Measured receiver element gain, NF and compression point.

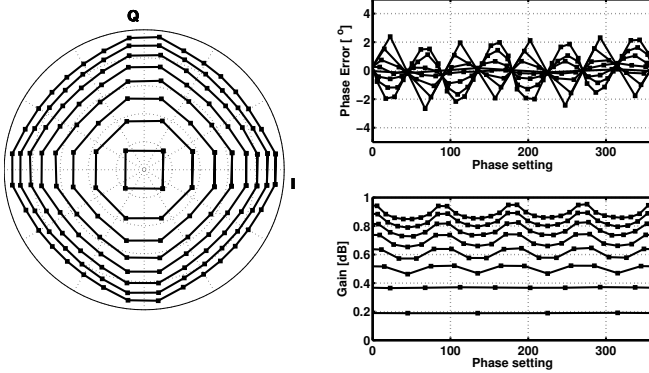
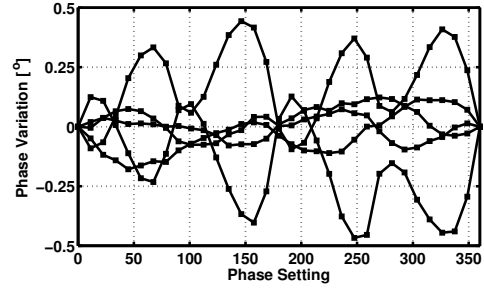


Fig. 20. Measured vector modulator constellation.

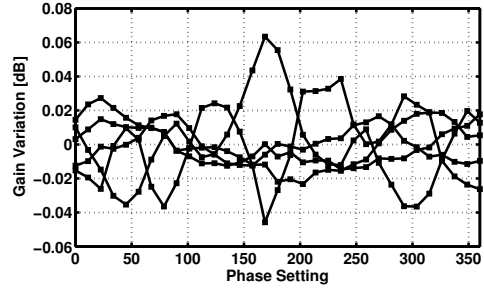
error are 0.2° and 0.04dB respectively. It is expected that the constellation is also insensitive to process spread and temperature.

To evaluate the spatial interferer rejection, the setup in Fig. 22 uses four signal generators to emulate the incoming phase front from an antenna array and thus directly measure the array factor. The generators have well matched frequencies due to locked reference crystals, but the initial phase differences are unknown. These phase differences are calibrated out with a network summing the generator output powers, utilizing destructive summing to detect the phase difference between pairs of generators. The residual phase and gain errors between the chip inputs are estimated to be 1° and 0.2dB respectively. In the setup, PCB micro strip coupling introduces -20dB coupling between adjacent RF inputs, a situation similar to the coupling between antennas in an array. The interferer nulling algorithm from section II is used to produce vector modulator settings that give an array factor with a main beam at 30° and a null between -60° and 15° . The measured patterns are plotted in Fig. 23. Even though the null is steered up to only 15° from the main beam, a spatial rejection of more than 20dB is reached for this 4-element beamformer. In light of the additional errors introduced by the measurement setup, this is not far off from the initial estimate of 26dB of spatial interferer rejection.

The measured performance is summarized in Table I. To the author's knowledge, no similar phased arrays in the same frequency band have been published to make a comparison with.



(a)



(b)

Fig. 21. Measured (a) phase and (b) gain variations between 5 dies for the maximum amplitude phase settings.

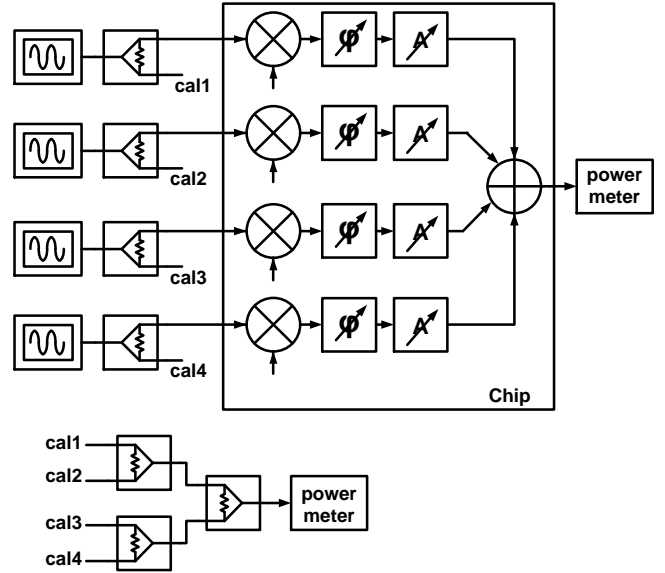


Fig. 22. Setup with phase calibration for measuring array factors.

V. CONCLUSIONS

In this work we have presented a 4-element beamforming receiver front end with a switched-capacitor vector modulator. The vector modulator uses a rational approximation for the sine and cosine to generate the required uniform phase steps and non-uniform amplitude steps for null steering. The switched capacitor implementation with 5 bit phase control and 3 bit amplitude control achieves an rms systematic phase and gain error of 1.4° and 0.4dB respectively. A spatial interference rejection $>20\text{dB}$ is demonstrated, severely alleviating the linearity requirements of the baseband circuitry.

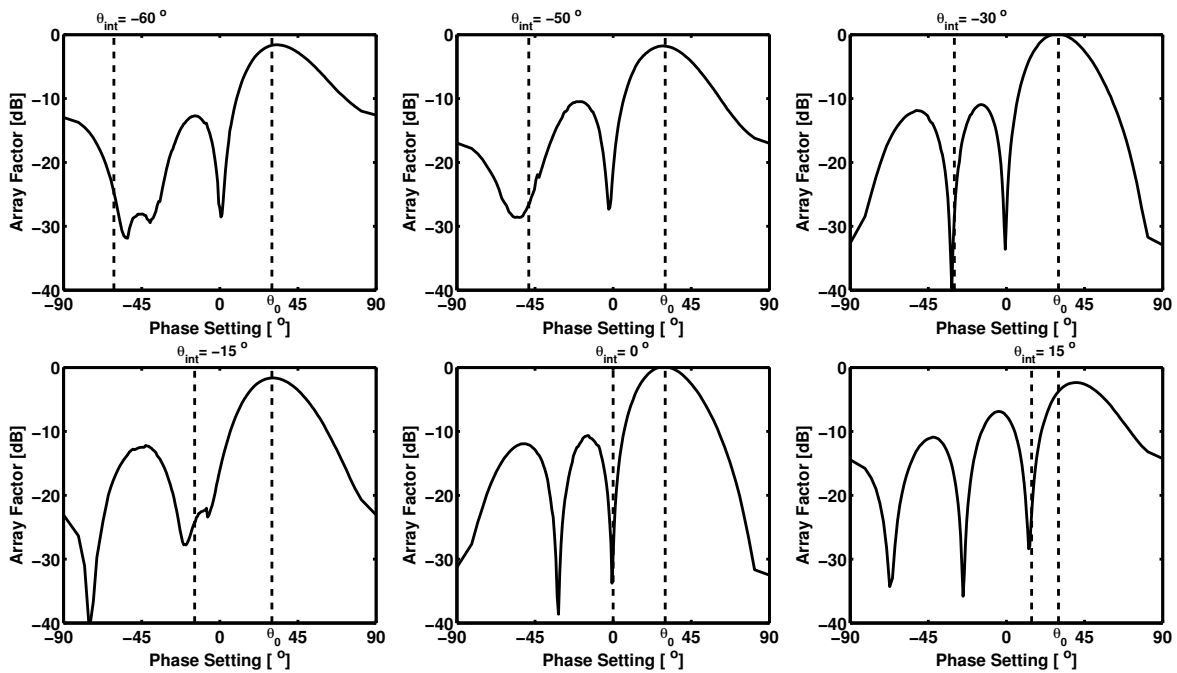


Fig. 23. Measured array factors with main beam at 30° and null steered to -60° , -50° , -30° , -15° , 0° and 15° .

TABLE I
PERFORMANCE SUMMARY

Phased Array:	
Technology	65nm CMOS
Die area	$0.9 \times 1.2 \text{ mm}^2$
RF frequency band	1 - 4GHz
Power consumption	308mW @ 1.2V ^a
Array directivity	6dB (4 elements)
Element phase mismatch (RMS)	0.2°
Element amplitude mismatch (RMS)	0.04dB
Main beam-to-null ratio	> 20dB

^a 120mW static, 188mW dynamic @ 2.5GHz RF

Single Element:	@ 2.5GHz RF
Gain	16dB
Noise figure	10dB DSB ^b
1dB compression point	-14dBm
In-band IIP3	-1dBm
In-band IIP2	40dBm
Phase control	5 bit
Amplitude control	3 bit
Phase error (RMS)	1.4°
Amplitude error (RMS)	0.4dB

^b Additional 6dB SNR improvement for full array

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