Micromachining of High-Contrast Optical Waveguides in ⟨111⟩ Silicon Wafers

G. Pandraud, G. Veldhuis, J. W. Berenschot, A. J. Nijdam, H. J. W. M. Hoekstra, *Member, IEEE*, O. Parriaux, and P. V. Lambeck

***Abstract*—A fabrication technique by KOH etching for very thin free standing plane parallel silicon bridges in a {111} silicon wafer is presented. The applications of such a stress free slab as an evanescent optical waveguide sensor of unusually high sensitivity are discussed.**

***Index Terms*—Etching, integrated optics, silicon, waveguides, sensors.**

I. INTRODUCTION

INTEGRATED optical devices are increasingly being used in (bio-)chemical sensing applications [1]. Usually, a change of absorption or the change of refractive index caused by an analysis above the waveguide sensor surface is monitored. The main design task for each application is to find a structure which maximizes the sensitivity on the quantity to be measured. It has recently been shown that a symmetrical waveguide with a large contrast between the waveguide index and the surrounding medium exhibits an unusually high sensitivity [2]. In the case of a water or gas cover, a very large contrast is obtained by using a pure silicon waveguide.

Several authors have reported on various techniques for making optical waveguides in or on crystalline silicon [3], [4]. Planar and rib waveguides formed from silicon-on-insulator (SOI) have exhibited losses significantly lower than 1 dB/cm, in the 1.3–1.55-μm wavelength range [5]. Free carrier plasma dispersion has been demonstrated in silicon waveguides as a method of modulating the refractive index [6]. The combination of these attractive features with the ease of device fabrication using well-established silicon microelectronic processing is leading to a growing interest in SOI integrated optical circuits for optical sensor and communication applications. In this work, an alternative procedure, and different processes have been developed for producing single crystal silicon waveguides. These consist of very thin free standing silicon bridges defined on a standard ⟨111⟩ oriented silicon wafer. We show in this letter that such bridge waveguide structure (which has mostly been considered so far for photonic band gap research) exhibits highly sensitive features which can profitably be used in shorter term sensor applications.

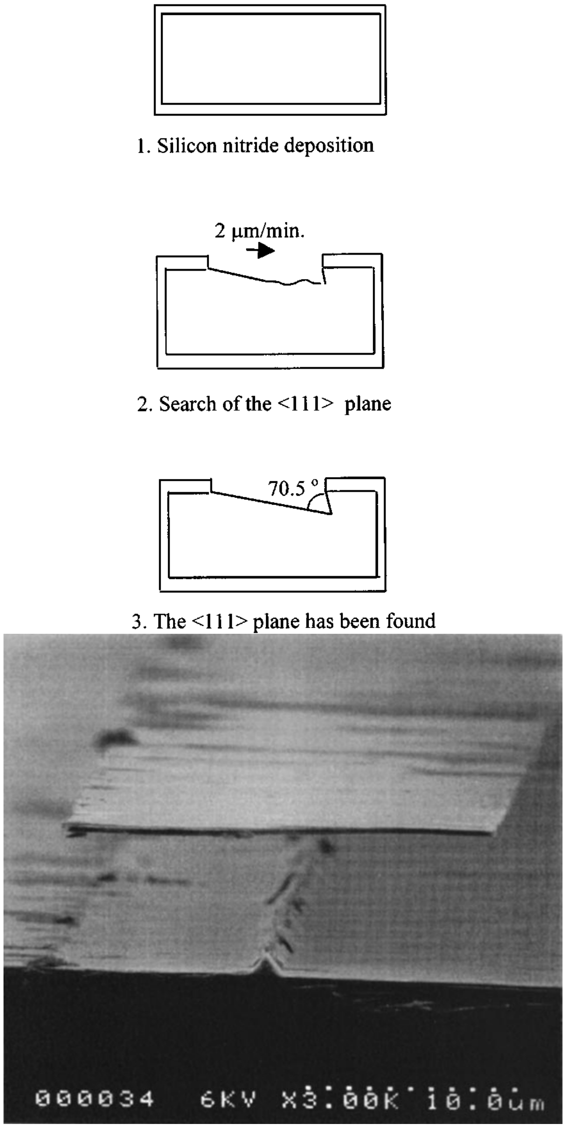


Fig. 1. Plane parallel silicon bridges. (a) Preetching step. (b) SEM picture.

A. Structure Fabrication

The material is a ⟨111⟩ orientation silicon wafer. Commercial standard wafers usually are cut 1° ± 0.5° off-axis. This means that the ⟨111⟩ crystal orientation is not perfectly parallel to the surface of the wafer. Wafers of more precise orientation can be ordered, but even these will never be cut parallel to the ⟨111⟩

Manuscript received September 7, 1999; revised November 23, 1999.

G. Pandraud is with the Bookham Technology Ltd., Abington, Oxfordshire OX14 4RY, U.K.

G. Veldhuis, J. W. Berenschot, A. J. Nijdam, H. J. W. M. Hoekstra, and P. V. Lambeck are with the MESA Research Institute, Twente University, NL-7500 AE Enschede, The Netherlands.

O. Parriaux is with the Laboratoire TSI, UMR CNRS 5516, Université Jean Monnet, F-42023 Saint Etienne, France.

Publisher Item Identifier S 1041-1135(00)02007-3.

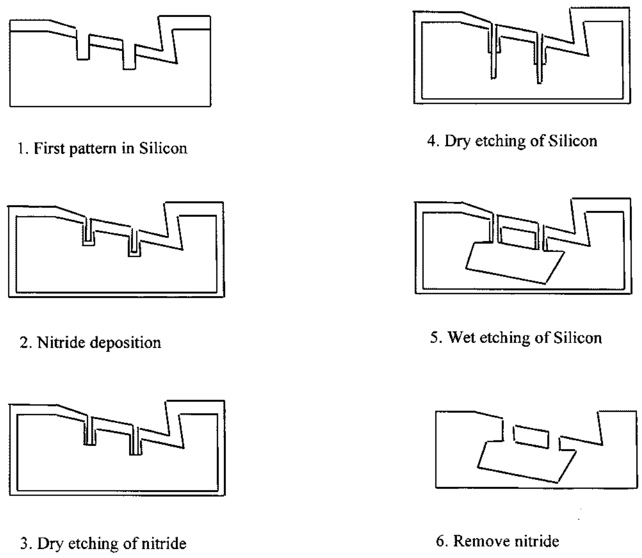
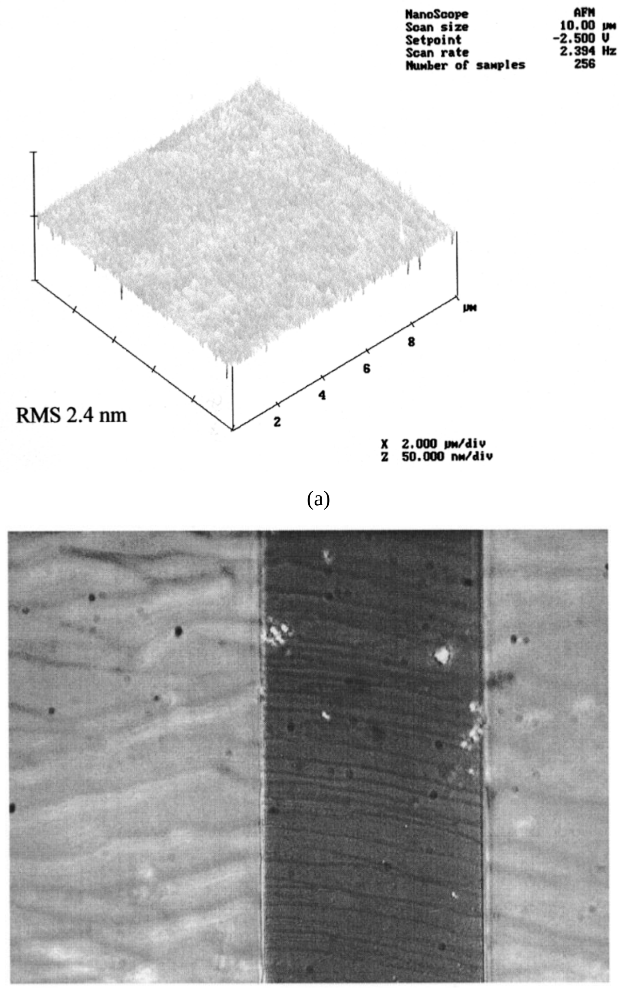


Fig. 2. Process flow for the fabrication of single crystal silicon bridges.



(a)

(b)

Fig. 3. (a) AFM scan and (b) microscope picture of the top surface of a bridge.

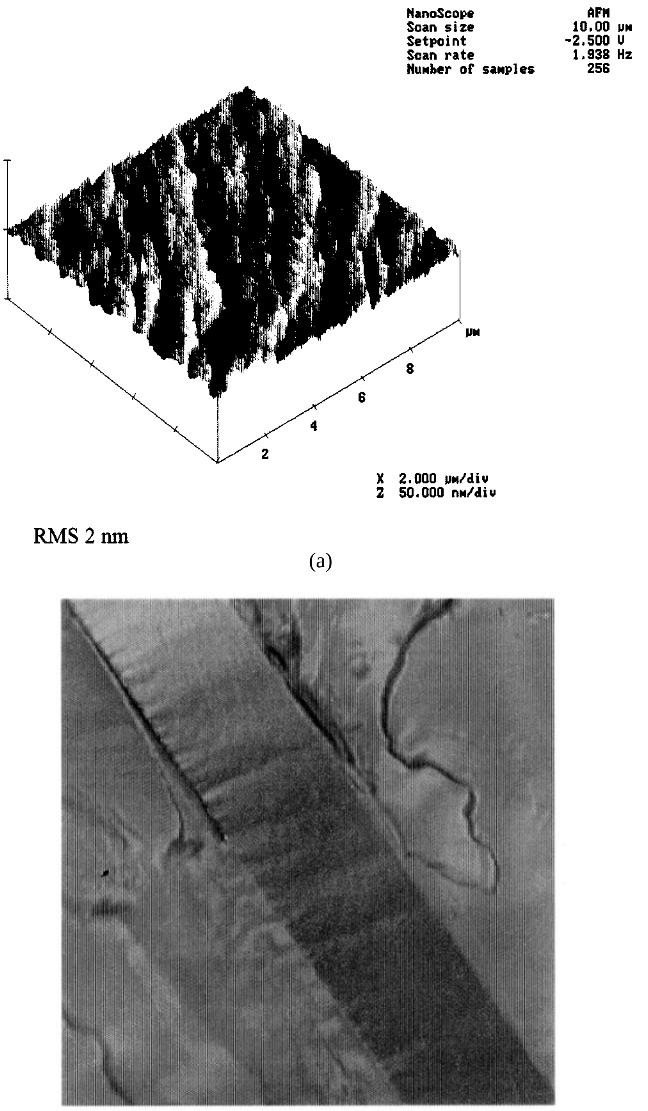
direction at the atomic scale. In order to fabricate plan parallel silicon bridges, we start with a KOH pre-etching step to obtain a wafer surface perfectly parallel to the ⟨111⟩ crystal orientation as shown in Fig. 1(a). To that end, a masking layer of silicon nitride is deposited on the ⟨111⟩ oriented wafer. Then a photolithography step and a dry etching of the nitride define an opening on the silicon surface. Immersing the wafer in 25 wt% KOH at 70 °C, the ⟨111⟩ plane is revealed. The etching rate is slow and depends on the angle between the ⟨111⟩ plane and the wafer surface. For standard wafers presenting an angle of $1^\circ \pm 0.5^\circ$ the etching rate to find the ⟨111⟩ plane is about 2 μm/min. Once the preetching step is ended and the new wafer surface is a ⟨111⟩ plane, the silicon nitride layer is removed in 50% HF.

The second phase for the micromachining of plane parallel bridges is described in Fig. 2 and is based on [7]. A first photolithography step defines the in-plane shape of the structures that are to be micromachined. Using a thick patterned resist layer, silicon is dry etched to a depth equal to the thickness required for the final bridge waveguide. After stripping off the resist layer, a LPCVD silicon nitride layer is deposited uniformly. Then a new photolithography step is performed using a mask with openings smaller than in the previous step. The silicon nitride film and the silicon substrate are then dry etched and the wafer is immersed in KOH after removing the resist layer. The etch rate is orientation dependent, so the etchant removes the silicon laterally and parallel to the ⟨111⟩ direction and under the bridges. The bottom of the structure is protected by virtue of the fact that it is a ⟨111⟩ plane and thus etches very slowly in KOH [8]–[10]. Finally, the silicon nitride etch stop is removed using 50% HF. Possible sticking problems during cleaning are avoided by etching deeper under the bridge.

B. Results

Performing the preetching step and the procedure sketched in Fig. 2, we obtained the device shown in Fig. 1(b). Here, a 20-μm-wide and 210-nm-thick (limit of the proposed fabrication scheme) bridge is shown. Such bridges can be used as waveguides, ridge waveguides or gratings [12] that can be etched down after the ⟨111⟩ plane has been found. Light could be easily coupled from free space into one surface grating and then coupled out of the waveguide from a second grating back into free space.

In order to assess the potential use of such bridges as optical elements a measurement of the residual roughness, resulting from the etching process, has been made. Fig. 3(a) and (b) shows an AFM scan and a microscope picture of the top of a bridge respectively. A surface roughness of 2.4 nm, after the KOH preetching step, was measured. The microscope picture shows a uniform surface. In order to make a scan of the surface of the underside of a bridge, an adhesive tape was stuck on the top of a bridge. Tearing it away made the bottom side accessible. Fig. 4 presents an AFM scan a) and a microscope picture b) of the bottom of a bridge. The rms roughness is 2 nm and the surface does not show any staircase resemblance. Using Marcuse's perturbation analysis, Rickman [12] calculated the scattering loss for a silicon core/air clad planar waveguide. For a 1-μm thickness and a 20-nm roughness waveguide, the scattering losses at 1.523 μm for the TE_0 mode are about 40 dB/cm. However, interface induced scattering is proportional to the square of the roughness, so, the proposed process, characterized by a roughness of 2 nm, can be expected to lead to scattering losses significantly lower than 1 dB/cm.



(a)

(b)

Fig. 4. (a) AFM scan and (b) microscope picture of the bottom surface of a bridge.

C. Discussion

The rapid development of optical communications and the development of microsystems toward optoelectronic integration technologies open new possibilities to single crystal silicon integrated optics. A number of groups are active in this domain [13] where industrial interests have started offering products [14]. So far, most R&D work is based on the SOI technology [13]. This is not a low cost technology yet and the supply of SOI wafers still relies upon a restricted number of industrial laboratories.

In contrast with the SOI technology, the slab silicon waveguide technology presented here uses standard wafers. It primarily leads to waveguides of high contrast. Applications in the communications field have already been proposed such as large FSR microring resonator dropping filters at 1.55-μm wavelength [15]. It is probably in the field of sensors, where manufacturing cost is a key factor, that the proposed technology for the fabrication of symmetrical waveguides using a standard $\langle 111 \rangle$ wafer is the most promising. Silicon is transparent in the wavelength range of the mid-IR where a large number of gases have strong absorption bands. Long interaction lengths are possible and the scattering effects of the residual roughness is dramatically reduced. Such characteristics are attractive for environmental applications [16].

In addition, a number of other sensors and microsystems can advantageously use free standing silicon thin films [17].

II. CONCLUSION

A low-cost process for producing symmetrical single crystal silicon slab waveguides is described. The resulting structure has the potential of becoming a building block for a number of optical microsystems such as unusually large sensitivity evanescent sensors as well as modulators, resonators and filters. The described technology is a complement to the better known SOI based waveguide technology and can also be a lower cost alternative.

ACKNOWLEDGMENT

The authors would like to thank T. Andringa for his assistance in silicon nitride deposition and valuable advices.

REFERENCES

[1] R. E. Kunz, “Miniature integrated optical modules for chemical and biochemical sensing,” *Sens. Actu. B*, vol. 38, pp. 13–28, Jan. 1997.
[2] G. J. Veldhuis, O. Parriaux, H. J. W. M. Hoekstra, and P. V. Lambeck, “Sensitivity enhancement in evanescent optical waveguide sensors,” *J. Lightwave Technol.*, submitted for publication.
[3] B. N. Kurdi and D. G. Hall, “Optical waveguides in oxygen-implanted buried oxide silicon-on-insulator structures,” *Opt. Lett.*, vol. 13, pp. 175–177, 1988.
[4] R. A. Soref and J. P. Lorenzo, “All-silicon active and passive guided-wave components for $\lambda = 1.3$ and 1.6 μm,” *J. Lightwave Technol.*, vol. LT-22, pp. 873–879, 1986.
[5] J. Schmidtchen, A. Splett, and B. Schuppert, “Low contrast single-mode optical waveguides with large cross section in silicon-on-insulator,” *Electron. Lett.*, vol. 27, pp. 1486–1487, Aug. 1991.
[6] G. V. Treyz, “Mach-Zender waveguide interferometers operating at 1.3 μm,” *Electron. Lett.*, vol. 27, pp. 118–120, Jan. 1991.
[7] G. Ensell, “Free standing single-crystal silicon microstructures,” *J. Micromech. Microeng.*, vol. 5, pp. 1–4, 1995.
[8] D. B. Lee, “Anisotropic etching of silicon,” *J. Appl. Phys.*, vol. 46, pp. 4569–4574, 1969.
[9] H. Seidel, L. Cespregi, A. Heuberger, and H. Baumgärtel, “Anisotropic etching of crystalline silicon in alkaline solutions I., orientation dependence and behavior of passivation layers,” *J. Electrochem. Soc.*, vol. 137, pp. 3612–3626, 1990.
[10] K. Sato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, “Characterization of orientation-dependent etching properties of single-crystal silicon: Effects of KOH concentration,” *Sensors and Actuators A*, vol. 64, pp. 87–93, Jan. 1998.
[11] W. Lukosz, D. Clerc, and P. M. Nellen, “Input and output grating couplers as integrated optical biosensors,” *Sens. Actu. A*, vol. 25–27, pp. 181–184, 1991.
[12] S. Yegnanarayanan, P. D. Trinh, F. Coppinger, and B. Jalali, “Compact silicon-based integratde optic time delays,” *IEEE Photon. Technol. Lett.*, vol. 9, pp. 634–635, May 1997.
[13] “Associations,” in *Bookham Technol.*, 1998.
[14] A. G. Rickman, G. T. Reed, and F. Namavar, “Silicon-on-insulator rib waveguide loss and mode characteristics,” *J. Lightwave Technol.*, vol. 12, pp. 1771–1776, Oct. 1994.
[15] B. E. Little, S. T. Chu, H. A. Haus, J. Foresi, and J. P. Laine, “Microring resonator channel dropping filters,” *J. Lightwave Technol.*, vol. 15, pp. 998–1005, June 1997.
[16] J. X. Fang, H. F. Taylor, and H. S. Chol, “Fiber-optic Fabry-Perot flow sensor,” *Microwave Opt. Technol. Lett.*, vol. 18, pp. 209–211, June 1998.
[17] G. Veldhuis, C. Gui, T. Nauta, T. M. Koster, J. W. Berenschot, P. V. Lambeck, J. G. E. Gardeniers, and M. Elwenspoek, “Mechano-optical on/off intensity switch,” *Opt. Lett.*, vol. 23, pp. 1532–1534, 1998.