Analysis of the Electrical Breakdown in Hydrogenated Amorphous Silicon Thin-Film Transistors

Nataša Tošić Golo, Fred G. Kuper, *Member, IEEE*, and Ton J. Mouthaan, *Member, IEEE*

***Abstract*—Electrical breakdown induced by systematic electrostatic discharge (ESD) stress of thin-film transistors used as switches in active matrix addresses liquid crystal displays has been studied using electrical measurements, electrical simulations, electrothermal simulations, and postbreakdown observations. Breakdown due to very short pulses (up to 1 μs) shows a clear dependence on the channel length. A hypothesis that electrical breakdown in the case of short channel TFTs is due to the punch-through is built on this dependence and is proved by means of electrical simulations. Further, the presence of avalanche breakdown in amorphous silicon thin-film transistors is simulated and confirmed. It is finally assumed that the breakdown is a thermal process. Three-dimensional (3-D) electrothermal simulations are performed in the static and transient regime, confirming the location of the breakdown spot within the TFT from the electrical simulations and postbreakdown observations.**

***Index Terms*—Electric breakdown, liquid crystal displays, semiconductor device reliability, thin-film devices.**

I. Introduction

AMORPHOUS silicon thin-film transistors (a-Si : H TFTs) based on hydrogenated amorphous silicon have been used as switches in active matrix addressed LCDs, in fingerprint and image sensors, etc. Transistors used in this investigation are designed with top-gate (staggered) structure, with Si_xN_y as the gate dielectric (Fig. 1). The TFT technology is published elsewhere (see for example [1]). In Fig. 1, a typical set of measured current–voltage (I–V characteristics is shown. The device physics is similar to the crystalline MOS devices. A typical threshold voltage is 6 V. Electron mobility in a-Si is very low (<1 cm^2/Vs). The active matrix liquid crystal displays that are made in thin film technology have been shown to exhibit excellent video performance and display uniformity. TFTs on glass plates are very sensitive to electrostatic discharge (ESD) damage. Here, ESD-sensitivity on the drains of grounded gate TFTs is investigated.

In our earlier experiments with stepped electrostatic discharge, stress on top-gate hydrogenated amorphous in amorphous silicon thin-film transistors, it was shown that the breakdown voltage depends strongly on the channel length [2] (see also Fig. 3). Namely, it was shown that the shorter channel length corresponds to the lower breakdown voltage.

In this paper our attention is focused on finding the physical reasons and the explanation of this dependence. The electrical breakdown of a-Si : H TFTs is elucidated with measurements and simulations.

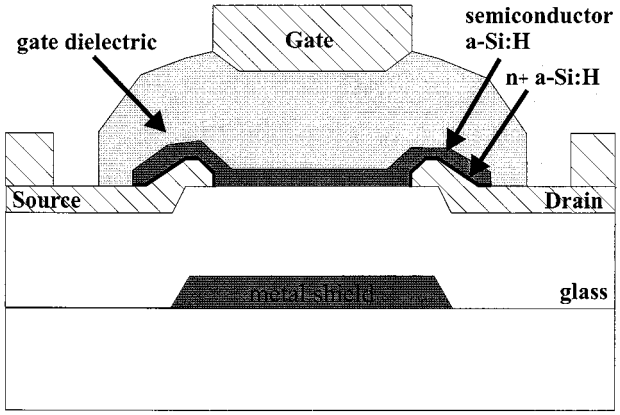

Fig. 1. Layout of a TFT.

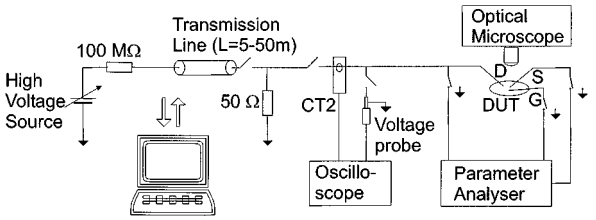

Fig. 2. Transmission line model experimental setup.

II. Experimental Data Analysis

A. Experimental Set-Up

In order to study breakdown behavior under electrical bias the following measurements have been carried out. The breakdown voltage under ESD stress has been measured by the transmission line model (TLM). The TLM system, shown in Fig. 2, was previously introduced for the studying of the transient behavior of electrostatic discharge protection devices for the IC circuits [3]. The TLM voltage pulse generator was typically set up with a pulse width of 100–1000 ns. That is a pulse duration that must be considered as rather long for an ESD investigation. In the case of a-Si : H TFTs such a long pulse was needed, as due to large resistivity of amorphous silicon, the RC time of the device is rather long (<100 ns) so that short pulse measurements would not always give correct results. The same

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TABLE I
BREAKDOWN VOLTAGES IN A SAMPLE WITH VARIATIONS OF W AND L

W/L	sample A1	sample B1	sample C1	mean value
100/10	420	450	410	427
100/100	430	440	400	423
8/9	430	430	400	420
4/9	430	430	400	420
10/9	420	420	400	413
18/9	410	410	400	407
6/9	420	420	390	410
100/9	410	400	370	393
100/8	370	370	320	353
14/7	350	330	300	327
100/6	280	280	260	277
10/5	260	240	230	243
100/4	210	190	190	197

experiments repeated for other pulse widths are investigated earlier in [4]. In these experiments the change of the parameters (like threshold voltage, transconductance, sub-threshold voltage) during the stress is monitored.

B. Experimental Results

The breakdown voltage under TLM pulse is defined as the voltage at which the drain current increases sharply and is accompanied with a decrease in the drain voltage. The results presented here concern:

- breakdown voltage versus channel width and channel length;
- breakdown voltage versus pulse length.

An overview of the TFTs with variety of the channel length and width tested by the TLM measurement system is given in Table I. These TFTs are designed for testing and manufactured by Flat Panel Display Co., The Netherlands.

From the data shown in Table I, it can be quickly concluded that breakdown voltage depends on the channel length and does not depend on the channel width (from the fact that the TFTs with the constant channel length $L = 9\,\mu$m and with different channel widths did not show noticeable variations of the breakdown voltage). The dependence of the breakdown voltage versus the channel length, which is extracted from the data shown in Table I, is separately plotted in Fig. 3. Fig. 3 shows that breakdown voltage depends almost linearly on the channel length for the short channel TFTs. That stands for the channel lengths of $L < 10\,\mu$m. For long channel TFTs ($L \geq 10\,\mu$m) the breakdown voltage stays constant with an approximate value of $Vbr = 425$ V.

Beside the breakdown voltage measurements in the sample consisting of the TFTs with W and L variations, another experiment is carried out in order to get a better insight in the breakdown physics. Namely, the breakdown voltage was

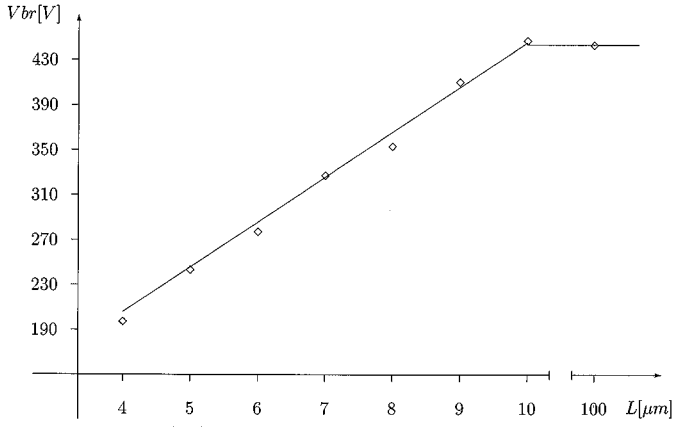

Fig. 3. Mean value of the breakdown voltage versus the channel length.

TABLE II
BREAKDOWN VOLTAGES OF THE TFTS WITH $W/L = 18/9$ TESTED BY THE TLM STRESS OF DIFFERENT PULSE LENGTHS

	100ns	300ns	500ns	$1\mu s$
sample T1	430	420	400	380
sample T2	430	430	400	380
sample T3	470	x	380	360
sample T4	470	x	370	360
sample T5	x	x	380	360
mean value	450	425	386	368

measured for different duration of the TLM stress pulse. Differences in breakdown voltage due to difference in channel lengths/batches, mask possible difference in breakdown voltages due to difference pulse lengths. Therefore for the following experiments samples with a number of TFTs with constant W/L ratio (18/9) were used. These samples were also manufactured for testing purpose only, by Hosiden, Japan. The technology used for samples A1, B1, C1 and T1–T5 was similar (same process flow), but not the same (different geometry of the photolithography masks). Therefore some differences in the measured results can be noticed. In Table II, the breakdown voltages of tested TFTs are listed. These TFTs were stressed with TLM pulses with pulse lengths of 100 ns, 300 ns, 500 ns, and 1 μs. It should be noted that the large ($\sim$100 ns) rise/fall time of the TFT has to be taken into account. Sign x in Table II is used in the case when there are no measured data. The data from Table II are graphically presented in Fig. 4. The experimental data show that the breakdown voltage lowers when the TLM stress time increases. Unfortunately the number of data points in the Fig. 4 is not enough for a reliable extrapolation.

C. Discussion of Experimental Results

The conclusion that we can draw from the experimental is that the breakdown voltage apparently depends on the channel length and does not on the channel width. In the TFTs with the channel length $L < 10\,\mu$m, so-called short-channel effects, similar as in the standard crystalline devices, occurs and the breakdown voltage is considerably lower. The current flow is depen-

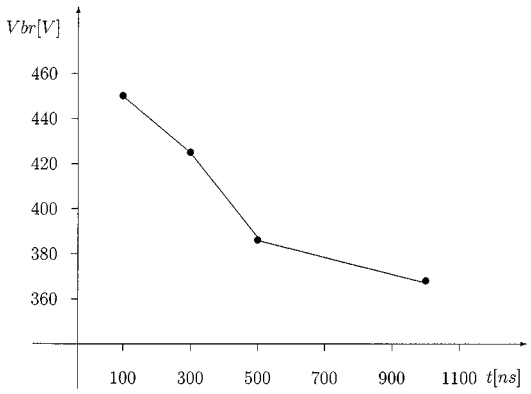

Fig. 4. Mean value of the breakdown voltage versus the TLM stress time.

dent on the W/L ratio, but also on the channel length itself, due to punch through effect, which will be discussed later on. It is also shown that the breakdown voltage depends on the stress time. As the stress time is increased, the breakdown voltage is decreased. These results suggest that electrical breakdown is also a thermal process. The heat generation is due to the current flow and it depends on the thermal properties of the materials used, amorphous silicon, Si_xN_y and glass. The time dependence suggests also that a high power dissipation develops (Wunch and Bell model [5]).

III. Device Simulations

A. Theoretical Introduction

The breakdown of amorphous silicon devices was earlier investigated in diodes [6], or in an antifuse structure [7], where an evidence was found of impact ionization in a-Si. In the thin film transistors itself a huge amount of work and research was focused on metastable effects in amorphous silicon, but very little was published on the subject on electrical breakdown. The items that have to be clarified about electrical breakdown in a-Si : H TFTs are the following.

- Is there punch-through?
- Is there impact ionization and avalanche breakdown?

Before the results of simulations regarding these questions will be shown, a few basic definitions will be introduced. Punch-through effect occurs when the neutral substrate width is reduced to zero at a sufficient drain voltage and the source depletion region is in direct contact with the drain depletion region. At this point, the source is effectively short circuited to the drain, and a large current can flow. What actually happens is that under high drain bias the channel depletion width is no longer constant along the length of the device, but varies from the source to the drain. This effect is called drain-induced barrier lowering (DIBL) effect and it occurs when higher drain voltage is applied to the device. It is very well known in MOS devices [8]. The surface potential (bend bending) along the channel between source and drain for long channel devices is normally constant. In short devices, or in long devices under very high drain biasing, it happens that the peak of the surface potential is reduced and is constant only over a small part of the channel, if at all. Since the peak surface potential is reduced, which means that the barrier is lowered, the current will increase.

Avalanche multiplication that may occur by means of impact ionization is very well explained in standard crystalline Si devices [9]. Electrons/holes gain so much energy in a high electric field that they can generate extra electron–hole pairs by exciting electrons from the valence band into the conduction band. In this way an avalanche of free carriers may arise. Could we expect an avalanche multiplication due to impact ionization in amorphous silicon?

B. Simulation Results

The electrical simulations of TFTs are performed by SILVACO [10] process and design simulation software.

1) Punch-Through: The effect of DIBL is shown through the simulations of:

- surface potential of an a-Si : H TFT under high drain bias;
- surface potential of a long- and a short-channel TFT under the same biasing conditions.

In Fig. 5 is shown how the surface potential is distributed along the channel for three different drain biases ($Vd = 1$, 2, 5 V). In all cases, the gate voltage was kept constant. It should be noted that the simulated TFT was scaled in lateral direction, which means that channel length and drain biasing are divided with a factor of ten. That does not influence the accuracy of the simulation results. This figure shows that increasing the drain bias, the barrier is decreased. It proves that the DIBL effect is present in a-Si : H TFT devices. It also helps us to understand the results obtained from the experiments. In the experiments the drain was stressed. Gate was grounded, so that the device was not active in the conductive mode. Initially, under very low drain voltage a low leakage current was flowing through the channel. As the drain voltage was increased, the DIBL effect was more and more pronounced. After the drain voltage exceeds a certain value, called threshold of degradation, the current flows through the device.

In another example, the same effect of barrier lowering can happen if the channel length is varied. Therefore, a TFT with two different channel lengths is simulated. The results of these simulations are presented in Fig. 6. The simulations show that with shortening of the channel, the barrier between source and drain is lowered. It also agrees with our experimental observations. Namely, it was noticed that both the threshold of degradation and the breakdown voltage depend on the channel length. The shorter TFTs degrade and fail earlier than the longer ones.

The previous simulation results proves the presence of the punch-through in a-Si : H TFTs. It shows that the punch-through occurs when drain voltage is high enough to suppress the barrier in surface potential between source and drain. It happens earlier in shorter devices for the reason that in the short channel devices, the barrier is already initially lowered.

2) Avalanche Multiplication: The question of the impact ionization and the avalanche breakdown is analyzed through the simulation of the recombination/generation rate under stepped-drain bias. The results of the simulations performed for a constant gate voltage ($Vg = 25$ V) and different drain biasing are shown in Fig. 7. Ionization rates of crystalline Si

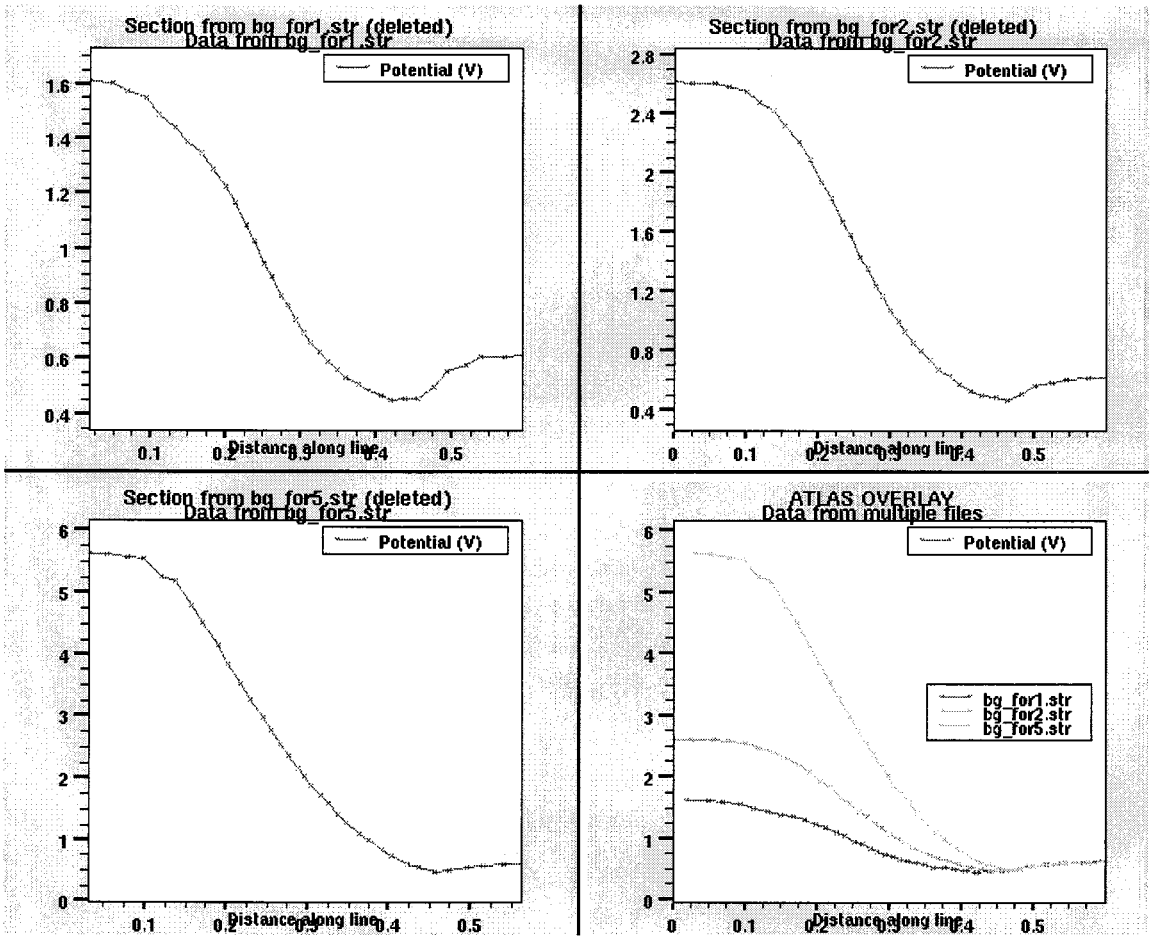

Fig. 5. Example of DIBL effect in amorphous silicon thin-film transistors simulated for various drain voltages ($Vd = 1, 2, 5$ V). x-axis represents the channel length [μm], $x = 0$ is the drain side, and $x = 0.6$ is the source side.

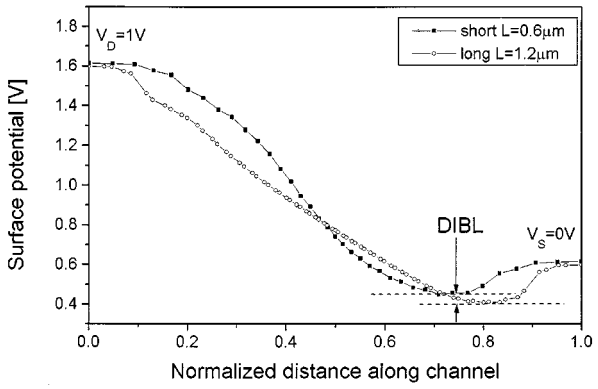

Fig. 6. Surface potential distribution along the channel obtained for TFTs with different channel lengths. x-axis represents the channel length [μm], $x = 0$ is the drain side, and $x = 0.6$ is the source side.

(c-Si) have been used since no other accurate data are available. a-Si will have lower binding energies at grain boundaries, so using c-Si data is a conservative estimate if conduction along grain boundaries is significant. Fig. 7 shows (please note that the drain voltage and the channel length are scaled by a factor of ten) that the peak generation rate is located at the drain, in the case when stress is applied to the drain. The generation peak value in the TFT with the channel length $L = 0.6$ μm changes from $G = 9 \cdot 10^{10}$ $(1/s$ cm$^3)$ for $Vd = 1$ V to $G = 1 \cdot 10^{21}$ $(1/s$ cm$^3)$ for $Vd = 10$ V and $G = 3 \cdot 10^{25}$ $1/s$ cm$^3)$ for $Vd = 20$ V. As the results are scaled by a factor of ten, it allows us to compare these results with the TFT with $L = 6$ μm and $Vd = 10$, 100, 200 V. The experimental shows that the breakdown in the TFT with $L = 6$ μm occurs at 280 V. In this case, one can expect an generation rate $G > 3 \cdot 10^{25}$ $(1/s$ cm$^3)$. This level of generation is able to start an avalanche breakdown. Simulation results prove that an avalanche breakdown is possible in amorphous silicon TFTs under ESD stress conditions.

IV. Thermal Analysis

A. Electrothermal Coupled Simulations

Thermal simulations in three-dimensional (3-D) in both static and transient regimes have been carried out. A simulator [11] has been used that translates a thermal model into an electrical equivalent, which in turn can be simulated using an electric circuit simulator. The simulations are performed in order to show the level of the temperature peak under ESD stress conditions and the location of the peak within the TFT. For the simulations, we use the simulation package LUMEX [11], which was developed at the University of Twente, Enschede, The Netherlands, and is used for coupled electrothermal simulations as a

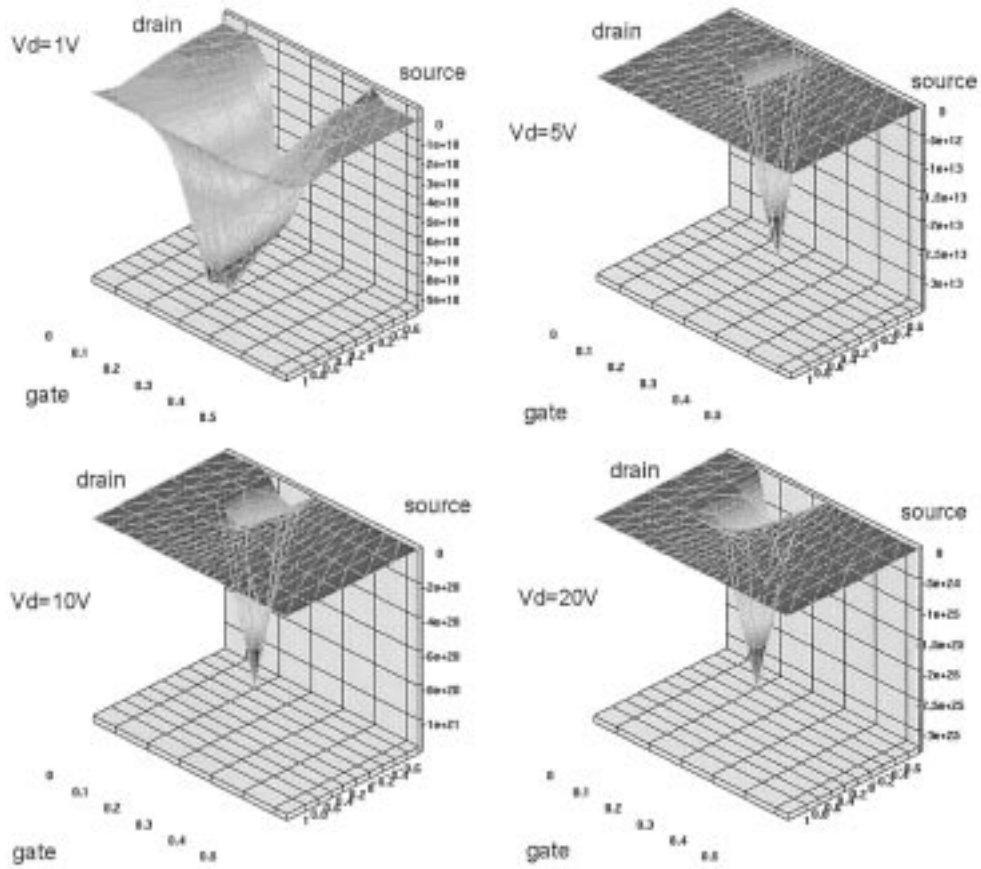

Fig. 7. Generation rate simulated under constant gate voltage ($Vg = 25$ V) and drain biasing $Vd = 1$, 5, 10, and 20 V. The entire thickness of a-Si is simulated (gate side on top).

preprocessor for the circuit simulator. For the circuit simulations, we use the package Pstar [12].

First, simulations of the TFTs with W, L variations are performed in order to show the temperature distribution over the TFT area in the short and long TFTs. The biasing conditions are: gate voltage $Vg = 60$ V and drain voltage $Vd = 100$ V. These biasing conditions are chosen to show the heat generation in the most severe case. The simulations were performed under assumption that the heat generation is equally distributed in all four lateral directions over the glass area. The area surrounding the devices was the same in all simulations. Only the channel length was varied, while the channel width was constant, as well as the drain and the source metal contacts widths. The simulated structure is designed according to the top-gate device built on a glass substrate and from the top side passivated over all device area, used in the experimental procedure. The temperature distribution shown in Fig. 8 is the temperature of the glass substrate in the first layer under the amorphous silicon layer. In Fig. 8, the channel length area has on the x-axis a finer grid than the surrounding substrate. The temperature distribution over TFTs shown in Fig. 8 is similar in all four cases. The simulations show that the temperature peak is located always at the drain side. Across the channel length, the temperature decreases from drain to source. In case of short devices the distribution is very much uniform across the channel length. For the channel length of $L = 4$ μm (Fig. 8), the simulation shows that the TFT is overheated. The simulated temperature is impossibly high ($\Delta T = 2400$ °C), so it implies that in the reality the TFT would be already broken down. Fig. 8 shows that in the TFT with $L = 6$ μm the temperature is relatively high ($\Delta T = 120$ °C). The device with $L = 10$ μm suffers much lower heating ($\Delta T = 28$ °C). Finally, the device with the length 100 μm is not heated ($\Delta T < 1$ °C). The simulations confirm that short channel devices suffer from more pronounced thermal heating due to the larger power dissipation. It is shown in the experiments that the breakdown voltage depends on the TLM pulse duration. The question is whether the change of breakdown with the change of the stress time is related to the thermal heating. Therefore, the 3-D electrothermal simulations were performed in transient regime. The stress conditions similar to the one in the experiment ($Vd = 350$ V, $Vg = 10$ V, $Vs = 0$ V, $W/L = 100$, and μm/20 μm) were simulated for variations of the pulse length. The results of the transient simulations are presented here by only one point chosen at the end of the stress pulse, when thermal heating is in its peak. The space coordinates of the location for which the results are shown are in the middle of the TFT width, at the drain side, which is chosen as it is shown to be the hottest point in the TFT. Fig. 9 shows the temperature rise for the stress pulses of different duration. It is shown that a certain time, which is in the order of an ESD pulse, is needed for establishing a temperature constant in time. After 100 μs the temperature rise in the hottest point becomes

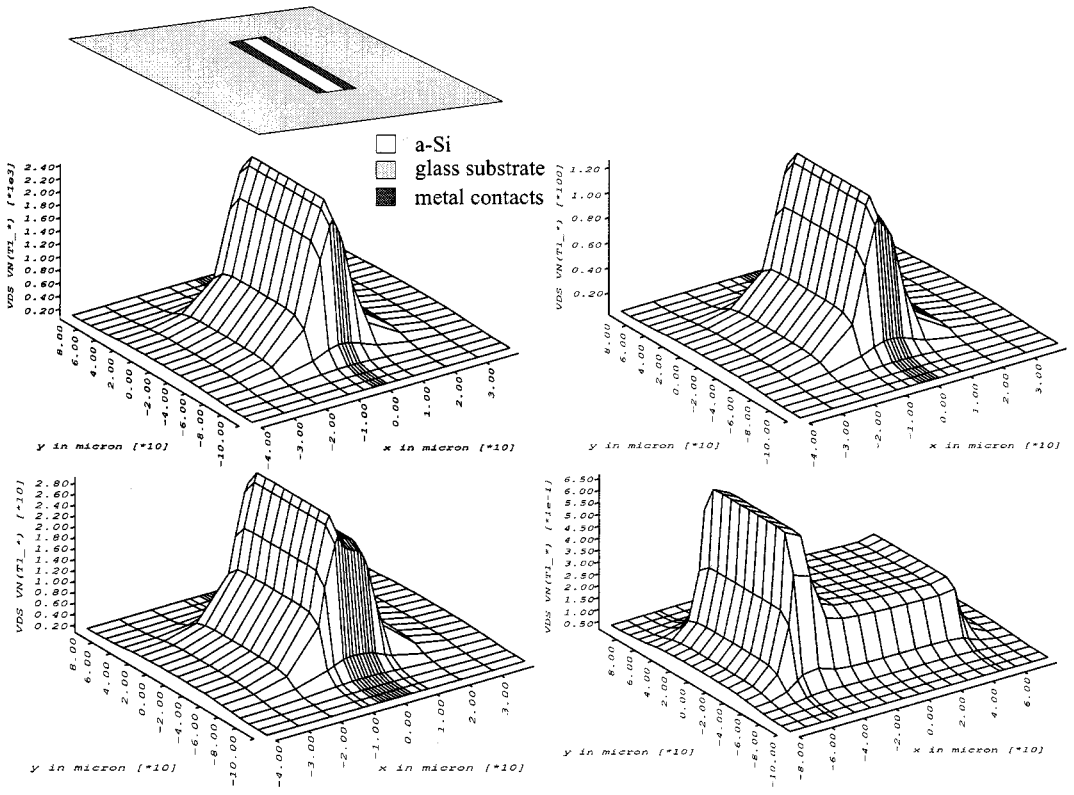

Fig. 8. Thermal simulations showing the temperature distribution in the TFTs with different channel lengths. The temperature profile is that of the a-Si layer. On the glass substrate, only the source and drain contacts are shown.

constant. It can be assumed that after the TFT enters thermal equilibrium and constant temperature is established, the breakdown voltage becomes constant.

B. Post-Breakdown Observation

Finally, postbreakdown observations have been carried out using optical microscopy and scanning electron microscopy (SEM). The observation confirms the location of the breakdown spot close to the drain in the case when the ESD stress is applied to the drain. The result is depicted in Fig. 10. Fig. 10 shows an example of breakdown in a TFT with $L = 6\ \mu$m, after etching of the top gate electrode. The size of the breakdown spot is large so that it covers almost the whole channel length. The center of the breakdown spot is located exactly on the drain/gate edge.

V. CONCLUSIONS

We have carried out an experimental and simulation study of the physics of electrical breakdown in amorphous silicon thin-film transistors. Electrical measurements, device simulations, electrothermal simulations and postbreakdown observations have been presented describing the breakdown event. It was found that the breakdown due to very short pulses (up to 1 μs) shows a clear dependence on the channel length. Electrical simulations have shown that a punch through effect is the cause of this channel-length dependence. It is also proven by means of electrical simulations that avalanche multiplication will happen near breakdown voltages. Three-dimensional electrothermal simulations are performed in static and transient regime confirming the location of the breakdown spot at the drain. The same conclusion is confirmed by means of electrical simulations and post-breakdown observations.

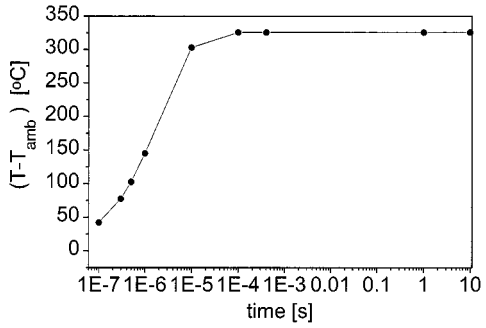

Fig. 9. Transient thermal simulations showing the temperature rise at the hottest point in the TFT under TLM stress of different pulse lengths.

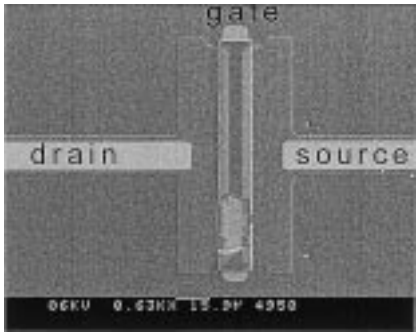

Fig. 10. SEM photograph showing the breakdown location in the TFT.

Thus, a consistent picture arises in which ultimate breakdown in TFTs at high drain voltage is caused by thermal overheating as a result of avalanche multiplication near the drain, where the punch-through effect creates a channel length dependence of the breakdown voltage.

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