Fabrication of thick silicon nitride blocks for integration of RF devices

L.J. Fernández, E. Berenschot, J. Sesé, R.J. Wiegerink, J. Flokstra, H.V. Jansen and M. Elwenspoek

A fabrication process for the creation of thick (tens of micrometres) silicon nitride blocks embedded in silicon wafers has been developed This new technology allows the use of silicon nitride as dielectric material for radio frequency (RF) circuits on standard CMOS-grade silicon wafers. Measurement results show that a performance similar to that of dedicated glass substrates can be reached.

Introduction: The enormous growth of wireless and portable applications has led to strong demands for high-performance monolithic low-cost passive components in RF and microwave integrated circuits (ICs). However, some traditional microwave passive components such as transmission lines and filters are difficult to integrate on the same chip with the RF and microwave circuits owing to the high substrate losses associated with standard low-resistivity CMOS-grade silicon substrates. As a result, most RF and microwave components are realised on special substrates such as AF45 glass [1, 2] or quartz [3]. Because of the need for monolithic integration with electronics, several techniques have been developed to allow the realisation of low-loss RF devices on standard silicon. These techniques include the use of dielectric layers such as polyimide [4] and benzocyclobutene [5], the use of polysilicon patterned ground shields [6], the use of silicon bulk-micromachining to remove the substrate locally under the RF components [7–9], and the use of surface-micromachined suspended metal structures at a distance of several tens of micrometres above the silicon surface [10, 11]. However, all these techniques impose restrictions on the device structures that can be realised or result in considerably higher losses than dedicated RF substrates. The best results are obtained with the freely suspended structures [7–11], but such free hanging structures are rather delicate, vulnerable to shocks and vibration, and difficult to package. Therefore, in this Letter we propose a new technique in which the silicon substrate is locally replaced by thick (tens of micrometres) blocks of silicon nitride, which has very good RF properties (tan $\delta = 5\text{–}9 \times 10^{-4}$). These silicon nitride blocks can be realised in a pre-CMOS process, i.e. before performing the regular CMOS process. The RF and microwave devices are realised on top of the silicon nitride islands by post-processing, i.e. after the CMOS process. Fig. 1 shows a schematic impression of a CMOS chip with integrated RF waveguide realised in this way. The only restriction is that the post-processing of the RF devices needs to be CMOS compatible, which is the case for most current surface micromachined devices. Low-stress, silicon-rich silicon nitride [12, 13] (SiRN) is chosen in order to minimise curvature of the silicon wafer due to residual tensile stress.

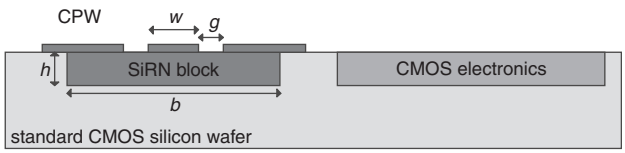

Fig. 1 *Cross-section of standard CMOS silicon wafer with silicon nitride block for monolithic integration of coplanar waveguide (CPW) and CMOS electronics*

Experimental results: Several test wafers have been processed with various thicknesses of the silicon nitride blocks. The effectiveness of the technique was evaluated by measuring the RF losses in coplanar waveguides (CPW) placed on top of the silicon nitride blocks. The CPW is one of the most commonly used RF circuits. It consists of three metal strips (see Fig. 1) on top of a dielectric material. The two electrodes at the sides are grounded, and the central one carries the RF signal. The impedance is determined by the width of the central line (w), the gap between the lines (g), the thickness of the dielectric (h), and the dielectric constant of the dielectric (ε_r). As shown below, silicon nitride blocks of 30 µm thickness result in performance levels very similar to dedicated substrates such as AF45 glass.

Silicon nitride layers are usually grown by low-pressure chemical vapour deposition (LPCVD). However, the maximum achievable layer thickness is in the order of 2 µm, which is too thin for use as intermediate layer between RF components and the silicon substrate. We developed a fabrication process based on refilling of deep trenches, which allows the creation of thick silicon nitride blocks in highly doped, standard silicon wafers. The process was successfully tested on two types of wafers: with ⟨100⟩ and ⟨110⟩ crystal orientation. Fig. 2 shows a summary of the fabrication process used for both types of wafers. The only difference is in the etching of silicon: in ⟨110⟩ wafers the silicon crystal orientation can be exploited to etch deep trenches by wet chemical etching, e.g. by TMAH or KOH; in standard ⟨100⟩ wafers this is not possible and deep reactive ion etching (DRIE) was used.

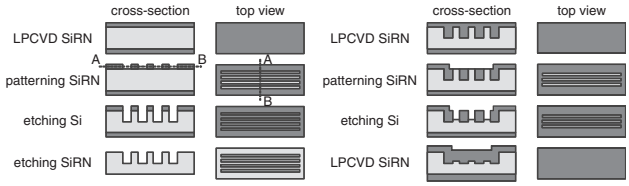

Fig. 2 *Fabrication process scheme for silicon nitride blocks embedded in standard silicon substrates*

The process starts with the deposition of a thin layer of silicon nitride (100 nm). This layer is patterned creating a large number of parallel rectangles. The length of the rectangles defines the length of the resulting silicon nitride block. The width and spacing between the rectangles are of the order of 2 µm. Next, deep trenches are created by anisotropic etching of the silicon substrate. The depth of these trenches defines the thickness of the resulting silicon nitride block. Then, the silicon nitride layer, which acted as a mask, is removed and a new silicon nitride layer is deposited. Because of the excellent conformal step coverage during LPCVD deposition, the trenches are completely filled by a deposition of 1 µm of silicon nitride. The silicon nitride is then patterned in order to gain access to the silicon located between the refilled trenches. This silicon is then removed by either DRIE or wet chemical etching. We used the latter option for our test samples because of its simplicity and its very high selectivity with respect to silicon nitride. Once the trenches are created, they are again filled by LPCVD SiRN, resulting in a thick silicon nitride block.

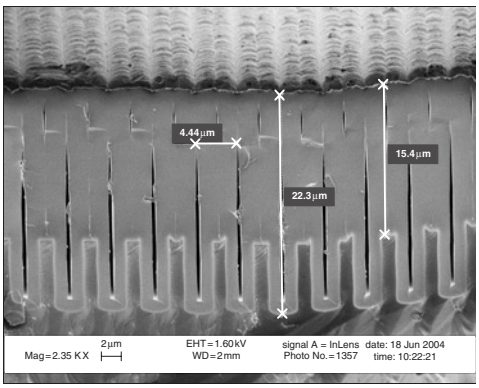

Fig. 3 *SEM picture of cross-section of silicon nitride block*

Fig. 3 shows a SEM picture of a cross-section of a 15 µm-thick silicon nitride block fabricated in a standard ⟨100⟩ silicon wafer. It clearly shows the voids that remain in the centre of the trenches after refilling. This is due to the fact that the trenches are the narrowest at the top as a result of the DRIE process. It is expected that these voids do not have any influence on the RF performance. A coplanar waveguide (CPW) was realised on top of the SiRN block by lift-off of a 1 µm-thick aluminium layer. The CPW has a length of 1 mm, which is 300 µm shorter than the SiRN block so that the end of the block will not affect the performance. To obtain 50 Ω characteristic impedance, CPW dimensions of $w = 90$ µm and $g = 30$ µm were used. Various sizes were used for the width, b, of the silicon nitride blocks, namely 50, 200 and 900 µm, in order to study the relation between losses and the amount of silicon nitride below the CPW.

The transmission losses (S_{12} parameter) of the CPW were measured against frequency up to 4 GHz. Fig. 4*a* shows the results for silicon

nitride blocks of 15 and 30 μm thickness together with the results for a CPW directly on silicon, on silicon with a 1.5 μm-thick SiRN layer and on low-loss AF45 glass. Clearly, the losses are the highest for the silicon substrate with −2.8 dB/mm. A small improvement is obtained using a 1.5 μm SiRN layer but the losses are still unacceptably high. A SiRN block of 15 μm thickness already gives an enormous improvement with −0.5 dB/mm losses at 4 GHz. A further improvement is reached with the block of 30 μm thickness. In that case we see that the performance is very close to that of dedicated AF45 glass substrates.

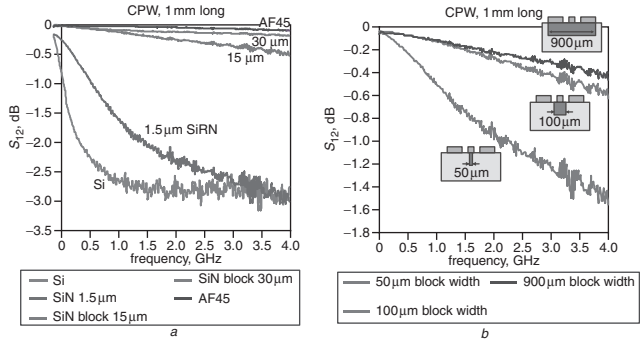

Fig. 4 *Measured losses (S_{12}) in dB, against frequency*

a Different substrates (bottom to top):
CMOS grade silicon
with 1.5 μm SiRN
with 15 μm-thick SiRN block
with 30 μm-thick SiRN block
dedicated AF45 glass substrate
b Three different widths of 15 μm-thick silicon nitride blocks

To study the improvement of the RF properties of a CPW in relation to the area where the silicon is replaced by silicon nitride, blocks 15 μm thick with three different widths (50, 100 and 900 μm) are compared. Fig. 4*b* shows the transmission losses for the three different configurations up to 4 GHz signal frequency. As expected, the losses decrease with increasing width of the silicon nitride block. A large improvement is already obtained with a SiRN block only 100 μm wide, which occupies part of the gap in the CPW ($w = 90$ μm and $g = 30$ μm) where most of the electric field is confined.

Conclusions: We have presented a novel fabrication process, which allows fabrication of thick blocks of low-stress silicon nitride in standard CMOS-grade silicon wafers. Measurements on coplanar waveguides have demonstrated the good RF properties of such blocks with transmission losses approaching those of dedicated RF and microwave substrates. Using the process as a pre-CMOS process allows the monolithic integration of high-performance RF and microwave devices with CMOS electronics.

Acknowledgment: This work is supported in part by the IST-2000-28261 EMMA programme of the European Commission.

20 October 2004
Electronics Letters online no: 20057499
doi: 10.1049/el:20057499

L.J. Fernández, E. Berenschot, J. Sesé, R.J. Wiegerink, J. Flokstra, H.V. Jansen and M. Elwenspoek (*MESA+, University of Twente, PO Box 217, 7500 AE Enschede, The Netherlands*)

References

1 Tilmans, H.A.C., *et al.*: 'MEMS for wireless communications: from RF-MEMS components to RF-MEMS-SiP', *J. Micromech. Microeng.*, 2003, **13**, pp. S139–S163
2 Fernandez, L.J., *et al.*: 'Radio frequency power sensor based on MEMS technology'. IEEE Sensors Conf., Toronto, Canada, October 2003
3 Rizk, J.B., and Rebeiz, G.M.: 'W-band CPW RF MEMS circuits on quartz substrates', *IEEE Trans. Microw. Theory Tech.*, 2003, **51**, (7), pp. 1857–1862
4 Ponchak, G.E., and Downey, A.N.: 'Characterization of thin film microstrip lines on polyimide', *IEEE Trans. Compon. Package Manuf. Technol. B*, 1998, **12**, pp. 171–176
5 Leung, L.L.W., *et al.*: 'Low-loss microwave filters on CMOS-grade standard silicon substrate with low-k BCB dielectric', *Microw. Opt. Technol. Lett.*, 2004, **40**, (1), pp. 9–11
6 Yue, C.P., and Wong, S.S.: 'On-chip spiral inductors with patterned ground shields for Si-based RF IC's', *IEEE J. Solid-State Circuits*, 1998, **33**, (5), pp. 743–752
7 Chang, J.Y.-C., *et al.*: 'Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier', *IEEE Electron Device Lett.*, 1993, **14**, pp. 246–248
8 Sun, Y., *et al.*: 'Micromachined RF passive components and their applications in MMICs', *Int. J. RF Microw. Comput. Aided Eng.*, 1999, **9**, pp. 310–325
9 Muller, A., *et al.*: 'Micromachined filters for 38 and 77 GHz supported on thin membranes', *J. Micromech. Microeng.*, 2001, **11**, (4), pp. 301–305
10 Yoon, J.-B., *et al.*: '3-D construction of monolithic passive components for RF and microwave ICs using thick-metal surface micromachining technology', *IEEE Trans. Microw. Theory Tech.*, 2003, **51**, (1), pp. 279–288
11 Dahlmann, G.W., *et al.*: 'High Q achieved in microwave inductors fabricated by parallel self-assembly'. Proc. Transducers '01, Munich, Germany, June 2001, pp. 1098–1101
12 Gardeniers, J.G.E., *et al.*: 'LPCVD silicon-rich silicon nitride films for applications in micromechanics, studied with statistical experimental design', *J. Vac. Sci. Technol. A*, 1996, **14**, (5), pp. 2879–2892
13 Sarajlic, E., *et al.*: 'Versatile trench isolation technology for the fabrication of microactuators', *Microelectron. Eng.*, 2003, **67–68**, pp. 430–437