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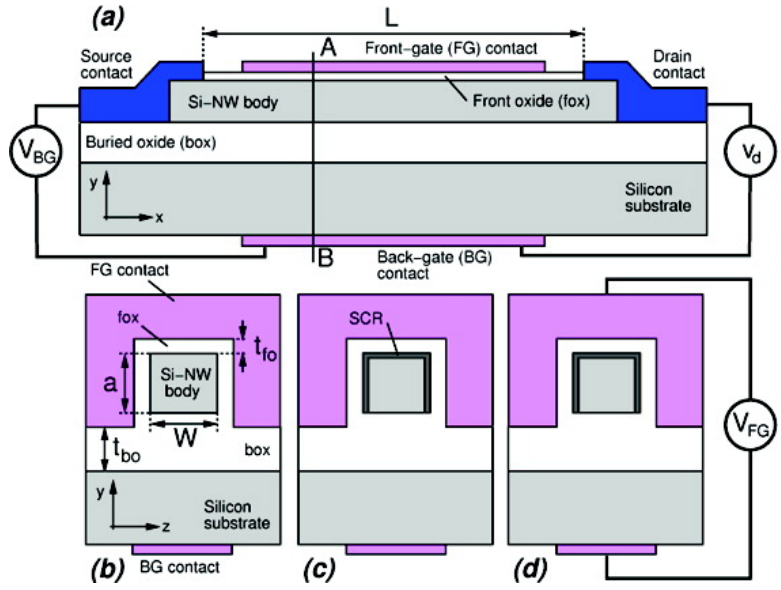

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Novel Top-Down Wafer-Scale Fabrication of Single Crystal Silicon Nanowires

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ABSTRACT

A new low-cost, top-down nanowire fabrication technology is presented not requiring nanolithography and suitable for any conventional microtechnology cleanroom facility. This novel wafer-scale process technology uses a combination of angled thin-film deposition and etching of a metal layer in a precisely defined cavity with a single micrometer-scale photolithography step. Electrically functional silicon and metallic nanowires with lengths up to several millimeters, lateral widths of ~100 nm, and thicknesses ~20 nm have been realized and tested. Device characterization includes a general description of device operation, electrochemical biasing, and sensitivity for sensor applications followed by electrical measurements showing linear *i*−*v* characteristics with specific contact resistivity $\rho_c \sim 4 \times 10^{-4}$ Ω cm^2 and electrochemical behavior of the oxidized silicon nanowires is described with the site-binding model.

Introduction. Over the past decade there has been a steady increase in reports of functional nanoscale (~10−100 nm) devices such as carbon nanotubes (CNTs)[1,2] and silicon nanowires (Si-NWs).[3,4] One- and two-dimensional structures, such as CNTs and nanowires (NWs), are technologically compelling due to their reported highly sensitive label-free detection of biomolecules in aqueous phase[5−12] and suitability for large-scale high-density integrated electronics.[4] Silicon NW devices are advantageous to CNT devices because of the well-established knowledge of silicon and silicon-related materials and mature planar microfabrication technologies.

Two broad micro/nanofabrication classifications have been previously defined: "bottom-up" and "top-down." The bottom-up approach assembles molecules and small solid structures from atoms, which are combined to into a large variety of shapes and functions. A large number of materials, such as Si, Ge, ZnO, and many others, have been successfully synthesized into nanostructures over the past decade.[13,14] Vapor−liquid−solid material growth is a commonly used bottom-up method for generating single-crystal nanostructures in large quantities.[15] Precursor gas mixtures containing dopants, such as boron and phosphorus, have resulted in in situ doped p-type or n-type Si-NWs, respectively.[16] Although bottom-up synthesized semiconductor NW devices are reported to have excellent electronic transport properties, the current manufacturing method does not provide controlled growth into high-density ordered arrays and typically requires transfer and assembly of devices on separate substrates, and reproducibly forming high-quality electrical contacts has been challenging.

Top-down fabrication technology, the standard technique for semiconductor manufacturing, has been used to realize NWs from Si,[7−9,11,12] Au and Ag,[17] as well as many other materials. Top-down fabrication is based on microfabrication processes, which consist mainly of deposition, etching, and ion-beam milling on planar substrates. Patterning is typically done using UV- and DUV-photolithography and commonly combined with advanced nanolithography techniques such as electron beam lithography (EBL) or focused-ion-beam (FIB) to realize feature sizes down to a few nanometers.[18,19] Although EBL and FIB techniques are valuable methods for a research environment, they are not currently amenable to large-scale manufacturing. Replication top-down fabrication techniques, such as nanoimprint lithography (NIL),[20] are capable of combining the resolution of EBL with large area pattern formation, and high-density Si-NW arrays have been reported using a specialized pattern transfer technique.[21] Nanoimprint methods are promising; however, significant development is required for general application to wafer-scale nanopatterning. Other Si-NW fabrication techniques, such as nanostencils,[22,23] size reduction,[24] and spacer edge lithography[25] are simple and low cost; however, lateral dimensions are difficult to control.

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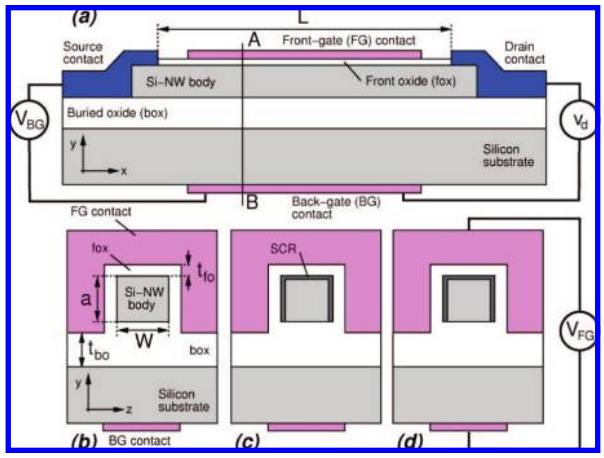

Figure 1. SOI Si-NW device cross sections (a) length $x-y$ view with device length L. (b) A−B cross section in $y-z$ view with device height a, width W, front oxide thickness t_{fo}, and buried oxide thickness t_{bo}. (c) Front-gate biasing space-charge region (SCR). (d) Front-gate biasing.

Although there has been significant progress in manufacturing functional Si-NWs, using both bottom-up and top-down approaches, the current methods can be improved and simplified using a combination of conventional microfabrication and new nanofabrication techniques. In this paper, we present a novel and simple fabrication technology, called deposition and etching under angles (DEA), which is based on standard microfabrication processes, such as contact photolithography, thin film deposition, and wafer-scale ion beam etching, to realize metallic nanowires with widths down to ~20 nm and lengths up to several millimeters. The key to providing improved dimensional control compared to other methods is a precisely defined cavity that permits controlled removal of part of the metal layer with an angled wafer-level ion beam that resembles a nanostencil structure patterned directly on the wafer surface, which minimizes lateral spread of the deposited metal. The metallic NWs are then used as a hard mask to transfer the pattern to the top silicon layer of a silicon-on-insulator (SOI) wafer by dry etching to realize wafer-scale Si-NWs, with lateral dimensions below 100 nm.[26] Additionally, we present a theoretical description of Si-NW device behavior and particularly highlight the importance of using a *reference electrode* to provide a well-defined surface potential at the Si-NW/solution interface. Finally, the electrical and electrochemical characterizations of the Si-NW devices are discussed.

Device Structure, Physics, and Electrical Biasing. In this section, the Si-NW device operation and sensitivity are described, and the importance of establishing a well-defined Si-NW surface potential for sensing applications is discussed. The top-down fabricated Si-NW device cross sections are shown in Figure 1. The thin Si-NW body is electrically isolated from the silicon substrate by a buried oxide (box) layer, and the front-gate (FG) and back-gate (BG) contacts are used to control the conductivity of the Si-NW with the front oxide (fox) and/or box layers, respectively. This type of device structure is commonly referred to as an asymmetric multigate field-effect transistor.[27] The upper three sides of the device have approximately the same oxide thickness and

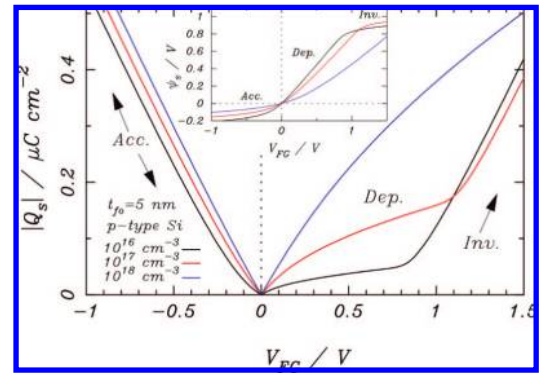

Figure 2. Total silicon charge $|Q_s|$ as a function of V_{FG} in the accumulation (Acc.), depletion (Dep.), and inversion (Inv.) regions with varying doping concentrations. Inset: surface potential ψ_s as a function of V_{FG}.

are said to be symmetric with respect to the FG. Since the BG box layer is typically much thicker (>10×) than the fox layer, then BG biasing is much larger compared to the FG to produce a similar field-effect and is said to be asymmetric to the FG.

The silicon field-effect devices have three distinct operation regimes where the accumulation, depletion, and inversion space charge regions are created in the semiconductor layer by controlling the potential ψ_s of the silicon surface. In the depletion regime, bound ionized impurity charge Q_d dominates, while in the accumulation and inversion regimes free charge (Q_a and Q_i, respectively) at the surface dominates. Since the Si-NWs are gate voltage controlled devices, it is useful to consider first the ideal voltage-controlled charge modulation behavior of the metal−oxide−semiconductor (MOS) system. The electrolyte−oxide−semiconductor (EOS) system will be described in the electrochemical characterization section.

Figure 2 shows the total silicon charge $|Q_s|$ of a single MOS surface, as V_{FG} is varied from small negative to small positive voltages, where an exact solution of Poisson's equation[28] is plotted for three different doping concentrations. The inset shows ψ_s as a function of V_{FG}, where ψ_s varies rapidly with V_{FG}, in the depletion region. However, a large V_{FG} is required to produce a small change in ψ_s, in the accumulation and inversion regions, which is important for device sensitivity. For negative V_{FG}, majority carrier accumulation occurs and increases sharply with V_{FG}, more or less independent of the impurity doping concentration. For small positive V_{FG}, the silicon body is partially depleted and strongly dependent on the silicon body doping. For larger V_{FG}, an inversion charge layer is formed and is strongly dependent on the body doping concentration and silicon body thickness.[29] In all three regions the device current−voltage and sensitivity characteristics are very different.

In this simplified description, effects of fixed-oxide and silicon/oxide interface trapped charges have been neglected and $V_{FG} = 0$ is defined as the flat-band potential where $\psi_s = 0$. Additionally, it should be noted that in the previous description, any depletion or accumulation region at the back-oxide Si-NW interface due to the back-gate contact has been neglected for partially depleted operation, which can be

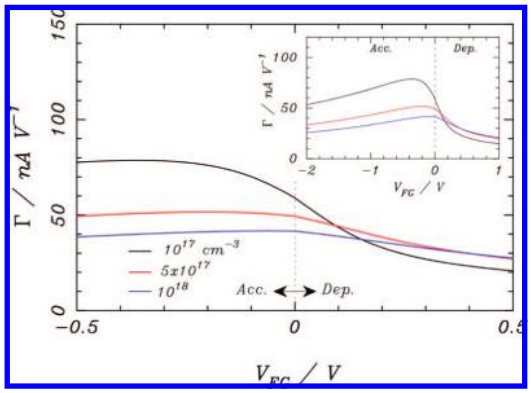

Figure 3. Sensitivity curves with $W = 50$ nm, $L = 5$ μm, and $t_{fo} = 5$ nm as a function of V_{FG} and doping concentration. Inset: sensitivity curves in accumulation and depletion operating regimes.

important for low channel doping levels and gate potentials near the threshold voltage.[32] Unless stated otherwise, it is assumed that the substrate back-gate contact is connected to the source contact and set to zero ($V_{BG} = 0$). For sensing applications, where the front-oxide layer is exposed directly to solution, the flat-band voltage is different and will be described below. There are many reports of devices operated with different biasing configurations, including negative V_{BG},[33,34] $V_{BG} = 0$,[5,9,10,12,35] and positive V_{BG}.[37,38] For devices with $V_{BG} = 0$, the device operating regime is not clear, because the surface potential is not well defined, and as shown in the inset of Figure 2, small surface potentials can produce large effects in low doped layers.

The low-frequency device sensitivity Γ can be estimated as $\Gamma \equiv |g_m|$, where $g_m = \partial i_d/\partial V_{FG}|_{vd} \approx \mu v_d C_p W/L$[39] is the small signal transconductance, μ is the carrier mobility, v_d is the drain to source voltage (Figure 1a), C_p is the equivalent capacitance calculated from Q_s,[40] and W/L is the width to length ratio. The sensitivity Γ scales proportionally with μ, v_d, and W, and inversely proportional to the length L. Calculated curves of Γ as a function of V_{FG} for a silicon surface with varying doping concentrations are shown in Figure 3. The mobility dependence on applied V_{FG} in the accumulation and inversion regions[41,42] and the bulk mobility reduction with increased doping concentration[43] have been considered in the calculation. However, carrier mobility may vary greatly, depending on the wafer manufacturing method and interface charges.

For small V_{FG}, the lowest doping concentration results in the largest Γ; however, it becomes the lowest for larger positive V_{FG} as the depletion depth increases. The sensitivity in the inversion region is not considered in this description due to transient effects that occur under certain conditions for homogeneously doped structures.[39] Low boron doping concentrations have been reported to result in higher sensitivity measurements.[9] Considering small front-gate voltages only, relevant for most sensing applications, Γ is indeed larger for lower doping concentrations. Since Γ increases further for small negative V_{FG} (p-type silicon), the increased sensitivity for lower impurity doping results from operation in the regions between depletion and accumulation. This highlights an important point that careful control of the surface potential in solution with a reference electrode is required to bias the device in the regime with highest sensitivity and well-defined surface potential, which has been largely neglected in the Si-NW literature. In fact, it was shown more than 30 years ago that solution biasing is required for field-effect device gating.[44]

The above model does not describe sensitivity changes as the NW cross-sectional area is reduced, which is beyond the scope of this article, but rather the effect of body doping and the importance of defining the surface potential. Although scaling to smaller dimensions is predicted to further improve sensitivity due to electrostatic gating of the depletion region in two dimensions,[35] the 1/*f* noise of Si-NWs has been shown to increase as the NW cross-sectional area decreases,[45] which may ultimately limit the Si-NW size for (low-frequency) sensing applications. The device sensitivity is dependent on other parameters, such as interface charge[46] and the proximity of the charged moiety to be detected to the surface and ionic strength of the buffer, which affects the Debye length at the sensing surface, and at the molecular level, and charge screening.[47,48]

A few observations emerge from this description. First, front-gate biasing in the accumulation and inversion regions should result in higher sensitivity compared to back-gate biasing. Second, for homogeneously doped structures operation in the inversion region can lead to transient effects due to a lack of minority carriers. Finally, the depletion-mode devices have the advantage of not requiring an additional voltage to induce inversion or accumulation and device sensitivity will increase with increased surface-to-volume ratio of the Si-NW body. However, the moderate to high doping levels required for depletion-mode devices can be difficult to maintain in nanoscale devices and require careful management of thermal processing steps. Therefore, simple and flexible fabrication methods are needed with well-controlled processes for impurity doping and oxidation.

Microfabrication. One of the important advantages of top-down Si-NW fabrication is that critical device attributes, such as impurity doping and electrical contacts, are well developed and can be precisely controlled. Another advantage of the top-down Si-NW fabrication is the commercial availability of high-quality SOI substrates. The important fabrication process steps of the DEA technique[26] are shown schematically in Figure 4. The Si-NWs presented in this article are manufactured from SOI wafers (SOITEC, France) with a 70 nm thick device layer Si(100) and 140 nm box layer. The first step of the process is to reduce the thickness of the device layer silicon to 40 nm using a thermal oxidation-wet etching thinning process. The remaining silicon device layer is then uniformly doped by ion implantation (energy, 30 kV; ion, BF_2^+; dose, 10^{14} cm^{-2}; angle, 7°) and subsequently annealed to form the uniform p-type silicon layer (950 °C, 100% N_2) with a target doping concentration of $\sim 5 \times 10^{18}$ cm^{-3}, which is sufficient to form an Ohmic electrical contact at the metal−silicon interface.[49] Although the presented devices are depletion-mode devices, the microfabrication process is very flexible and any general device configuration

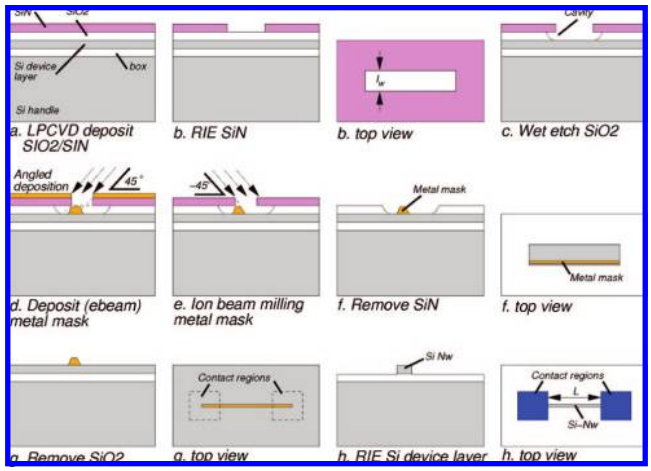

Figure 4. Single-mask silicon nanowire DEA fabrication process.

can be realized. A 20 nm thick thermal oxide (SiO_2) is reactively grown with wet-oxidation (950 °C) on the silicon device layer. Next, a 20 nm layer of stoichiometric silicon nitride (Si_3N_4) is deposited in a low-pressure chemical vapor deposition (LPCVD: 200 mTorr, 800 °C, 22 sccm SiH_2Cl_2, 66 sccm NH_3) reactor directly on the SiO_2 surface (Figure 4a).

A photolithographically (EVG 620, Electronic Visions Group) defined window $l_w \sim 3$ μm (Figure 4b), is etched (20 mTorr, 150 W, 20 sccm CHF_3, 5 sccm O_2) using reactive ion etching (RIE) in the Si_3N_4 layer (Figure 4b). The width l_w can be scaled down to submicrometer dimensions with refined lithography conditions. The exposed SiO_2 layer is wet etched in dilute hydrofluoric acid (5%) to form the undercut region between the Si_3N_4 and silicon layers (Figure 4c), which is the precisely formed cavity. A thin metal (Cr) layer is then electron-beam evaporated at a 45° angle, with respect to the substrate (Figure 4d). Ion beam milling (Ar, 10 kV) is subsequently done at −45° to remove a portion of the metal layer in the cavity, which results in a hard-etch metal mask layer (Figure 4, panels e and f). The remaining Si_3N_4 and SiO_2 layers are removed using a combination of RIE and wet etching, shown in Figure 4, panels f and g. Figure 5 shows a scanning electron micrograph (SEM) of a ~33 nm wide metal hard mask. The quality of the Si-NW surfaces can be improved by optimizing the ion-beam milling angle and deposition of the metal mask layer such that the metal layer is located mostly in the cavity and then a larger milling angle will produce a well-defined edge and reduce the surface roughness.

A second lithography step is then used to mask contact regions at the ends of the Si-NWs. The Si-NW structures are finally formed using RIE (100 mTorr, 200 W, 20 sccm SF_6, 5 sccm O_2). The metal hard mask layer is removed in a wet etchant (CR-14, Transene Co., Inc.), as shown in Figure 4h. The exposed silicon surfaces have been oxidized to form a thin (~5−10 nm) SiO_2 electrical isolation layer using conventional dry oxidation (950 °C, 5 min). The oxide isolation layer is removed at the electrical contact regions in a dilute hydrofluoric acid etch (5%) and a Ni/Pt (20 nm/180 nm) layer is deposited and subsequently annealed (450 °C, 20 min.) to form a NiSi silicide at the Ni−Si interface.

An atomic force microscopy image (Digital Instruments, Dimension 3000) of a fabricated Si-NW device with $t \approx 30$ nm and $W \approx 180$ nm is shown in Figure 5c. During the final process steps, a small amount (~5−10 nm) of the box layer is removed. In this article, functional Si-NW devices with widths down to ~100 nm in moderately dense device arrays (spacing down to ~500 nm), tunable Si-NW body conductance, and Ohmic contacts have been realized with the DEA technique.[50] Finally, a thin (~1 μm) parylene layer was vapor deposited and patterned (O_2 plasma with photoresist mask) to electrically isolate the metal contact regions from the electrolyte samples for electrochemical characterization. The devices are wire bonded and attached to a circuit board and all external connections encapsulated with a thick epoxy layer (Hysol, Henkel AG and Co.). Figure 5 shows various images of fabricated Si-NW devices and device arrays.

Electrical Measurements. The depletion-mode Si-NW devices presented in this article are homogeneously and uniformly doped p-type. The electrical characteristics of the fabricated Si-NW devices have been measured to quantify the following: (i) doping concentration N_a and resistivity ρ_s of the silicon body layer, (ii) electrical contact behavior with a two-contact device, and (iii) contact resistance R_c using a modified transfer length method (TLM).[51] The measurement of carrier mobility is also extremely important for accurate device modeling but is beyond the scope of this article. Many techniques are available for extracting carrier mobility and are summarized in ref 51.

A conventional four-point probe structure was used to measure the resistivity ρ_s, which is used to eliminate the effect of R_c in the measurement. For 50 μm long Si-NWs, the average measured resistivity is $\rho_s = (2.84 \pm 0.58) \times 10^{-2}$ Ω cm (10 samples), which translates into $N_a \approx 2 \times 10^{18}$ cm^{-3}, with device cross-sectional area $A_c \approx 8.0 \times 10^{-15}$ m^2 estimated from AFM imaging.[52] The reduced doping concentration compared to the target doping concentration of 5×10^{18} cm^{-3} was due to boron segregation from the thin silicon layer (segregation coefficient less than unity), which demonstrates the importance of careful device design, fabrication, and characterization.

The electrical behavior of the silicon devices can be evaluated by considering a simple lumped-resistance model of the Si-NW devices for dc and low frequency operation as $R_T \approx 2R_c + R_s$, where R_T is the total impedance across the Si-NW device and R_s is the series resistance of the undepleted silicon layer. The electrical contacts are a critical aspect in the design, fabrication and sensitivity of Si-NW based devices. Forming electrical contacts on submicrometer scale devices is well-established and described extensively in the literature for more than 3 decades.[53] The ideal electrical behavior of Ohmic contacts is characterized by linearity and low voltage drop across the interface.[49] Figure 6 shows measured $i-v$ characteristics and symmetric zero-crossing behavior. Histograms show ~20% variation around the mean

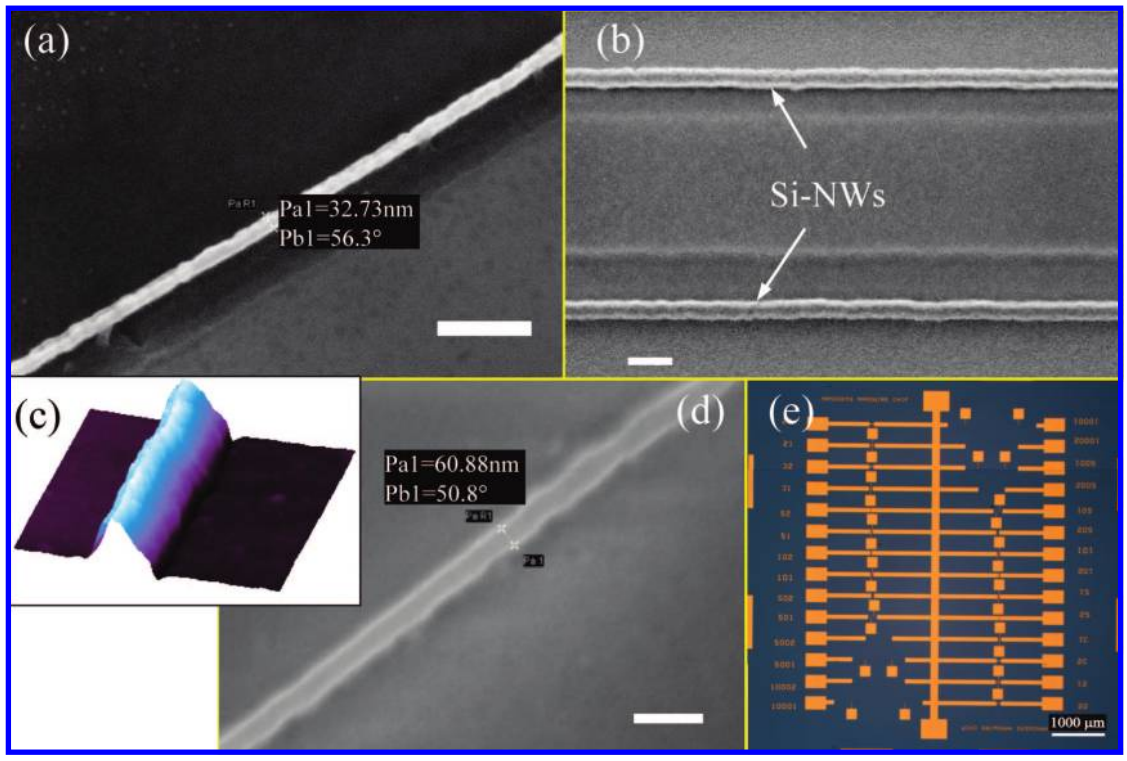

Figure 5. Fabricated device images: (a) SEM image of metal hard mask prior to silicon device layer etching with lateral width ~33 nm (scale bar: 200 nm); (b) SEM of parallel Si-NWs (scale bar: 200 nm); (c) AFM image of a typical Si-NW (*x*,*y* length: 1 μm; vertical height 50 nm); (d) SEM of single Si-NW (scale bar: 200 nm); (e) 7 mm × 7 mm test chip showing electrical contact pads interconnecting 28 Si-NW pairs.

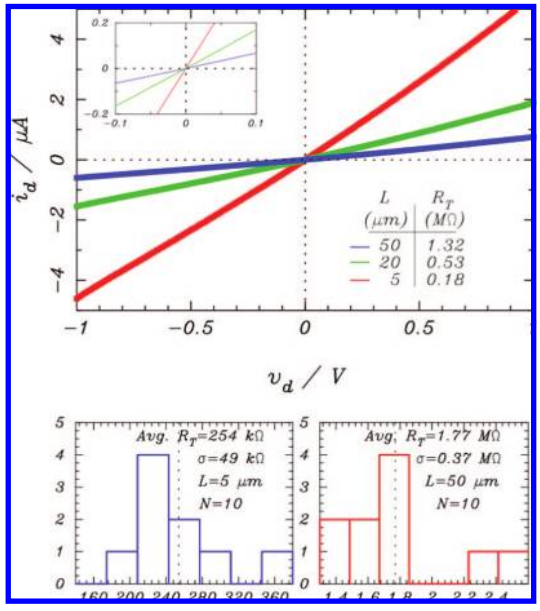

Figure 6. Measured $i-v$ curves (two-point measurement) of Si-NW devices with varying lengths: upper inset, zero-crossing point; lower, total resistance histograms for $L = 5$ and 50 μm.

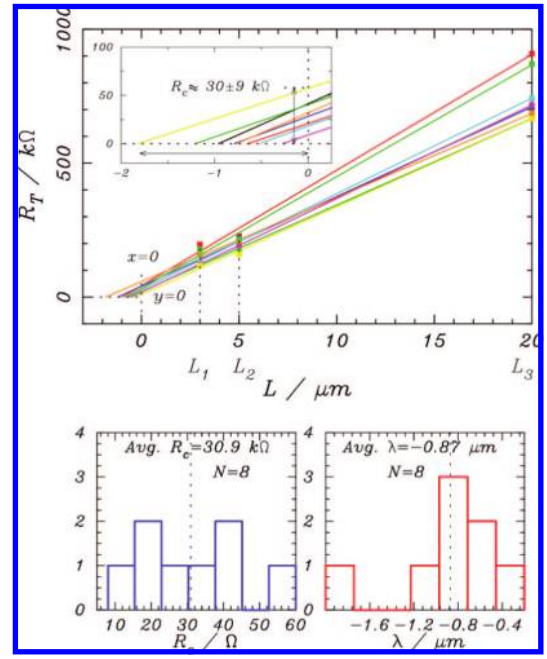

Figure 7. TLM analysis results: upper inset, $x = 0$ crossing (vertical arrow) and $y = 0$ crossing (horizontal arrow); lower, measured contact resistance (left) and penetration length λ (right) histograms.

resistance. The slope of the $i-v$ measurements is $R_T \approx \Delta v_d/\Delta i_d$.

Figure 7 shows TLM measurements of Si-NWs devices with lengths $L_1 = 3$, $L_2 = 5$, and $L_3 = 20$ μm. The contact resistance was determined by extrapolating to the $x = 0$ crossing of R_T-L_i plot. The $y = 0$ crossing indicates the contact penetration depth λ, an important parameter to estimate contact efficiency.[51] The measured data show $R_c = 30 \pm 9$ kΩ (average specific contact resistivity $\rho_c = 4 \times 10^{-4}$ Ω cm^2) with large variation of contact resistance from device to device. Since λ is smaller than the contact length, then interface area λW has been used to calculate the specific

contact resistivity. The slope of the R_T-L data indicates a resistivity $\rho_s = 2.86 \pm 0.36 \times 10^{-2}\ \Omega$ cm, which is consistent with the four-point measurements, discussed earlier.

Further refinements are required to reduce the contact resistivity to the $10^{-5}-10^{-6}\ \Omega\ \text{cm}^2$ range, commonly achieved in the semiconductor industry.[54] For a Si-NW with length $L = 50\ \mu$m, the obtained contact resistance represents about 2% of the total Si-NW resistance.

The formation of *good* electrical contacts to silicon using planar fabrication technology requires consideration of the Schottky barrier and surface contamination. A practical solution to reduce the potential barrier height of the metal−silicon is to properly choose a metal layer with a low work function difference and doping of the region under the contact, such that carrier transport across the metal−semiconductor interface is dominated by quantum-mechanical tunneling and the barrier width is as narrow as possible. Surface contamination, such as residual oxide or polymer layers, is an important issue and can be minimized with large contacting areas and proper cleaning procedures.[54]

Electrochemical Characterization. Since the Si-NW sensors are similar to ion-sensitive field effect transistor (ISFET) sensors,[55] the electrochemical behavior can be described directly with techniques and methods developed over the past few decades to understand electrochemical behavior of field-effect devices.[56−58] Gating the depletion-mode devices is similar to a junction field effect transistor,[59,60] with the exception that the depletion layer width is modulated with the field effect at the FG and/or at the buried oxide region with the BG. For a p-type layer with $W \gg a$, the conductance parallel to the layer (x-direction) is $\sigma = \zeta(a - f_d)\mu$, where ζ is the charge density and f_d is the depletion function.[61] An applied field at the silicon surface changes the charge by ΔQ_d, resulting in a conductance layer change $\Delta\sigma/\sigma = \Delta Q_d/\zeta/(a - f_d)$, which was described more than 60 years ago.[62] For an ideal rectangular cross section and small v_d (Figure 1a), the current can be approximated using the gradual-channel approximation[59,63] as $i_d \approx \mu q N_a v_d (a - f_d) W/L$, where the silicon layer is assumed partially depleted and the front-gate and back-gate voltages are uncoupled. The sensitivity is $\Gamma \equiv |g_m| = \partial i_d/\partial V_{FG}|_{vd} \approx \mu q N_a v_d (\partial f_d/\partial V_{FG}) W/L$. For $W \sim a$ the depletion current is $i_d \approx \mu q N_a v_d (a - f_d)(W - 2f_d)/L$, and corresponding sensitivity is $\Gamma \approx \mu q N_a v_d (aW - 2f_d)(\partial f_d/\partial V_{FG})/L$. This simple model does provide insight into device behavior; however, more sophisticated models are required for precise prediction of device performance.

The front-gate of the MOS structure is replaced with an electrolyte solution and reference electrode forming the EOS structure, shown in Figure 8, where the reference electrode electrically biases the solution and has an internal potential drop E_{ref}, which results in a new flatband voltage expression $V_{FB} = E_{ref} - \phi^{Si}/q - \psi_o - Q_{tfo}/C_{fo} + \chi^{sol}$, where E_{ref} is the reference electrode potential, ϕ^{Si}/q is the silicon work function and χ^{sol} is the dipole potential of the solution.[64]

The current i_d was measured directly with a lock-in amplifier. All experiments were conducted with a universal buffer mixture consisting of phosphoric acid, acetic acid, and boric acid. The device sensitivity is shown in Figure 9 with measured device responses from front-gating in solution and the corresponding measured i_d in the inset. The measured Γ shows the same general behavior as shown in the Figure 2. For $L = 50\ \mu$m and $W = 150$ nm, the estimated sensitivity is $\Gamma \sim 12$ pA mV^{-1}, compared to the measured value of 16 pA mV^{-1} at $V_{FG} = 0$ V, due to differences in carrier mobilities in the depletion and accumulation regions and will be published elsewhere.

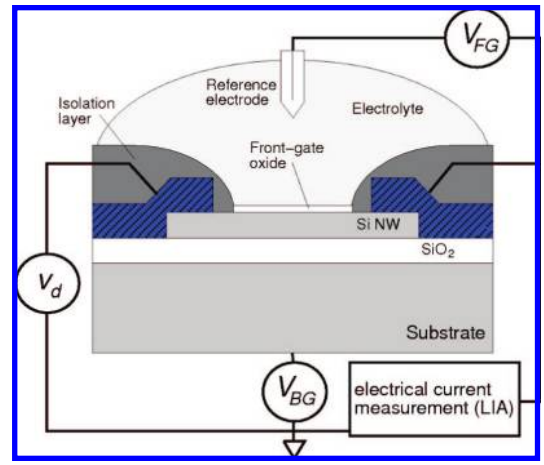

Figure 8. Si-NW device configuration in solution with Ag/AgCl reference electrode (Radiometer Analytical) and lock-in amplifier (SR830, Stanford Research Systems). All measurements performed with $v_d = 50$ mV and 37 Hz modulation frequency and $V_{BG} = 0$.

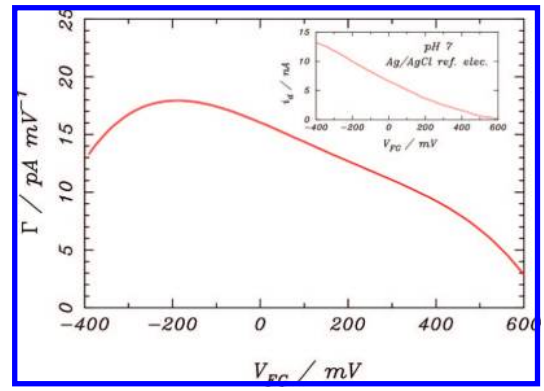

Figure 9. Calculated Γ from the measured i_d as a function of V_{FG}. Inset: Conductivity modulation of a single Si-NW with applied V_{FG}.

The behavior of the Si-NW devices with SiO_2 surfaces has been analyzed with techniques developed for ISFETs.[56−58] The charging of a surface in a liquid has been previously described in detail.[65] A partially depleted Si-NW device with the substrate and one device contact grounded ($v_s = V_{BG} = 0$) can be approximated with the physical electrochemical representation as **M/Si-NW | front-oxide | electrolyte | reference electrode | M′**, where M is the metal electrode and M′ is the contact to the reference electrode. For fully depleted Si-NWs, the full substrate structure, including the buried oxide and substrate layers, must be included in the electrochemical model.

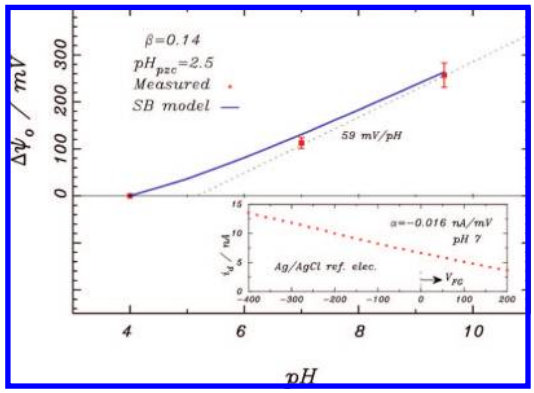

Figure 10. Measured and calculated (SB model) pH behavior of oxidized Si-NWs. Error bars ±10%. The black dotted line shows the ideal Nernst behavior. Lower inset: calibration curve.

The surface potential ψ_o of the electrolyte−oxide interface is dependent on the pH of the electrolyte solution due to the interaction of the insulator surface with ions in solution. For oxides, the surfaces are commonly considered amphoteric and can act as a proton donor or acceptor. In the case of SiO_2, three types of surface sites are available, Si−OH, Si−O^-, and Si-OH_2^+, which have been considered in the site-binding (SB) model[65] and used extensively to describe ISFET behavior. The general SB expression is 2.3-(pH_{pzc} − pH) = $\psi_o/kT + \sinh^{-1}(\psi_o/\beta kT)$, where pH_{pzc} is the solution pH where $\psi_o \approx 0$ and β is a dimensionless sensitivity parameter $\beta = q^2N_s\delta/C_{eq}kT$, where N_s is the total number of surface sites, δ is a measures the reactivity of the surface, and C_{eq} is the equivalent capacitance of the electric double layer.

Tests at pH 4, 7, and 10 were performed and results compared to the SB model (Figure 10). The devices were placed in pH 7 buffer and surfaces allowed to equilibrate for a period of about 2 h. The Si-NW current was recorded, and then a calibration curve was recorded by measuring i_d as a function V_{FG}, the gate voltage applied to the reference electrode. The lower inset in Figure 10 shows an i_d-V_{FG} calibration curve. The calculated i_d−pH response curve is calculated from the SB model and compared to the measured values by using the NW current at pH 7 as a reference. The measured data fit the SB model reasonably well with $\beta \approx 0.14$ and $pH_{pzc} = 2.5$, which matches well for published reports of SiO_2 surfaces[56]

Conclusion. Although significant advancements have been made in realizing functional Si-NWs over the past decade, using both bottom-up and top-down approaches, the existing approaches can be improved and simplified by using conventional microfabrication methods. We present a novel, low cost, and simple fabrication technology, called deposition and etching under angles, DEA, which is based on standard microfabrication processes, i.e., contact photolithography, thin-film deposition, and wafer-scale ion beam etching, to realize metallic nanowire etch templates in cavities with lengths up to several millimeters and widths down to 20 nm. The nanostencil structure patterned directly on the wafer surface provides improved dimensional control compared to other methods with the use of a precisely defined cavity that permits controlled removal of part of the metal layer with an angled wafer-level ion beam. Functional Si-NW devices with widths down to 100 nm in moderately dense device arrays have been realized, and electrical and electrochemical device characterizations of fabricated Si-NWs have been presented. Electrical measurements show linear $i-v$ characteristics and specific contact resistivity $\rho_c \sim 4 \times 10^{-4}\ \Omega\ cm^2$, which demonstrates that this simple, low-cost fabrication technique is capable of producing high-quality Si-NW sensors. Electrochemical measurements following methods developed for the ISFET sensors demonstrate that the oxidized Si-NWs can be described with the SB model. Additionally, we present a description of Si-NW device behavior and sensitivity and highlight the importance of using a reference electrode to provide a well-defined surface potential at the Si-NW/solution interface.

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References

(1) Tans, S. J.; Devoret, M. H.; Dai, H. J.; Thess, A.; Smalley, R. E.; Geerligs, L. J.; Dekker, C. *Nature* **1997**, *386*, 474.
(2) Avouris, P.; Appenzeller, J.; Martel, R.; Wind, S. J. *Pr. Inst. Electr. Elect.* **2003**, *91*, 1772.
(3) Lieber, C. M. *Solid State Commun.* **1989**, *107*, 607–616.
(4) Beckman, R.; Johnston-Halperin, E.; Luo, Y.; Green, J. E.; Heath, J. R. *Science* **2005**, *310*, 465.
(5) Cui, Y.; Wei, Q. Q.; Park, H. K.; Lieber, C. M. *Science* **2001**, *293*, 1289.
(6) Kong, J.; Franklin, N. R.; Zhou, C. W.; Chapline, M. G.; Peng, S.; Cho, K. J.; Dai, H. *Science* **2000**, *287*, 622–625.
(7) Li, Z.; Chen, Y.; Li, X.; Kamins, T. I.; Nauka, K.; Williams, R. S. *Nano Lett.* **2004**, *4*, 245.
(8) Beckman, R. A.; Johnston-Halperin, E.; Melosh, N. A.; Luo, Y.; Green, J. E.; Heath, J. R. *J. Appl. Phys.* **2004**, *96*, 5921.
(9) Bunimovich, Y. L.; Shin, Y. S.; Yeo, W.-S.; Amori, M.; Kwong, G.; Heath, J. R. *J. Am. Chem. Soc.* **2006**, *128*, 16323–16331.
(10) Kim, A.; Seong Ah, C.; Young Yu, H.; Yang, J.-H.; Baek, I.-B.; Ahn, C.-G.; Woo Park, C.; Sim Jun, M. *Appl. Phys. Lett.* **2007**, *91*, 1039011−3.
(11) Stern, E.; Klemic, J. F.; Routenberg, D. A.; Wyrembak, P. N.; Turner-Evans, D. B.; Hamilton, A. D.; LaVan, D. A.; Fahmy, T. M.; Reed, M. A. *Nature* **2007**, *445*, 519–522.
(12) Gao, Z.; Agarwal, A.; Trigg, A. D.; Singh, N.; Fang, C.; Tung, C. H.; Fan Y, Y.; Buddharaju, K. D.; Kong, J. *Anal. Chem.* **2007**, *79*, 3291–7.
(13) Xia, Y.; Yang, P.; Sun, Y.; Wu, Y.; Mayers, B.; Gates, B.; Yin, Y.; Kim, F.; Yan, H. *Adv. Mater.* **2003**, *15*, 353.
(14) Fan, H. J.; Werner, P.; Zacharis, M. *Small* **2006**, *2*, 700.
(15) Wagner, R. S. *Appl. Phys. Lett.* **1964**, *4*, 89–90.
(16) Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. *J. Phys. Chem.* **2000**, *104*, 5213.
(17) Schider, G.; Krenn, J. R.; Gotschy, W.; Lamprecht, B.; Ditlbacher, H.; Leitner, A.; Aussenegg, F. R. *J. Appl. Phys.* **2001**, *90*, 3825.
(18) Vieu, C.; Carcenac, F.; Pepin, A.; Chen, Y.; Mejias, M.; Lebib, A.; Manin-Ferlazzo, L.; Couraud, L.; Launois, H. *Appl. Surf. Sci.* **2000**, *164*, 111.
(19) Craighead, H. G.; Howard, R. E.; Jackel, L. D.; Mankievich, P. M. *Appl. Phys. Lett.* **1983**, *42*, 38.
(20) Chou, S. Y.; Krauss, P. R.; Renstrom, P. *Appl. Phys. Lett.* **1995**, *67*, 3113.
(21) Jung, G.-Y.; Johnston-Halperin, E.; Wu, W.; Yu, Z.; Wang, S.-Y.; Tong, W. M.; Li, Z.; Green, J. E.; Sheriff, B. A.; Bouki, A.; Bunimovich, Y.; Heath, J. R.; Williams, R. S. *Nano. Lett.* **2006**, *6*, 351.
(22) Zhou, Y. X.; Johnson, A. T., Jr. *Nano. Lett.* **2003**, *3*, 1371.

(23) Tong, H. D.; Jansen, H. V.; Tas, N. R.; Gadgil, V. J.; Carlen, E. T.; van den Berg, A. *Proceedings of the 14th Intlernational Conference on Solid-State Sensors, Actuators and Microsystems*, Lyon France, June 10−14, 2007, p 191.
(24) Choi, Y.-K.; Zhu, J.; Grunes, J.; Bokor, J.; Somorjai, G. A. *J. Phys. Chem. B* **2003**, *107*, 3340.
(25) Flanders, D. C.; Efremow, N. N. *J. Vac. Sci. Technol., B* **1983**, *1*, 1105.
(26) Tong, H. D.; Chen, S.; Carlen, E. T.; van den Berg, A. *Proc. Eurosensors XXII*, Dresden, Germany, Sept. 07−10 2008.
(27) *FinFETs and Other Multi-Gate Transistors*; Colinge, J.-P., Ed.; Springer Science+Business Media, LLC: New York and London, 2008.
(28) Kingston, R. H.; Neustadter, S. F. *J. Appl. Phys.* **1955**, *26*, 718.
(29) Lim, H. K.; Fossum, J. G. *IEEE Trans. Electron Devices* **1983**, *Ed-30*, 1244–1251.
(30) The MOS flat-band voltage is $V_{FB} \equiv V_{FG}(\psi_s = 0) = \phi_{MS} - Q_{tfo}/C_{fo}$, where ϕ_{MS} is the work function difference between the metal front-gate contact and the silicon layer, Q_{tfo} is the total trapped and fixed charges associated with the front-gate oxide[31] and C_{fo} is the capacitance per unit area of the front-gate oxide.
(31) Deal, B. E.; Sklar, M.; Grove, A. S.; Snow, E. H. *J. Electrochem. Soc.: Solid State Sci.* **1967**, *114*, 266–274.
(32) McDaid, L. J.; Hall, S.; Eccleston, W.; Alderman, J. C. *Solid-State Electron.* **1989**, *32*, 65–68.
(33) Stern, E.; Wagner, R.; Sigworth, F. J.; Breaker, R.; Fahmy, T. M.; Reed, M. A. *Nano. Lett.* **2007**, *7*, 3405–9.
(34) Elfström, N.; Karlström, A. E.; Linnros, J. *Nano Lett.* **2008**, *8*, 945–949.
(35) Li, Z.; Rajendran, B.; Kamins, T. I.; Li, X.; Chen, Y.; Williams, R. S. *Appl. Phys. A: Mater. Sci. Process.* **2005**, *6*, 351.
(36) Cattani-Scholz, A.; Pedone, D.; Dubey, M.; Neppl, S.; Nickel, B.; Feulner, P.; Schwartz, J.; Abstreiter, G.; Tornow, M. *ACS Nano* **2008**, *2*, 1653–1660.
(37) Nikolaides, M. G.; Rauschenbach, S.; Bausch, A. R. *J. Appl. Phys.* **2004**, *95*, 3811–3815.
(38) Elfström, N.; Linnros, J. *Nanotechnology* **2008**, *19*, 235201.
(39) Nicollian, E. H.; Goetzberger, A. *Bell Syst. Tech. J.* **1967**, xxx1055–1133.
(40) $C_p = C_{fo}C_s/(C_{fo} + C_s)$, where $C_s = \pm\, \partial Q_s/\partial V_{FG}$.
(41) Sun, S. C.; Plummer, J. D. *IEEE J. Solid-State Circuits* **1980**, *SC-15*, 562–573.
(42) Mudanai, S.; Chindalore, G. L.; Shih, W.-K.; Wang, H.; Ouyang, Q.; Tasch, Al F., Jr.; Maziar, Christine M.; Banerjee, S. K. *IEEE Trans. Electron Devices* **1999**, *46*, 1749–1759.
(43) Masetti, G.; Severi, M.; Solmi, S. *IEEE Trans. Electron Devices* **1983**, *ED-30*, 764–769.
(44) Kelly, R. G. *Electrochim. Acta* **1977**, *22*, 1–8.
(45) Reza, S.; Bosman, G.; Saif Islam, M.; Kamins, T. I.; Sharma, S.; Williams, R. S. *IEEE Trans. Nanotechnol.* **2006**, *5*, 523.
(46) Schmidt, V.; Senz, S.; Gosele, U. *Appl. Phys. A: Mater. Sci. Process.* **2007**, *86*, 187–191.
(47) Janata, J. Proc. of the 2nd Int. Meeting on Chemical Sensors. 1986, Bordeaux France, 25−31.
(48) Sorensen, M. H.; Mortensen, N. A.; Brandbyge, M. *Appl. Phys. Lett.* **2007**, *91*, 102105.
(49) Lepselter, M. P.; Andrews, J. M. *Ohmic Contacts to Semiconductors*; Schwartz, Bertram, Ed.; The Electrochemical Society, Inc.: New York, 1969; p 159.
(50) Note: the realized silicon nanowires are wider than the metallic masking nanowires. Further optimization of the dry-etching transfer step will result in an improved transfer aspect ratio.
(51) Schroeder, D. *Semiconductor Material and Device Characterization, Third ed.*, 3rd ed.; John Wiley & Sons, Inc.: New York, 2006.
(52) Many of the tested devices had two Si-NWs per electrical contact.
(53) Maddox, Roy L. *IEEE Trans. Electron Devices* **1985**, *ED-32*, 682–690.
(54) Wolf, S.; Tauber, R. N. *Silicon Processing for the VLSI Era*, Vol. 2: Process Integration; Lattice Press, 1990.
(55) Bergveld, P. *IEEE Trans. Biomed. Eng.* **1970**, *17*, 70.
(56) Bousse, L.; de Rooij, N. F.; Bergveld, P. *IEEE Trans. Electron Devices* **1983**, *ED-30*, 1263.
(57) van den Berg, A.; Bergveld, P.; Reinhoudt, D. N.; Sudholter, E. J. R. *Sens. Actuators* **1985**, *8*, 129–148.
(58) van Hal, R. E. G.; Eijkel, J. C. T.; Bergveld, P. *Sens. Actuators, B* **1995**, *24−25*, 201–205.
(59) Shockley, W. *Proc. I.R.E.* **1952**, *40*, 1365–1376.
(60) Sze, S. M. *Physics of Semiconductor Devices*, 2nd ed.; John Wiley & Sons, Inc.: New York, 1981.
(61) $f_d(V_{FG}, V_{FB}, N_a, C_{fo}) = \xi(V_{FG} - V_{FB} + \xi^2/4C_{fo}^2)^{1/2} - \kappa_s\varepsilon_0/C_{fo}$, where $\xi = (2\kappa_s\varepsilon_0 q N_a)^{1/2}$.
(62) Shockley, W.; Pearson, G. L. *Phys. Rev.* **1948**, *74*, 232–233.
(63) Brews, J. R. *Solid-State Electron.* **1978**, *21*, 345–355.
(64) Bousse, L. *J. Chem. Phys.* **1982**, *76*, 5128.
(65) Yates, D. E.; Levine, S.; Healy, T. W. *J. Chem. Soc., Faraday Trans. 1* **1974**, *70*, 1807.
(66) Cristoloveanu, S.; Gardener, S.; Jaussaud, C.; Margail, J.; Auberton-Hervé, A. J.; Bruel, M. *J. Appl. Phys.* **1987**, *62*, 2793–2798.

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