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An interface board for the control and data acquisition of the Medipix2 chip

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Abstract

We have designed an interface board between the Medipix2 chip and a general-purpose commercial PCI-based acquisition card, making the Medipix2 fully controllable from a PC. The main component on the board is an FPGA that implements the data transmission between the chip and the PC, as well as a number of internal registers to control the operation of the chip. Besides the FPGA, the board also includes a number of data converters for different purposes, a timing source, power supply regulators to generate the power supply voltage needed by the chip, and some level converters to accommodate the different logic levels at the PC, FPGA and Medipix2 chip.

The board has been designed to interface with a chip-board containing a maximum of eight Medipix2 chips. The Medipix2 chips are read out via their serial data interface using the LVDS standard.

We will describe the design of the board, its operational characteristics and show how the board has been used to characterize the Medipix2 chip.

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1. Introduction

The Medipix series of photon counting X-ray imaging readout chips is a spin-off of research done at CERN in the area of readout chips for pixel detectors used in high-energy physics experiments [1]. Two chips have been designed and manufactured: the Medipix1 chip [2] (also known as PCC or Photon Counting Chip) and the Medipix2 chip [3,4].

Originally, the Medipix1 system consisted of a readout chip, a sensor and a complex VME-based control and data acquisition system. A much simpler and cheaper system (MUROS1[2] [5] was developed at NIKHEF, and it has become standard in almost all Medipix1 characterization

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[2] MUROS stands for Medipix re-Usable Read Out System.

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and application uses. The key characteristics of the MUROS1 system were its use of "off-the-shelf" components such as a conventional PC with two data acquisition cards (one for digital signals and another one for analog signals), and a simple interface board (the MUROS1 board itself) which served as a "buffer" between the PC and the chip, as well as generating the power supply levels and the analog test pulse.

In this paper, we report on the design and manufacture of a similar system, this time for the Medipix2 chip, called MUROS2. Our goal has been to develop and manufacture a simple system for the data acquisition and the control of the Medipix2 chip. As in the MUROS1 case, we only use "off-the-shelf" components to make the system simple, testable and affordable. The main characteristics of the system are: full digital control of the PC over the MUROS2 board (the Medipix2 chip itself is also fully digitally controlled); maximum flexibility by the use of programmable logic; and the use of serial data transmission in order to minimize the number of connections between the Medipix2 chip and the MUROS2 board. Our design was targeted for use with a system containing a maximum of eight Medipix2 chips [6]. A total of 25 MUROS2 boards have been manufactured and tested and are currently operational.

The next section describes the components found on the board. Section 3 goes into more detail on the control and data acquisition. Section 4 explains the design and manufacture process of the MUROS2 board. Section 5 illustrates the use of MUROS2 together with the Medipix2 chip and the Medisoft4 software [7]. Finally, we conclude by pointing out further research topics.

2. Board components

Fig. 1 shows a block diagram of the MUROS2 system. The power supplies and the analog references for the data converters are omitted for simplicity. MUROS2 is connected to a PCI digital acquisition card inside the PC on one side and to a board containing the Medipix2 chips on the other. Additionally, a general purpose 32-bit input/output connector is also present in MUROS2.

The functional blocks inside the FPGA in the figure will be discussed in more detail in Section 3.

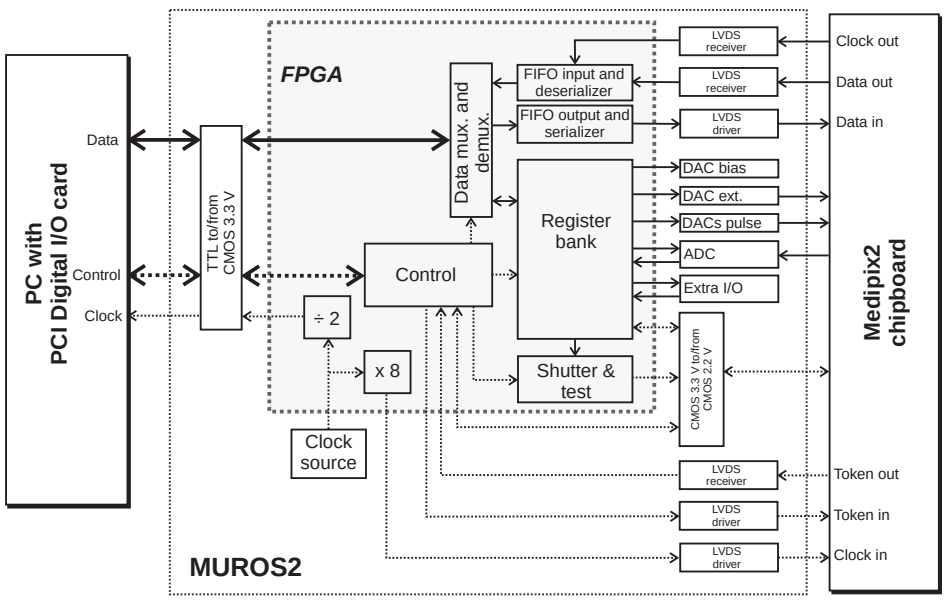

Fig. 1. Block diagram of the MUROS2 system.

We will briefly mention now the remaining components found on the board.

The main clock source (*Clock Source* in the figure) generates a clock signal with an adjustable frequency between 7 and 30 MHz. From this signal, two additional clock signals are created. The first one has a frequency equal to half the frequency of the main clock source, and it is used for the data communication between the PC and the MUROS2 board. Using the PLL inside the FPGA, we multiply the frequency of the original clock signal by eight to generate the second additional clock signal, used for the data transmission between MUROS2 and the Medipix2 chips. The reason for the 16 to 1 clock ratio between the PC-MUROS2 and the MUROS2-Medipix2 data transmission is that the former is realized via a 16-bit-wide parallel bus, while the latter is done via a 1-bit serial link. Hence, to keep the same data rate at both ends one needs to scale the clock frequencies with a factor 16.

A number of digital transceivers are also found in MUROS2 to translate between the different logic levels used by the PC (TTL), the FPGA (3.3 V CMOS) and the Medipix2 chip (2.2 V CMOS).

The MUROS2 board includes four Digital-to-Analog-Converters (DACs) and one Analog-to-Digital-Converter (ADC). *DAC bias* in Fig. 1 generates a value between 0 and 5 V that can control the external high voltage power supply used to bias the detector in the Medipix2 system. *DAC external* can override one of the internal DACs in the Medipix2 chip [3]. The other two DACs are used together to control the amplitude and polarity of the analog test pulse as described later in Section 3.3. Finally, the ADC measures the values of the internal DACs in the Medipix2 chip for calibration purposes.

The power supply subsystem in the MUROS2 board delivers the appropriate supply voltages to the Medipix2 chips as well as to the internal components in the MUROS2 board. Only one external 3.3 V power supply is needed, all other values are generated in MUROS2 from this external supply and the 5 V given by the PC via the connection with the digital acquisition card.

3. Control and data acquisition

The most important part of the MUROS2 board is the control and data acquisition subsystem. We have implemented this subsystem in an EP20K100E FPGA from Altera [8]. Fig. 2 shows a block diagram of the functional blocks inside the FPGA. The clock generation circuitry is not shown for clarity purposes.

The 32-bit wide bus connecting the PCI-based acquisition card located in the PC and the MUROS2 board is divided in two blocks. Sixteen bits are used as asynchronous control signals, and the other 16 bits are used as data lines for synchronous parallel data transfer between the

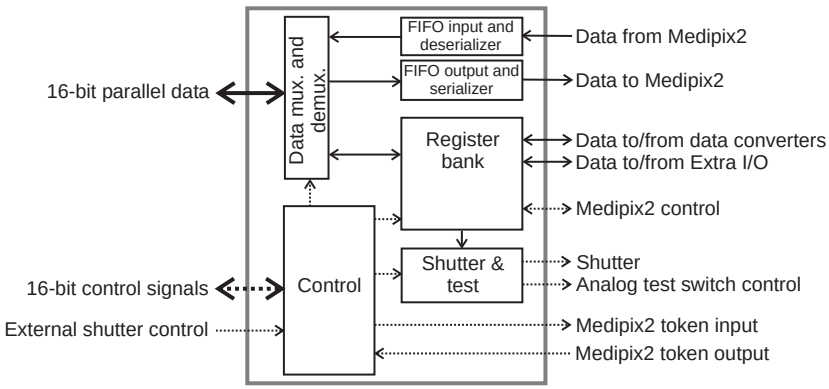

Fig. 2. Block diagram of the FPGA that implements the control and data acquisition.

PC and the MUROS2 board. Depending on the status of the control lines, the data is routed to the Medipix2 chipboard or to the register bank.

There are a total of 12 registers which are used to control the data converters in the board, the image acquisition modes in Medipix2, the operation mode of the Medipix2 chips and the extra I/O bus present in the MUROS2 board. All registers can be written and read, except a read-only register that stores information about the version of the code loaded into the FPGA.

3.1. Medipix2 data transfer

The contents of the pixel counters can be read from the Medipix2 chip in two different ways: using a 32-bit parallel bus or using a 1-bit LVDS line. In order to load the configuration bits for the pixels in the matrix, as well as for programming the internal bias DACs, only the 1-bit LVDS line can be used. MUROS2 only supports 1-bit serial data readout. We made the choice to focus MUROS2 development as well as further research into serial data communication. If the chipbard contains more than one chip, they are connected in *daisy chain* mode.

The serial protocol implemented in Medipix2 uses six different signals: *data* (input and output), *clock* (input and output) and *token* (input and output). All six signals use the LVDS[3] standard. The low-voltage swing (around 350 mV) is good for achieving a low power dissipation and fast switching. Differential signalling helps against EMI[4] and common-mode noise.

MUROS2 sends the data aligned to its output clock. In order to read the data coming from the Medipix2 chip correctly and to take into account any delay or skew introduced by cabling or by other chips (if connected in daisy chain), the data arriving to MUROS2 is read at the edges of the clock coming out of the Medipix2 chip and not of the clock going out of MUROS2.

The LVDS transmitters and receivers in MUROS2 are not implemented in the FPGA, but are external components. The reason for this is that the FPGA model we used has only two LVDS I/O ports and we need six of them, as mentioned in the previous paragraph.

The token signal is of importance specially in the case where more than one Medipix2 chip needs to transfer or receive data, and the chips are connected in daisy chain. When a Medipix2 chip receives the token, it can put the contents of its pixel counters into the data output line. All other Medipix2 chips in the daisy chain are in "transparent mode" connect directly their data inputs to their data outputs.

In order to transmit data between the PC and the Medipix2 chipboard, two extra blocks are needed in order to serialize and deserialize the data. The serialization block converts the 16 bits of data coming from the PC to the 1-bit data stream for the Medipix2 chip. The deserialization block converts the 1-bit stream from the Medipix2 chips into 16-bit words to be transferred to the PC. Each block includes one FIFO to decouple the communication MUROS2-PC from the MUROS2-Medipix2. The depth of these FIFOs can be adjusted by reprogramming the FPGA.

3.2. Control of the image acquisition modes

The most essential part of the system is the control of the image acquisition of the Medipix2 chip. Image acquisition in the Medipix2 chip is governed by a *shutter* signal. When this signal is high (shutter closed), the pixel counters do not count and their contents can be read out of the chip. When the signal is low (shutter open), the pixel counters enter counting mode and readout operations are suspended.

MUROS2 implements five different image acquisition modes or ways to control the *shutter* signal. These modes are selected by writing into one of the registers in the FPGA (the *Configuration Register*). In the first mode, the control of the shutter signal is accomplished directly by setting one of the bits of the Configuration Register.

The second mode includes the possibility of using a timer. First, the number of clock cycles that one wants the shutter to be open is loaded into the *Timer Register*. Next, one writes into the shutter bit in the Configuration Register to start

[3] LVDS stands for Low Voltage Differential Signalling.

[4] EMI stands for Electromagnetic Interference.

the acquisition. When the number of clock cycles loaded in the Timer Register has elapsed, the shutter is automatically closed.

The third and fourth modes work similar to the previous two, only instead of using the bit in the Configuration Register, an external signal is used to control the shutter.

The fifth image acquisition mode is the so-called *continuous acquisition* mode. This mode can be used to acquire "movie-like" image sequences, without having to worry about possible latencies in the PC. First, the number of exposures (or frames) is loaded into the appropriate register. Then, the duration of each exposure is loaded into the Timer Register. When the shutter bit in the Configuration Register is set, the acquisition begins. After each exposure is finished, MUROS2 will automatically begin to read the data from the Medipix2 chip, and when the data has been completely read out, the next exposure will start. During the full process, the PC only needs to be in "reading data" mode. Alternatively, the triggering of the exposures can be controlled by an external signal.

3.3. Control of the analog test pulse generation

A much used and important feature of MUROS1 is the ability to generate test pulses that can be used to test the Medipix1 chips electronically before bump bonding to a sensor. This feature is also implemented in MUROS2.

In MUROS2 two identical DACs determine the high and low levels of the test pulse. Additionally, a train of digital pulses is generated in the FPGA. These three signals (both analog values and the train of digital pulses) are then sent to the chipboard, where they are used as inputs to an analog multiplexer. This multiplexer switches its output between the two DAC values at a rate controlled by the digital pulses. This method allows the test pulse to be generated as close as possible to the chip, thereby minimizing the influence of distortion and attenuation. The Medipix2 chip allows for the collection of both electrons and holes. Both polarities can also be tested electronically by setting the values of the DACs appropriately.

4. MUROS2 design and manufacturing

The main design effort has been on the programming of the FPGA. This could be done in parallel to the design of the Medipix2 chip itself thanks to the availability of Verilog models for the control and data transmission part of the Medipix2 chip. The code for the FPGA was also written in Verilog and the functionality of MUROS2 connected to a Medipix2 chip could be easily simulated.

The schematic entry of the Muros2 board was done at NIKHEF, but the final layout and manufacture of the boards was outsourced. Fig. 3 shows a photograph of the final board. The board was manufactured in a standard PCB process with six copper layers and its dimensions are 180 by 170 mm.

Because MUROS2 is designed to be used with one to eight Medipix2 chips, special care was taken in the design of the board's housing to allow for proper dissipation of the heat generated by the voltage regulators when eight Medipix2 chips are used. The photograph also shows an aluminium block where the regulators are mounted.

5. Using MUROS2 with the Medipix2 chips

The MUROS2 board, together with the Medisoft4 software, has been used successfully to characterize the Medipix2 chips. Fig. 4 shows a screen capture from Medisoft4 showing the data read from one chip after loading a mask into the chip and performing an analog test.

Twelve Medipix2 wafers, each containing 98 chips, have been tested using the MUROS2 board together with the Medisoft4 software.

Tests have shown that maximum data rates above 100 Mbit/s are possible. The data rate that can be reliably achieved with the current MUROS2 system is about 160 Mbit/s. Taking into account that each Medipix2 chip contains 851968 bits of data, the minimum readout time is 5.734 ms/ chip.

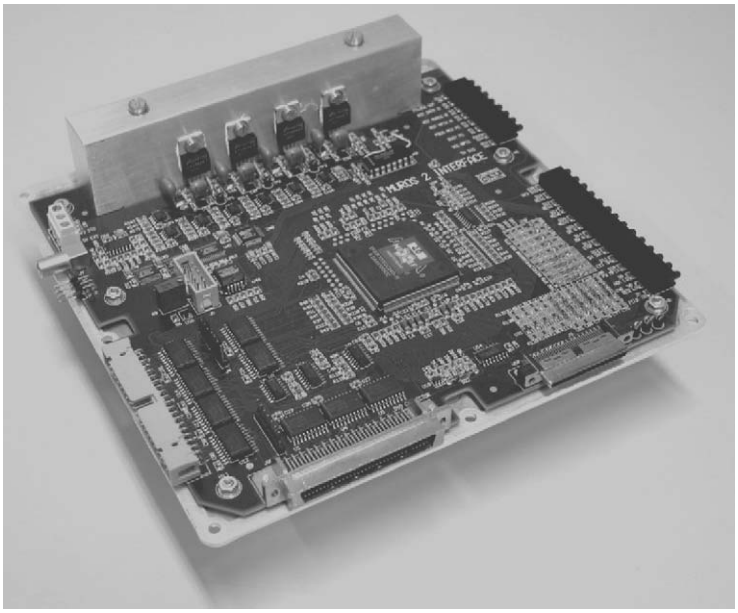

Fig. 3. Photograph of the MUROS2 board.

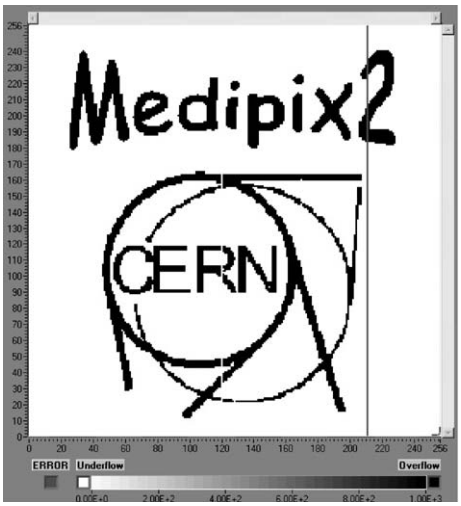

Fig. 4. Screen capture from Medisoft4 software after using MUROS2 to load a mask into a Medipix2 chip, applying test pulses to the selected pixels and reading out the values. The black pixels have 1000 counts and the white 0. The threshold was approximately 4000 electrons and the input charge per event was about 8000 electrons.

6. Conclusions and future work

We have designed a control and data acquisition board for the Medipix2 pixel readout chip that has been manufactured and is being successfully used for measuring and characterizing the Medipix2 chips. Modifications and improvements to the system can be easily accomplished by merely changing the FPGA program without having to physically modify the board itself.

At present time, there are two limitations to the maximum data rate that can be achieved with the current system: the maximum data rate allowed by the FPGA (160 Mbit/s for the FPGA in our design) and the maximum data rate supported by the Medipix2.

The first problem is being solved by the FPGA manufacturers themselves, and already at the time of writing this paper some manufacturers offer FPGA with integrated serializers–deserializers running at 3.7 Gbit/s rates. The main remaining challenge is finding ways to increase the data rate at the pixel readout chip itself. There are already chips that allow data rates of 10 Gbit/s [9].

Another direction for further research is the elimination of the PCI card in the PC in order to further simplify the system, either by including the PCI bridge in MUROS2 or by using a different communication protocol such as, for example, USB or IEEE-1394.

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