The electrical conduction and dielectric strength of SU-8

2009 J. Micromech. Microeng. 19 065012

(http://iopscience.iop.org/0960-1317/19/6/065012)

J. Micromech. Microeng. **19** (2009) 065012 (7pp) doi:10.1088/0960-1317/19/6/065012

The electrical conduction and dielectric strength of SU-8

Joost Melai[1,3], Cora Salm[1], Sander Smits[1], Jan Visschers[2] and Jurriaan Schmitz[1]

[1] Semiconductor Components, MESA+ Institute, University of Twente, Enschede, The Netherlands
[2] NIKHEF, Amsterdam, The Netherlands

E-mail: j.melai@utwente.nl

Received 19 January 2009, in final form 29 March 2009
Published 20 May 2009
Online at stacks.iop.org/JMM/19/065012

Abstract
This paper presents a study on the dielectric behavior of SU-8 photoresist. We present measurements on the leakage current levels through SU-8 layers of varying thickness. The leakage current is dominated by thermionic emission. We have further determined the dielectric strength of SU-8 to be 4.4 MV cm^{-1}. The remarkably high dielectric strength allows the material to be used for high-voltage applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

SU-8 negative tone photoresist [1] is widely used in microtechnology. SU-8 can be spin cast with thicknesses covering a broad range from 1 μm to 1 mm. For this a series of products differing in viscosity are available [2]. These layers can be patterned using standard UV lithography techniques, for instance using mask-aligners for contact lithography. Very high aspect ratio structures can be made, both for dark-field and light-field structures (although light-field structures are more difficult to develop).

Initially SU-8 was intended for use as a sacrificial photoresist mask, for instance for molding processes [3]. These applications are well matched to the strengths of SU-8 mentioned above; they do, however, require the SU-8 to be removed. This has proven to be one of the main bottlenecks in using SU-8. Because the material is very hard and stable, it is difficult to remove it successfully [4, 5].

Successful stripping can for instance be achieved with (long) O_2 plasma ashing or Piranha cleaning. Both of these can have detrimental effects on, for instance, many different metal layers. As a result other types of resists have been formulated for sacrificial applications, for instance KMPR [6]. There have been efforts on using SU-8 in combination with a dedicated release layer, and a nice application of this technique is shown in [7]; also many alternative release layers are referenced. This technique is complicated; successful stripping is not guaranteed because the release step is very geometry dependent and the released structures can break upon release if they are too brittle.

The majority of reported applications currently use SU-8 as a structural material. The cross-linked material is an integral part of the device that is not removed in later processing. The material has been used to make micro-fluidic devices, cantilevers, optical devices and many other structures. Many examples are referenced in an excellent review publication [8] on SU-8, focusing on lithographic patterning capabilities. The mechanical aspects have also been studied widely [9–11]. Other studies have been performed on the radiation hardness of SU-8 [12], which is interesting for sensor and space applications.

Recent work [13] shows the use of a suspended metal grid supported with SU-8 pillars over a CMOS imaging chip to make a gaseous radiation imaging detector. In these so-called InGrid (integrated grid) detectors a large bias voltage is applied to the grid so that, by inducing a controlled electron avalanche in the gas above the chip, single electrons can be detected. For this and similar electron multiplication structures (such as the structure discussed in [14]), high electric fields are essential and thus the dielectric (SU-8) has to withstand a considerable electric bias voltage. We have investigated the dielectric strength (DS) of SU-8 in order to find out the limits of the material for high-voltage (HV) applications. We reported our first findings in [14]. The present paper presents new data from improved test structures that allow us

[3] Author to whom any correspondence should be addressed.

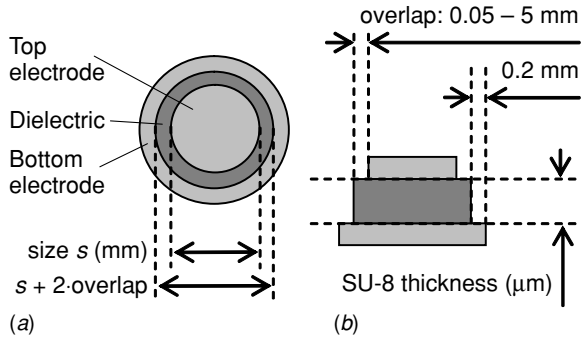

Figure 1. Illustration of an SU-8 capacitor test structure, top view (*a*) and cross-section (*b*). The most important design parameters are the size and the SU-8 overlap which determines the degree of isolation.

to quantify the dielectric strength. This parameter has not been studied extensively in the literature. Some statements can be found on websites. Reference [2] contains a datasheet for the special purpose SU-8 2000 and 3000 products, on this datasheet the dielectric strength is specified as 1.1–1.2 MV/cm, measurement conditions or other details are omitted.

The dielectric strength is defined as the maximal electric field (E_{BD}) that can be applied before immediate breakdown for a given thickness. For well-designed test structures (with effective edge termination), the dielectric strength approaches the one-dimensional critical field strength of the material. Generally, for long-term stability, a system should operate at fields well below the dielectric strength of the materials used.

2. Experimental details

Many applications use SU-8 layers with a thickness of several tens of micrometers. It is very difficult to directly test the dielectric strength of such thick layers because the extremely high test voltages require exotic equipment and safety precautions. Besides, the edge termination (to avoid early breakdown at the edges) of test structures becomes much harder to make. For these reasons, we have carried out breakdown tests only on thinner structures, with SU-8 thickness in the range of 2–15 μm. Breakdown voltages are then well below 10 kV. These layers are made of SU-8 2 and SU-8 5, which are different formulations of the same material, differing only in the fraction of solvent. The final epoxy matrix is the same and we therefore expect that the results obtained are of general relevance to other SU-8 layers.

2.1. Electrical test structures

The test structures used for dielectric strength evaluation are metal–insulator–metal (MIM) capacitors with a mesa layout. Figure 1 shows a device with a concentric circular layout.

The overlap of the bottom electrode over the dielectric is always 0.2 mm on all sides. The overlap of SU-8 over the top electrode is varied from 0.05 mm to 0.2 mm and in another set of devices from 0.2 mm to 5 mm. These large overlap values are intended to keep the surface leakage current negligible.

The lateral size of the devices is in the millimeter regime. The abnormally large surface area of the devices is needed to obtain measurable results with our test equipment, both in terms of leakage current and capacitance, when the dielectric thickness is increased to tens of micrometers.

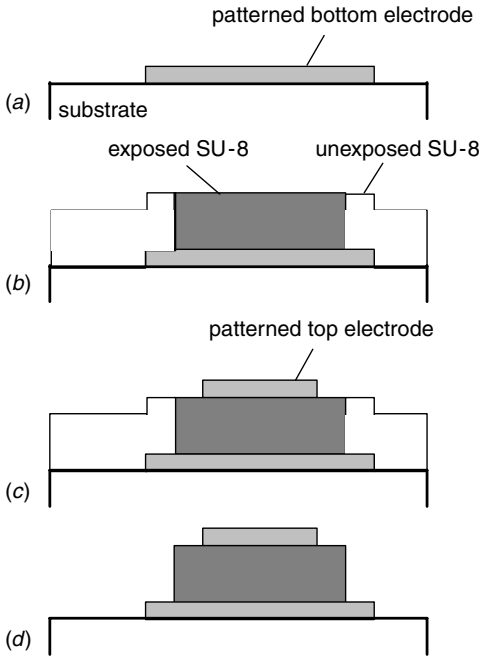

Figure 2. Overview of the processing sequence followed to make the test structures.

2.2. Processing of test structures

The test structures presented in this paper are made in a manner similar to that of the suspended grid structures presented in [13]. The process is illustrated in figure 2. The SU-8 processing follows the guidelines from the vendor [2], unless specified otherwise.

First, the metal bottom electrode is made by sputtering 1 μm of Al on top of a substrate. The devices are made on top of a carrier Si substrate with a thermally grown oxide layer of approx. 900 nm. The Al is patterned using lithography, PAN etchant (phosphoric-acetic-nitric acid) at 55 °C and resist strip (10 min fuming HNO_3), see figure 2(*a*).

SU-8 is spun on using a conventional spin coater with spin speeds in the range 1000–3000 rpm. After spinning, the layer is first left to settle for 40–60 min on a hotplate set to room temperature (RT); this reduces the edge bead. Then, the temperature of the hotplate is increased, for a soft bake at 95 °C. The temperature is ramped up and down very slowly to prevent cracking of the layers [15].

Conventional UV contact lithography is used to pattern the (negative tone) SU-8. In the exposed regions, an acid is generated by the photo-acid generator; this acid initializes the cross-linking of the polymer material. After the exposure, a post-exposure bake (PEB) is performed to accelerate the cross-linking reaction and to improve the contrast of the image. During the PEB, it is also important to prevent temperature shocks. Therefore, the heating is slowly increased from RT to 80 °C and then lowered gently back to RT. The resulting structure is depicted in figure 2(*b*).

Table 1. Process conditions used to fabricate different SU-8 layers.

Material type	Spin speed (rpm)	Soft-bake time (min)	Exposure dose (mJ cm^{-2})	PEB time (min)	Measured thickness (μm)
SU-8 2	2000	4	140	4	2.16–2.25
SU-8 2	1500	4	140	4	2.74–2.85
SU-8 2	1000	4	140	4	3.88–3.93
SU-8 5	3000	4	140	4	4.97–5.09
SU-8 5	2000	7	180	5	7.1
SU-8 5	1000	7	180	5	13.1
2 × SU-8 5	2000	2 × 7	240	5	19.0

In standard SU-8 processing, the resist image is now developed by washing away the unexposed uncross-linked regions of the photo-resist with a suitable solvent. This can be acetone or the standard SU-8 developer PGMEA. After the development, the wafers are rinsed with isopropyl alcohol (IPA) to improve the drying. Water rinsing is avoided because water may seep into the layers and deteriorate the layer quality and performance. After development, a final hard-bake (HB) step may be given to strengthen the layer, remove small cracks and improve adhesion [16, 17]. This is normally done on a hotplate at temperatures between 120 °C and 180 °C [2].

The main difference with the standard processing described is that for the MIM capacitor structures (as well as for the suspended grid structures referenced above), the development step is delayed until the top electrode is formed. The uncross-linked SU-8 is used as a sacrificial material for support of the top aluminum layer. This is the most straightforward method to reliably define mesa structures of this type.

On top of the SU-8 layer, a 500 nm thick Al electrode layer is deposited by low power sputtering. This metal layer is patterned in the same way as the bottom electrode (figure 2(*c*)).

Finally, the SU-8 layer is developed. By design all unexposed, uncross-linked regions are directly exposed to the developer. Development is done by immersion in acetone at RT using ultrasonic excitation. The development progress is checked visually. Development takes between 5 and 10 min depending on the layer thickness. The final result is shown in figure 2(*d*).

The deposition parameters have been optimized for mesa structures; they are different from the settings used for the suspended structures in [13]. Despite the optimization, it is still possible that a skin of cross-linked SU-8 forms at the top of the unexposed sections of the resist layer. The long development times and ultrasonic excitation are needed to remove these thin skins of (partially) cross-linked material. An additional cleanup step is performed in Microstrip 5010 (∼30 min, room temperature) to remove residues.

The layer thickness of SU-8 was varied by using the spin conditions given in table 1. Two different dilutions of SU-8 have been used to reach the required thicknesses. The different layers also require adjustments to the baking times and the exposure dose. The thickest layer has been made by repeating the coat and soft-bake step.

The final thickness after processing has been measured using a Dektak profiler. Each thickness given in the table is an average over 5–10 measurements. The experiments on the first four thinner layers have been repeated several times; the thickness range given is the range found among the averages for all wafers.

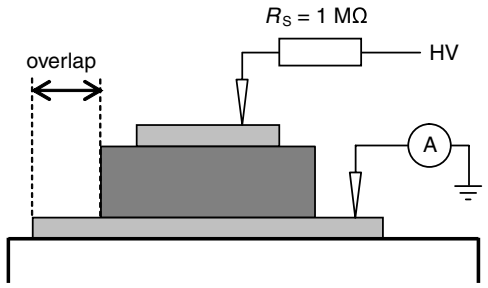

Figure 3. Measurement set-up showing the device connected to the SMU of an HP 4156 parameter analyzer used as a current-meter and the high-voltage bias connected in series with a high-ohmic protection resistor.

2.3. *Electrical characterization*

High voltage current-voltage (HV-*IV*) measurements are performed on a Karl Süss PM8 probe station using a purpose-built probe with a non-conductive arm. We measured *I*–*V* characteristics by applying a bias voltage using a Fug HCN 200 K-12500 source and measuring the current with the SMU of an HP 4156B Parameter Analyzer. The measurement set-up is shown in figure 3.

To prevent discharges, a special, dedicated probe has been made. In a normal probe, the coaxial (or triaxial) orientation of the signal and ground/shield leads is maintained very close to the probed surface in order to limit aberrations due to capacitive/inductive coupling. With our HV probe, however, the shield ends some distance (several centimeters) before the probe needle to prevent discharges. The probe arm is made out of Teflon (instead of metal). The mechanical manipulator is that of a standard Karl Süss probe. Figure 4 shows the purpose built probe. The cables are interconnected using Radiall SHV connectors. All measurements were done under N_2 atmosphere. To prevent deformation of the SU-8 layer by the probing needle, the contact has to be made relatively gently. Probing is always aimed at the center of the top electrode. Reproducible leakage currents are obtained in a large range of needle pressure. Until breakdown, no material deterioration of the probe location is observed; in the event of breakdown through the dielectric, the destruction of the layer starts at the probe location.

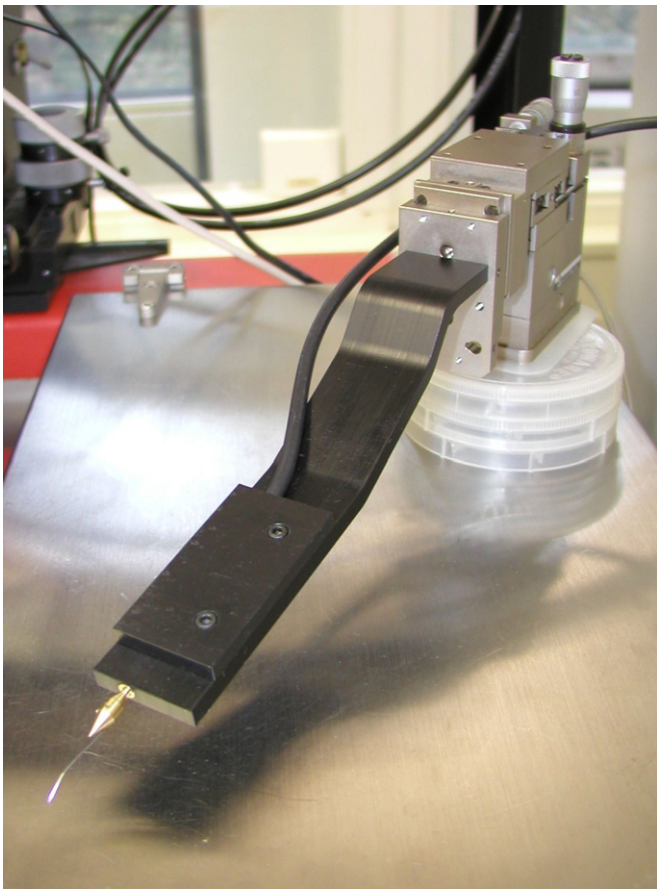

Figure 4. HV probe made by replacing the metal arm (optimized for coaxial shielding) with a Teflon arm optimized for isolation width.

The other terminal of the device is contacted with a standard SMU of an HP 4156B parameter analyzer. This terminal is kept at 0 V, and the current is sampled continuously using a long integration time. Typically it takes 2–5 s for the current to stabilize.

To limit the dielectric breakdown discharge current as well as to shield the current sensing SMU from the high voltage, a protection resistor is connected in series with the device at the high side. For the presented measurements, we have used a resistor network with an effective 0.99 MΩ series resistance and a maximum power rating of 8 W.

Additional measurements have been performed on thicker layers (7–19 μm). These measurements are made using a simpler set-up. Precise measurement of the current is not possible but higher voltages can be reached. The bottom electrode is grounded; the high voltage is applied using a Danbridge JP-30-A high-voltage source.

3. Results and discussion

3.1. Low-field conduction

We have measured bottom electrode current as a function of (positive) bias voltage applied to the top electrode. The bias was increased in steps of 50 V. Each time the current level is recorded after it has stabilized. The current increases steadily with voltage. Figure 5 shows *J*–*V* curves (average and 1σ spread) obtained from a series of nine devices on four different wafers with a varying SU-8 layer thicknesses. The current density is calculated by dividing the current with the top electrode area as measured after processing. We assume that the current mainly consists of a bulk component that scales with the electrode area and a surface (overlap) component that scales with the perimeter. From the initial results, we conclude that well before breakdown ($V < 1000$ V), the area component is dominant.

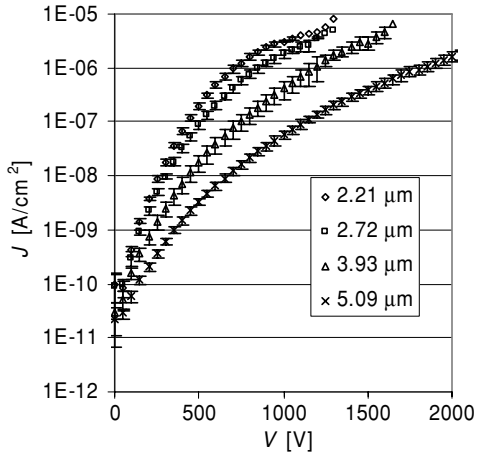

Figure 5. *J*–*V* characteristics (average and 1σ spread) of different MIM capacitors with a varying SU-8 thickness as stated in the legend. The current decreases with increasing thickness.

3.2. Conduction mechanism

Conduction through the structure is influenced by two components: the conduction through the dielectric itself and the injection of carriers into the structure from the electrodes. By careful observation of the leakage currents, we have determined which mechanism is the limiting factor.

The *J*–*V* characteristics presented in figure 5 show that the behavior is strongly non-ohmic, suggesting that the transport is dictated by injection from the dielectric–metal interface. In fact, if the current density is plotted against the electric field strength E (shown later), we see that the curves for devices with different thicknesses fall on top of each other over almost the entire range. This proves that the conduction is not limited by resistance in the layer, which must scale with thickness.

The electric field strength E is defined in (1), where V is the bias voltage and t is the thickness of the SU-8 layer:

$$E = \frac{V}{t}. \tag{1}$$

Because the electric field strength is not very high, we assume that Fowler–Nordheim injection is limited and that thermionic emission is dominant. Thermionic emission [18] can be described by the formula given in (2). Here, J is the current density, A is the Richardson constant, T is the absolute temperature, W is the energy of the charge carriers and k is the Boltzmann constant (8.620×10^{-5} eV K^{-1}):

$$J = A \cdot T^2 \cdot \exp\left(\frac{-W}{kT}\right). \tag{2}$$

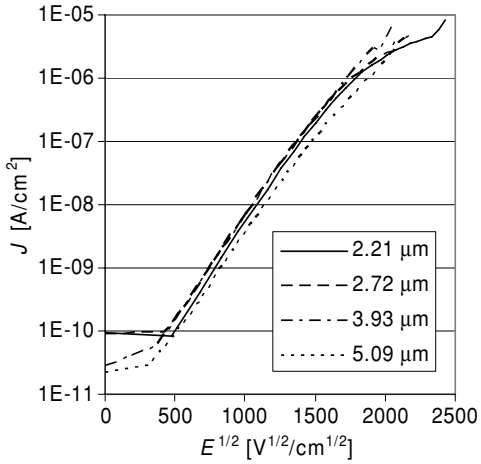

Figure 6. Leakage current density versus the square root of the electric field strength for devices with different SU-8 thicknesses.

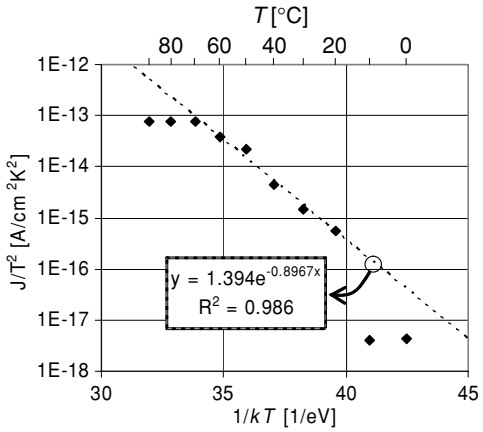

Figure 7. Plot of J/T^2 versus $1/kT$; leakage current density is measured at a bias voltage of 200 V. The temperature was varied from 0 to 90 °C.

The carrier energy W is determined, as shown in (3), by φ_{Al}, the work function of Al (4.28 eV), $\chi_{\mathrm{SU\text{-}8}}$, the electron affinity of the dielectric SU-8, and ΔW, a barrier lowering due to the applied bias:

$$W = \varphi_{\mathrm{Al}} - \chi_{\mathrm{SU\text{-}8}} - \Delta W. \tag{3}$$

The shift ΔW due to the bias field strength is defined in (4), where e is the electron charge (1.602×10^{-19} C), E is the electric field strength, $\varepsilon_{\mathrm{rel}}$ is the relative permittivity of the dielectric (∼4) and ε_0 is the absolute vacuum permittivity (8.854×10^{-14} F cm^{-1}):

$$\Delta W = \left(\frac{e \cdot E}{4\pi \cdot \varepsilon_{\mathrm{rel}} \cdot \varepsilon_0}\right)^{1/2}. \tag{4}$$

Combining equations (2)–(4), we obtain the following expression (5) for the logarithm of the current density $\log(J)$:

$$\begin{aligned} \log(J) &= C + \theta \cdot \sqrt{E} \\ C &= \log\left(A \cdot T^2 \cdot \exp\left(\frac{-(\varphi_{\mathrm{Al}} - \chi_{\mathrm{SU-8}})}{kT}\right)\right) \\ \theta &= \left(\frac{e}{4\pi \cdot \varepsilon_{\mathrm{rel}} \cdot \varepsilon_0}\right)^{1/2} \cdot \frac{1}{kT}. \end{aligned} \tag{5}$$

In figure 6, the leakage current through the SU-8 layer is plotted logarithmically against the square root of the electric field across the dielectric. This is done for four different SU-8 layer thicknesses. As can be seen in the plot, the leakage current scales logarithmically with the square root of the electric field in a wide current range.

The leakage current level is determined by the electric field strength at the interface where the current is injected; it does not depend on the SU-8 layer thickness as can be seen by the nearly identical curves obtained for the different layers. Only the wafer with the thickest SU-8 layer (5.09 μm) has slightly lower current. This cannot be explained by measurement errors in the bias voltage or the thickness of the layer. It is noted however that the three thinner layers are made with SU-8 2 whereas the thickest layer is made with the more viscous SU-8 5 product.

The leakage current density is strongly temperature dependent. Equation (1) is reformulated as (6)

$$\frac{J}{T^2} = A \cdot \exp\left(\frac{-(\varphi - \Delta\varphi)}{kT}\right). \tag{6}$$

Figure 7 shows J/T^2 plotted against the inverse of thermal energy kT (in units 1 eV^{-1}). We see that for the temperature range from room temperature until 80 °C (which is just below the highest temperature reached during processing of the structure), the metric $\log(J/T^2)$ scales with the inverse of temperature.

The linear behavior seen in the two graphs presented points out that the leakage current is determined by thermionic emission of carriers from the Al electrodes into the dielectric material.

Using a logarithmic fit made to the data presented in figure 7, the coefficients A and energy W ($=\varphi - \chi - \Delta W$) can be determined. We obtain a value of $A = 1.394$ A cm^{-2} K^{-2}. The Richardson constant is a physical parameter which is linearly proportional with the effective mass of the electron. In vacuum, where $m_{\mathrm{e}} = m_0$, the value of A is 120.2 A cm^{-2} K^{-2}. Our measurement suggests therefore that the effective mass of electrons in SU-8 is around $0.012\ m_0$.

The carrier energy is $W = 0.9$ eV. At a bias level $V = 200$ V, the shift ΔW is found to be only 0.12 eV.

The difference in work function from the metal to the dielectric is therefore $0.9 + 0.12 = 1.02$ eV. The work function of Al is 4.28 eV. We find an electron affinity of 3.24 eV for SU-8.

3.3. Dielectric strength

When the bias is increased, breakdown occurs, at which point the current rapidly increases and saturates. The breakdown causes irreversible damage to the device. We have seen that breakdown occurs in the middle of the device, through the dielectric. Figures 8(*a*) and (*b*) show the device before and after such breakdown events. Also, in some cases, we have seen breakdown laterally across the isolation width from the

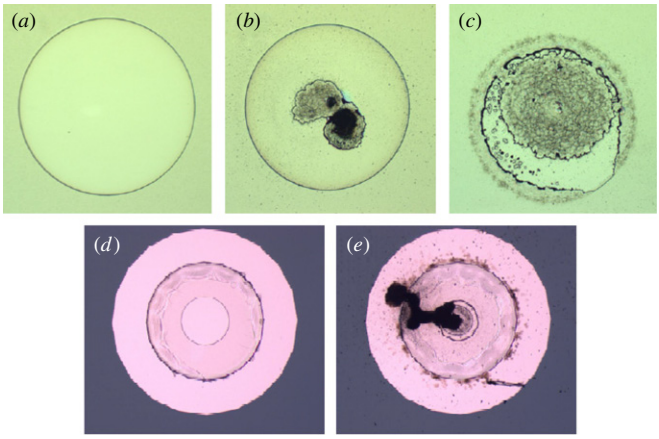

Figure 8. Top electrode area of devices, (*a*) before breakdown measurement, (*b*) after center (bulk) breakdown, (*c*) prolonged edge breakdown, (*d*) device with small isolation width before breakdown and (*e*) after edge breakdown.

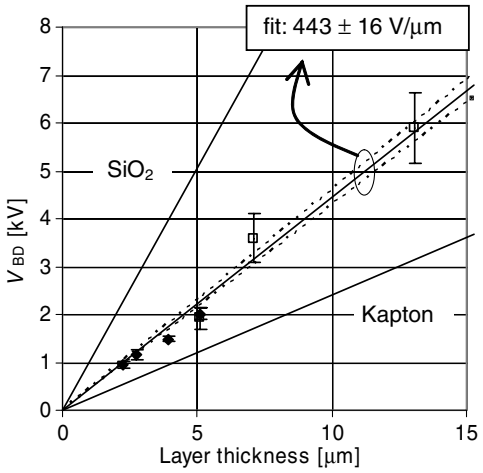

Figure 9. V_{BD} of SU-8 plotted versus thickness; the dielectric strength of SU-8 and of two other materials is indicated with drawn lines.

side of the top electrode to the nearest point of the other electrode. Current flows across the surface of the SU-8, which does not usually lead to an immediate short. If the high current is sustained for some time, a very large part of the top electrode will be consumed, as shown in figure 8(*c*).

Some device designs feature a shorter isolation width. The device in figure 8(*d*) has an isolation width of only 0.2 mm. The entire device, top electrode, SU-8 overlap and bottom electrode can be seen. In these devices, breakdown is almost exclusively edge breakdown and it usually results in a rapid creation of a black deposit across the isolation overlap that effectively shorts the two electrodes; this can be seen in figure 8(*e*).

The breakdown voltage (V_{BD}) is defined as the highest voltage that can be applied before the current rises uncontrollably. The current is always ramped up slowly.

Figure 9 shows V_{BD} (average and 1σ spread) measured on devices with varying dielectric thickness. The first four points (diamonds) were measured on the same devices as used for the leakage current measurements. The open squares represent additional data points with larger SU-8 thickness. These are measured with a simpler set-up (as outlined above). With a linear fit through all data points, we determine that the dielectric strength of SU-8 is 443 ± 16 V μm^{-1} or 4.43 ± 0.16 MV cm^{-1} (1σ) for SU-8. This value is independent of whether or not an additional hard-bake of the SU-8 is performed; this is experimentally verified for a hard-bake temperature of 150 °C.

For reference the dielectric strength of two other materials is also indicated in figure 9. The dielectric strength of SU-8 (4.4 MV cm^{-1}) is higher than that of Kapton (2.4 MV cm^{-1}), as well as that of other similar construction materials such as Parylene-N (2.8 MV cm^{-1}) and PEEK (0.2 MV cm^{-1}). The values are obtained from datasheets of commercial vendors of these products. Kapton is a polyimide material that is very often used for gaseous detectors (referenced in [13]) such as GEM foils. The device presented in [13] makes use of SU-8 to build a novel gaseous radiation detector. For this detector (and for GEM foils), the DS is required to be >1 MV cm^{-1}. The performance of SU-8 exceeds this requirement easily. The value we obtain is also significantly higher than the value of 1.1–1.2 MV cm^{-1} specified in the datasheet for SU-8 2000/3000 [2].

The dielectric strength of thermally grown silicon oxide (SiO_2, 8–9 MV cm^{-1} for thick layers) is also indicated in the graph. The dielectric strength of SiO_2 is one of the highest achievable and it certainly has the highest dielectric strength found among materials used in conventional micro-electronics. The dielectric strength of SU-8 reaches as much as 50% of that of SiO_2.

Figure 10 shows a cumulative histogram of the breakdown distribution for various layers. For the thinner layers the breakdown occurs almost exclusively in the center of the device (situation B, shown in figure 8(*b*)). We consider this the intrinsic breakdown of the dielectric material. For the thicker layers, the breakdown voltage becomes so high that we more often observe a preliminary breakdown at the perimeter of the device (situation C). This results in a severe erosion of the top electrode as illustrated in the micrograph in figure 8(*c*).

From this and other results mentioned above, we conclude that edge termination of HV-biased SU-8 structures is critical. A large enough overlap is required to prevent destructive discharges along the surface. The devices shown in figure 10 have an overlap distance from 0.2 mm to 5 mm. The thinnest devices show an intrinsic (bulk) breakdown of around 1 kV. For these devices, the smallest overlap of 0.2 mm is sufficient to prevent early (surface) breakdown. For the thicker devices, we see a larger variation in breakdown voltage and corresponding mode. These devices require a larger isolation width to consistently observe intrinsic bulk breakdown. From 2 mm onward, breakdown values become stable.

We have performed our measurements in an N_2 ambient. Surface breakdown will be strongly suppressed in the Ne-, Ar- or He-based gas mixtures typically used in the gaseous radiation detectors [19]. Specifically, the additional molecular gas fraction that is added to these mixtures, such as CH_4, isobutane or DME, increases the breakdown strength greatly.

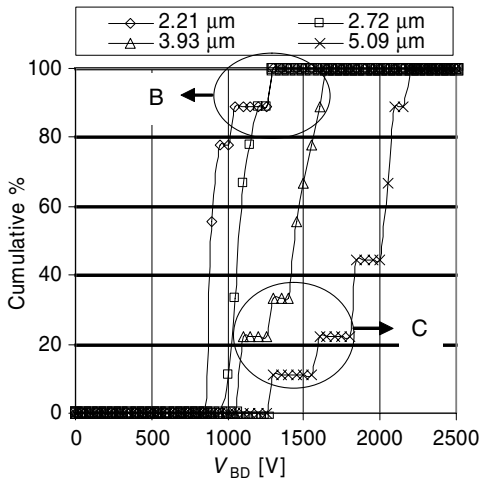

Figure 10. Probability plot showing different breakdown modes: intrinsic BD in the middle (B) and pre-mature BD on the edge (C) of the device.

Therefore, we have not investigated surface breakdown effects further.

4. Conclusions

We have presented measurements on the dielectric behavior of SU-8 under low- and high-voltage bias conditions.

The leakage through SU-8 is found to be a reliable and repeatable smooth function of voltage and, at least for the very large device sizes used here, the current scales well with the contact area. The leakage current density through the dielectric layer scales logarithmically with the square root of the bias field strength ($E^{1/2}$), and the logarithm of J/T^2 is inversely proportional to the temperature. This indicates that thermionic emission from the Al electrode causes the leakage current.

The dielectric strength of SU-8 is 4.43 ± 0.16 MV cm^{-1}. This value is remarkably high for a polymer material, and it is more than sufficient for the requirements of gaseous radiation detectors.

A suitable edge termination is essential for SU-8 structures if they are subjected to high bias voltages. Due to the high intrinsic dielectric strength of the material, a large overlap of the dielectric with respect to the electrode is needed.

Acknowledgments

The authors acknowledge the help of V M Blanco Carballo and F van Rossem. This work was funded by Dutch Technology Foundation STW (project TEL-6630).

References

[1] Lorenz H, Despont M, Fahrnl N, LaBianca N, Renaud P and Vettiger P 1997 SU-8: a low-cost negative resist for MEMS *J. Micromech. Microeng.* **7** 121–4
[2] http://www.microchem.com/products/su_eight.htm
[3] Shaw J M, Gelorme J D, LaBianca N C, Conley W E and Holmes S J 1997 Negative photoresists for optical lithography *IBM J. Res. Dev.* **41** 81
[4] Dentinger P M, Clift W M and Goods S H 2002 Removal of SU-8 photoresist for thick film applications *Microelectron. Eng.* **61–62** 993–1000
[5] Kim S J, Yang H, Kim K, Lim Y T and Pyo H B 2006 Study of SU-8 to make a Ni master-mold: adhesion, sidewall profile, and removal *Electrophoresis* **27** 3284–96
[6] Lee C H and Jiang K 2008 Fabrication of thick electroforming micro mould using a KMPR negative tone photoresist *J. Micromech. Microeng.* **18** 055032–8
[7] Sato H, Matsumura H, Keino H S and Shoji S 2006 An all SU-8 microfluidic chip with built-in 3D fine microstructures *J. Micromech. Microeng.* **16** 2318–22
[8] del Campo A and Greiner C 2007 SU-8: a photoresist for high-aspect-ratio and 3D submicron lithography *J. Micromech. Microeng.* **17** R81–95
[9] Lorenz H, Laudon M and Renaud P 1998 Mechanical characterization of a new high-aspect-ratio near UV-photoresist *Microelectron. Eng.* **41–42** 371–4
[10] Conradie E H and Moore D F 2002 SU-8 thick photoresist processing as a functional material for MEMS applications *J. Micromech. Microeng.* **12** 368–74
[11] Yu H, Balogun O, Li B, Murray T W and Zhang X 2006 Fabrication of three-dimensional microstructures based on single-layered SU-8 for lab-on-chip applications *Sensors Actuators* A **127** 228–34
[12] Key M J, Cindro V and Lozano M 2004 On the radiation tolerance of SU-8, a new material for gaseous microstructure radiation detector fabrication *Radiat. Phys. Chem.* **71** 1003–7
[13] Blanco Carballo V M, Chefdeville M, van der Graaf H, Melai J, Salm C, Schmitz J and Timmermans J 2008 A radiation imaging detector made by postprocessing a standard CMOS chip *IEEE Electron Dev. Lett.* **29** 585–7
[14] Melai J, Salm C, Smits S M, Blanco Carballo V M, Schmitz J and Hageluken B 2007 *Proc. of the SAFE Workshop (Veldhoven, the Netherlands)* (Veldhoven: STW) pp 529–34
[15] Bystrova S, Luttge R and van den Berg A 2007 Study of crack formation in high-aspect ratio SU-8 structures on silicon *Microelectron. Eng.* **84** 1113–6
[16] Pan T, Baldi A and Ziaie B 2007 Remotely adjustable check-valves with an electrochemical release mechanism for implantable biomedical microsystems *Biomed. Microdevices* **9** 385–94
[17] Salm C, Blanco Carballo V M, Melai J and Schmitz J 2008 Reliability aspects of a radiation detector fabricated by post-processing a standard CMOS chip *Microelectron. Reliab.* **48** 1139–43
[18] Sze S M and Kwok K N G 2007 *Physics of Semiconductor Devices* 3rd edn (Hoboken, NJ: Wiley-Interscience) pp 157, 227–8
[19] Sauli F 1977 *CERN Yellow Report 77-09* p 46–8