Strain and Conduction-Band Offset in Narrow n-type FinFETs

T. van Hemert, *Student Member, IEEE*, B. Kaleli, R. J. E. Hueting, *Senior Member, IEEE*, D. Esseni, *Fellow, IEEE*, M. J. H. van Dal, and J. Schmitz, *Senior Member, IEEE*

***Abstract*—In this paper, we compare measurements of the conduction-band (CB) offset in [110]- and [010]-oriented narrow n-type FinFETs with a model taking into account both strain and quantum confinement. We estimate the complete strain tensor for the scarce strain measurement points available with finite-element-method simulations of the thermal expansion effect. We found an inhomogeneous compressive strain that increases for smaller fin widths. The experimental CB offset is extracted from temperature-dependent transfer characteristics. The results show a lowering of the CB edge up to 40 meV for fin widths down to 5 nm. These experimental observations compare well with the model, and hence, the band offset can be explained by both quantum confinement and strain.**

***Index Terms*—Double-gate FETs, leakage current, quantum wells, semiconductor device measurement, strain, stress, thermal expansion.**

I. Introduction

ONE of the reasons that multiple-gate architectures, such as the fin-shaped field-effect transistor (FinFET), are becoming the standard in integrated circuits [1] is their improved electrostatic behavior. The multiple gates result in an enhanced control of the charge in the channel. When designed properly, the gate can deplete the entire silicon (Si) fin. This enables volume inversion, where the inversion layer extends throughout the entire body, resulting in a steeper subthreshold swing (SS) compared with a single-gate bulk metal–oxide semiconductor FET (MOSFET) [2] with equal channel length. Strained Si layers have been incorporated into the MOSFET to increase both carrier mobility and injection velocity [3]–[6]. The strain is generally not uniformly distributed throughout the semiconductor. Process simulations have revealed that the strain depends on the fin dimensions and penetrates a certain depth into the Si [7]. Holographic interferometry measurements [8] also indicate that the strain depends on the fin width. Hence, we expect that the amount of strain depends on the device geometry. Strain implies deformation of the crystal lattice and so results in an offset of the conduction-band (CB) valleys [9]. For very small dimensioned FinFETs, the CB splits into discrete energy levels, the so-called subbands. This effect is termed quantum confinement (QC) and appears as an upward shift in the CB levels and a downward shift of the valence-band levels.

Manuscript received September 10, 2012; revised November 1, 2012, December 18, 2012, and January 10, 2013; accepted January 14, 2013. Date of current version February 20, 2013. This work is supported by NanoNextNL, a micro and nanotechnology programme of the Dutch ministry of economic affairs, agriculture and innovation (EL&I) and 130 partners. The Dutch Technology Foundation STW, applied science division of NWO and the Technology Program of the Ministry of Economic Affairs supported parts of this research. The review of this paper was arranged by Editor A. Schenk.

T. van Hemert, B. Kaleli, R. J. E. Hueting, and J. Schmitz are with the MESA+ Institute for Nanotechnology, University of Twente, 7522 Enschede, The Netherlands (e-mail: t.vanhemert@utwente.nl; b.kaleli@utwente.nl; r.j.e.hueting@utwente.nl; j.schmitz@utwente.nl).

D. Esseni is with the Department of Electrical Engineering, Mechanical Engineering and Management, University of Udine, 33100 Udine, Italy (e-mail: esseni@uniud.it).

M. J. H. van Dal is with the Advanced Device Technology Division, TSMC Europe, 3001 Leuven, Belgium (e-mail: mark_van_dal@tsmc.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2241765

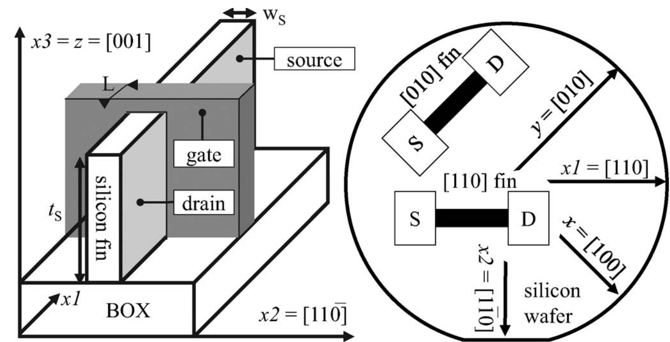

Fig. 1. Schematic view of the [110] FinFETs and the orientation of the fins on the Si wafer. The 65-nm-high fin is on top of a 145-nm-thick BOX layer. The orientation of the device coordinate system $[x1, x2, x3]$ is shown relative to the crystal coordinate system $[x, y, z]$. w_S is the fin width.

In this paper, we aim to measure the CB offset for very narrow n-type Si FinFETs. Since both QC and strain have an influence on the CB offset, we estimate the strain values for various fin dimensions. In the following sections, we present simulations to interpret the strain measurements, a theory to explain the CB offset, the measurement methodology, the experimental results, and finally, the conclusions.

II. Strain Modeling

Fig. 1 shows a schematic representation of the FinFET. The fin has source and drain connections, and the channel region is surrounded by the dielectric and the gate. The crystal $[x, y, z]$ and device $[x1, x2, x3]$ coordinate systems are also shown. We investigated two differently oriented FinFETs. The first has a [110] channel transport direction and $(1\bar{1}0)$-oriented sidewalls. The second has [010] as transport direction and (100)-oriented sidewalls. The Si fin is covered by a stack of silicon dioxide (SiO_2) and high-k hafnium silicate (HfSiO). The exact composition is $Hf_{0.4}Si_{0.6}O$. On top of these dielectrics, the titanium nitride (TiN) and poly silicon (Poly-Si) gate layers have been

0018-9383/$31.00 © 2013 IEEE

TABLE I
MECHANICAL PARAMETERS OF THE ISOTROPIC MATERIALS, t IS THE THICKNESS, c IS THE STIFFNESS, ρ IS THE POISSON RATIO, CTE IS THE TEMPERATURE EXPANSION COEFFICIENT, AND $\epsilon_{\rm lim}$ IS THE ELASTIC LIMIT. HfSiO IS NOT A THOROUGHLY INVESTIGATED MATERIAL, AND AS A RESULT, SOME PARAMETERS HAD TO BE TAKEN FROM REFERENCES WITH COMPARABLE MATERIALS. IN [12], THE DATA WERE INTERPOLATED FROM COMPARABLE COMPOUNDS. IN [13], ρ WAS CALCULATED AND MEASURED FOR $HfSiO_4$. IN [14], THE CTE WAS MEASURED FOR $HfSiO_4$

	t [nm]	c [GPa]	ρ [-]	CTE [10^{-6}/K]	$\epsilon_{\rm lim}$ [%]
Poly-Si	100	160 [15]	0.22 [16]	6.4 [15]	2 [16]
TiN	7	640 [17]	0.25 [17]	9.4 [8]	5 [18]
HfSiO	1.7	110 [12]	0.2 [13]	3.6 [14]	-
SiO_2	1	57 [19]	0.20 [19]	0.6 [20]	2 [21]
Si	65	169		3.5 [15]	3 [22]

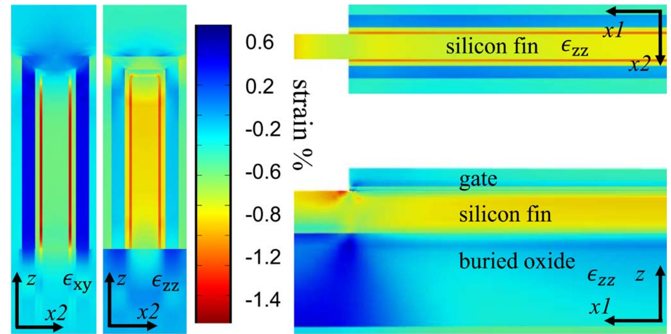

Fig. 2. Cross-sectional views of the fin in plane with the device coordinate system $[x1, x2, x3]$ through the center of the FinFET in Fig. 1, showing the simulated strain at room temperature for a 10-nm-wide fin. Note that the device coordinate axes are indicated.

deposited. During the front-end-of-line device integration of the FinFETs used in this work [10], the gate undergoes heat treatments as high as 1370 K, inducing the plastic relaxation of the Si channel and the TiN gate. Upon cooling, a stress field is built up in the channel due to the large difference in the coefficient of thermal expansion (CTE) of Si and TiN.

We investigated the plastic relaxation of the gate stack and the subsequent stress build-up by implementing a multiphysics 3-D finite-element-method (FEM) simulation [11] of the thermal expansion. We simulated the structure as shown in Fig. 1. To manage the computational load of the model, we assumed the following. We neglected the Si substrate below the BOX and applied fixed boundaries to the bottom of the BOX layer to mimic the stiff Si substrate. We verified that the results are essentially insensitive to variations of the BOX thickness, and thus, simulating the complete substrate is not imperative. We simulated various degrees of corner rounding and found that this hardly affects the final result and that rounding can be neglected. The fins always form a group of five parallel fins, with a pitch of 200 nm. This can be simplified by simulating only one of the five fins and applying symmetric boundary conditions to the sides. The step coverage of the Poly-Si has not been taken into account; however, we verified that the results are insensitive to thickness variations, suggesting that the step coverage is not relevant. To mimic the behavior of the relatively large and, hence, stiff source/drain connections, the Si fin was simulated 100 nm longer than the region overlapped by the gate and symmetric boundary conditions were applied to the source/drain sides. All other boundaries were free to move.

The parameters for the FEM simulations are summarized in Table I. An anisotropic model was used for the Si fin, while the other materials were modeled isotropically. Since HfSiO is a relatively unknown material, its properties are not determined with good precision. Furthermore, the literature references for the mechanical properties are obtained from bulk test structures, whereas our structures are in the nanometer scale, and hence, the properties may differ. The induced strain depends strongly, but not exclusively, on the CTE. For example, a material with low stiffness is easier to deform and, thus, will receive a higher strain. In Fig. 2, the simulated strain for a 10-nm-wide fin is shown, indicating that the strain is not uniform in the Si fin. First, the BOX is not a stressor; hence, the bottom of the fin receives a lower strain. Second, the gate deforms the fin surface in plane with the dielectric. At the top, this is perpendicular to the z-axis, and thus, the top of the Si fin receives a lower strain $\epsilon_{\rm zz}$. Third, the dielectric layers surrounding the Si fin, being SiO_2 and HfSiO, have a relatively low stiffness (see Table I); therefore, they deform much more than the Si fin under stress. This explains the high strain levels in the dielectric. From holographic interferometry measurements [8], we expected a strain along the z-axis of $\epsilon_{\rm zz} = -0.8\%$, which is, in fact, comparable with the volume average of the simulated strain.

In the simulation, elastic deformation, i.e., a linear relation between the stress and strain, has been assumed. This holds as long as the strain is well below the elastic limit of the materials. These limits are shown in Table I. To our knowledge, the elastic limit for HfSiO has not yet been published. For the other materials, we found maximum strain levels well below this limit. In this paper, we aim to model the band offset as a function of the strain and fin dimensions. The simulations show a slightly nonuniform strain. We calculated the resultant nonuniform current and found a 1% change in the current ratio between a thick and narrow fin. This effect can be neglected, and uniform strain can be assumed. Hence, in the remainder of this paper, when we mention strain, we refer to the average strain in the Si fin surrounded by the gate. As mentioned before, the strain is a result of a difference between the CTEs of materials. Hence, it can be insightful to simulate the strain as a function of the temperature. This is shown in Fig. 3(a). The figure also shows the electrical measurement temperature range, revealing that the strain varies with temperature in our experiments. Nevertheless, this 0.1% change is small compared with the overall strain of -0.6%. Also, the fin-width dependence of the strain, after the cool-down step inducing strain, has been investigated, as shown in Fig. 3(b).

The simulated strain is in the same order as the holographic measurements [8] but shows weaker fin-width dependence. Therefore, we use these results only to estimate nonmeasured strain components and the strain for other fin widths. Extrapolating the strain in Fig. 3(b) for infinite fin widths results in close-to-zero strain. On the other hand, zero fin width should give a certain maximum. This behavior can be fitted well with an exponential function. In our previous work [23], we assumed a linear dependence; however, a linear function cannot fit the behavior for infinitely small or large fin widths. The

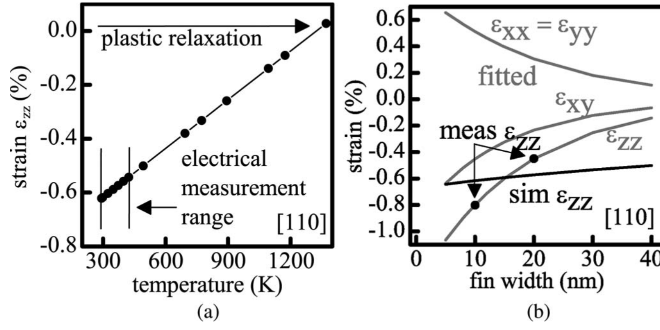

Fig. 3. (a) Simulated strain in a 10-nm-wide fin as a function of the temperature. The collection of points around room temperature show the electrical measurement range. (b) (Dots) Measured, (black line) simulated, and (gray lines) fitted dependence of the strain on the fin width after the cool-down step at room temperature.

holographic interferometry measurements [8] are available only for two fin widths; however, three are needed to fit an exponential function. Therefore, we add a third point to the measurements with $w_S = 1000$ nm and $\epsilon_{\rm zz} = 0$. To calculate the effect on band alignment and quantum confinement, the complete six-component strain tensor is required for all fin widths. To estimate this tensor, we extract the ratio of the components of the strain tensor, for instance, $\epsilon_{\rm zz}/\epsilon_{\rm xy}$, from the simulations. These ratios multiplied by the measured and extrapolated data for $\epsilon_{\rm zz}$ give a good approximation for the complete strain tensor for all considered fin widths. This approach can be justified by all stress–strain relations being linear. This procedure has been followed for both [110]- and [010]-oriented fins.

III. Band Offset

It has been reported that the band minima in a semiconductor depend on strain [9], [24], [25]. Furthermore, for narrow fin widths, QC needs to be taken into account. With this purpose, the Si body is viewed as a square energy well and the energy levels of the subbands for electrons is calculated from the Schrödinger equation. This is a defendable approximation in the subthreshold regime that we are mostly interested in (see Section IV). The offset of the valleys along the x-, y-, and z-axes is the superposition of the offsets due to strain [26] and QC [27] and can be written as

$$E_{k,n} = \Xi_d(\epsilon_{\rm xx}+\epsilon_{\rm yy}+\epsilon_{\rm zz})+\Xi_u\epsilon_{\rm kk}+E^{\rm shear}_{\Delta_k}+\frac{\hbar^2}{2m^*_{Q,k}}\frac{n^2\pi^2}{w_S^2}$$

$$E^{\rm shear}_{\Delta_z} = -\frac{\Theta}{4\kappa^2}\epsilon^2_{\rm xy} \qquad (1)$$

where $k = x, y, z$ is the valley index and n is the subband index. Ξ_d and Ξ_u are the deformation potentials, and Θ, η, and κ are the model parameters from [25], whose numerical values are summarized in Table II. $\epsilon_{\rm yz}$ and $\epsilon_{\rm xz}$ are zero; therefore, $E^{\rm shear}_{\Delta k}$ is nonzero for the $k = z$ valley only. Hence, it is not necessary to show the shear-strain dependence for the other valleys. For the same reason, the shear-strain dependence of the quantization effective mass $m^*_{Q,k}$ is only shown for the z-valley in the [110]-oriented fins.

TABLE II
PARAMETERS USED FOR BAND DEFORMATION CALCULATION FROM [25]. THE QUANTIZATION MASSES [27] $m^*_{Q,k}$ ARE EXPRESSED IN THE ELECTRON REST MASS $[m_0]$

Ξ_d[eV]	Ξ_u[eV]	Θ	η	κ
1.1	9.29	0.53	-0.809	0.189

orient.	side.	$m^*_{Q,x}$	$m^*_{Q,y}$	$m^*_{Q,z}$
[110]	$(1\bar{1}0)$	0.315	0.315	$0.19(1+\eta\epsilon_{\rm xy}/\kappa)^{-1}$
[010]	(100)	0.916	0.19	0.19

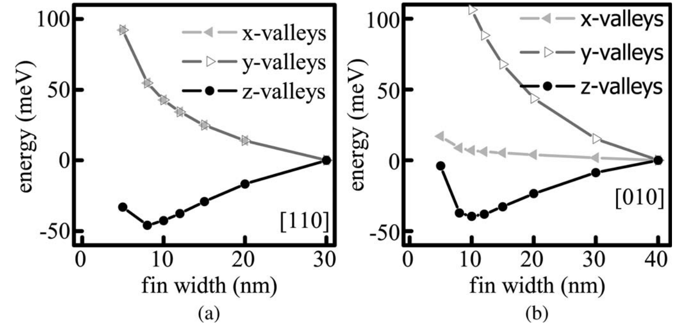

Fig. 4. Calculated offset of the CB valleys due to strain and QC. (a) For the [110]-oriented fins and (b) the [010]-oriented fins.

In Fig. 4, the energy offset for the lowest subbands of the different CB valleys are shown as a function of the fin width. To ease the comparison with the results presented further in this paper, the 30-nm fin width is taken as a reference for the [110]-oriented fins and the 40-nm fin width is taken for the [010]-oriented fins. The strain leads to a splitting of the CB valleys. With compressive strain $\epsilon_{\rm zz}$, the z-valleys move down and the other valleys move up. For [110]-oriented devices, the strain along the $x2$- and $x1$-axes is shear, translating in an equal offset of both x- and y-valleys. In the [010] channel, instead, the strain displaces the valleys differently. For both cases, the strong compressive z-axis strain $\epsilon_{\rm zz}$ moves down the z-valley. Most of the electrons occupy the lowest available energy levels. Therefore, a measurement of the CB offset effectively probes the z-valleys.

In a narrow high-aspect-ratio undoped FinFET, the charge density in subthreshold is fairly uniform in the fin width [28]. The influence of the substrate bias can be neglected as the body factor [29] is close to 1. The electron gas is nondegenerate, and hence, the subthreshold current is given by [30]

$$I_D = N\frac{t_S\mu q u_t}{L}\left[1-\exp\frac{-V_{\rm DS}}{u_t}\right]\exp\left[\frac{\chi_{\rm Si}-\phi_m+V_{\rm GS}}{u_t}\right] \cdot\frac{k_BT}{\pi\hbar^2}\sum_{k,n}m^*_{d,k}\left[\exp-\frac{E_{k,n}}{k_BT}\right] \qquad (2)$$

where N is the number of parallel fins, k_B is the Boltzmann constant, $t_{\rm S}$ is the fin height, μ is the electron mobility, $\chi_{\rm Si}$ is the Si electron affinity, ϕ_m is the metal work function, and $m^*_{d,k}$ is the density-of-states effective mass. If, as assumed earlier, the lowest subband, in our case $k = z$ and $n = 1$, carries most of the current, then the subthreshold current ratio of devices with different fin widths yields

$$\eta_{\rm rat} = \frac{I_{\rm meas}}{I_{\rm ref}} \propto e^{\frac{\Delta E_{z,1}}{k_BT}} \qquad (3)$$

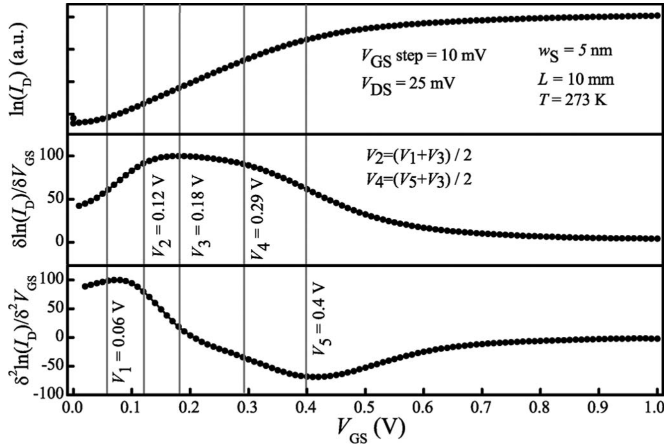

Fig. 5. $\ln(I_D)$ and smoothed derivatives as a function of the gate voltage, which are necessary to define the subthreshold region of the graph. For convenience sake, normalized values are used for the derivatives. $\delta \ln(I_D)/\delta V_{\mathrm{GS}}$ peak is located at V_3, and $\delta^2 \ln(I_D)/\delta^2 V_{\mathrm{GS}}$ has extreme values at V_1 and V_5.

where I_{meas} and I_{ref} are the subthreshold currents obtained from a measured and a reference device, respectively. The temperature derivative of η_{rat} gives the CB offset between the thick and thin devices, in our case $\Delta E_{z,1}$. We assume that χ_{Si}, ϕ_m, and ϵ are constant in the measured temperature range. We expect that the temperature dependence of the low-field mobility is equal for the measured fin widths [31] and, hence, does not influence the results. The same holds for the oxide thickness and the density-of-states effective mass.

IV. Experimental Technique

The FinFETs were obtained from the NXP-TSMC Research Center [10]. The temperature-dependent transfer characteristics were recorded with a Keithley 4200 semiconductor parameter analyzer and a Cascade probe station.

The temperature dependence of the ratio of the subthreshold current densities is used to calculate the CB offset [30]. The obtained results are valid as long as (2) holds, and this can be verified from the temperature dependence of the extracted SS, which clearly should be almost the same for the considered fin widths in the considered temperature range. Moreover, the devices should not show any short-channel effect, which is, in fact, the case for the long devices used in the measurements.

For further analysis, it is convenient to have a definition for the subthreshold region where (2) is valid. Fig. 5 shows $\ln(I_D)$. The peak of $\partial \ln(I_D)/\partial V_{\mathrm{GS}}$ at V_3 is in the center of the region. The $\partial^2 \ln(I_D)/\partial^2 V_{\mathrm{GS}}$ maximum at V_1 gives the start of the subthreshold region. Equivalently, the minimum indicates the end at V_5. Similar methods have been proposed to obtain the threshold voltage (V_T) at V_5 [32] or to characterize the hump effect [33]. We define the lower and upper limits of the subthreshold region at V_2 and V_4, respectively. An exponential function is fitted to the data in the subthreshold region to eliminate noise. The slope of the fit gives the average SS. From the fit, the CB offset was extracted with the method described in Section III.

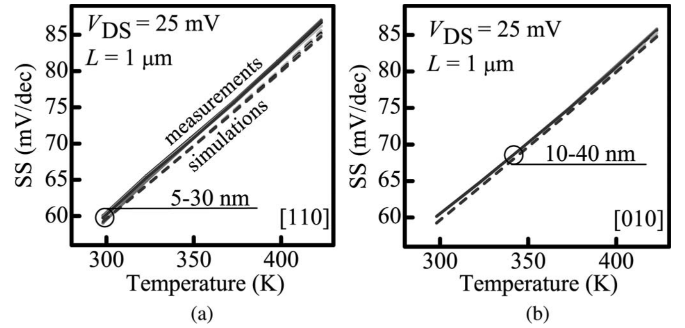

Fig. 6. Extracted SS from (lines) both measurements and (dashed lines) TCAD simulations. (a) For the [110]-oriented fins. For 5–30-nm fin widths, the SS shows linear temperature dependence and small variation. Hence, the CB offset can be calculated from the subthreshold characteristics. (b) For the [010]-oriented fins. Here, the 10–40-nm fin widths show suitable SS.

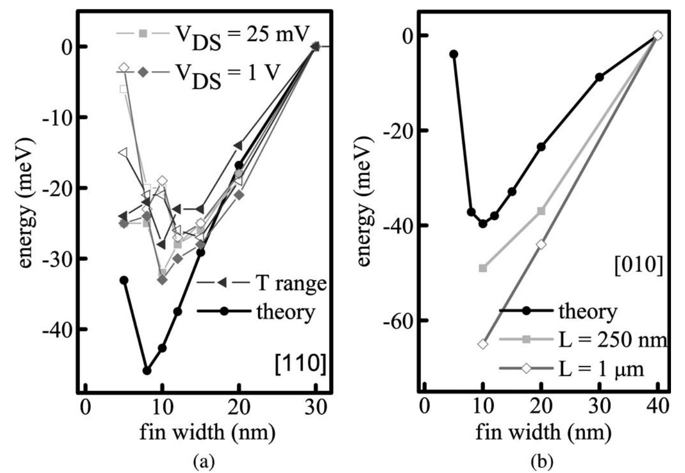

Fig. 7. Extracted CB offset compared with the values according to the theory of the z-valleys obtained from Fig. 4. The open symbols are for 1-μm-long fins. (a) For the [110]-oriented fins, where also results obtained with $V_{\mathrm{DS}} = 1$ V instead of 25 mV, indicated by V_{DS}, and results obtained with a smaller temperature range, from 293 K instead of 233 K indicated by T, are shown. Closed symbols are for 10-μm-long fins. (b) For the [110]-oriented fins. Closed symbols are for 250-nm-long fins.

V. Band Offset Results

The subthreshold region of measured transfer characteristics was identified using the method shown in Fig. 5. The extracted values for the SS are shown in Fig. 6. According to (2), the SS of the considered fin widths should be the same. Clearly, this is the case for the fin widths shown in the figure. Hence, we can use 30- and 40-nm-wide fins as reference for the [110] and [010] orientations, respectively. In addition, the SS extracted from simulations [34], including band offset due to strain, and the quantization effects using the density gradient model [35], [36] are shown. The results are in a good agreement with the measurements.

We measure a current obtained from an ensemble of electrons, and any extracted parameter thus represents an average or effective value. Using (3), the band offsets were extracted and are shown in Fig. 7. The results reveal a lowering of the CB for smaller fin widths. In addition, for the [110] orientation, we have data for fin widths below 10 nm, where the CB starts to shift up. For comparison, the calculated offset of the lowest CB valleys, in our case, the z-valleys, is also shown. Both theory

and measurements show the same qualitative dependence on fin width. Additional measurements were also done with an alternate temperature range and drain–source bias (V_{DS}). These show no qualitative difference. Therefore, the general observation is that narrowing the fins increases the strain, as predicted by FEM simulation, and shifts the z-valleys downward. Fin widths below 10 nm were available for the [110] orientation only, and here, quantization needs to be taken into account. This effect counteracts the strain and shifts the Δ_2 valleys upward.

VI. Conclusion

In this paper, we have investigated the CB offset in narrow FinFETs. This offset is partly caused by strain. Using multiphysics simulations, we estimated the ratio of the different strain components. Applying this ratio to actual measurements of the most important strain component yielded insight into the complete strain tensor. Finally, the strain for different fin widths was estimated using inter- and extrapolation.

The CB offset was calculated as a function of the fin width and strain. The obtained results for both [110]- and [010]-oriented Si fins are well comparable with the measured CB offsets. The CB offset can be explained by the superposition of two physical effects: (1) an increase in compressive strain in the fin height direction for narrower fins moving the CB z-valleys downward and (2) QC for fin widths below 10 nm, separating the energy levels available to electrons and moving the CB valleys upward.

Acknowledgment

The authors would like to thank S. Smits for his help in the measurement laboratory, F. Wiggers for assisting in some parts of the measurements, and A. Paternoster, who is with the Applied Mechanics Department, University of Twente, for helping in the multiphysics FEM simulations.

References

[1] International Technology Roadmap for Semiconductors. [Online]. Available: www.itrs.net

[2] R.-H. Yan, A. Ourmazd, and K. Lee, “Scaling the Si MOSFET: From bulk to SOI to bulk,” *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.

[3] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam, “Innovative materials, devices, and CMOS technologies for low-power mobile multimedia,” *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 96–130, Jan. 2008.

[4] S. Takagi, T. Iisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, “Carrier-transport-enhanced channel CMOS for improved power consumption and performance,” *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 21–39, Jan. 2008.

[5] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, and D. A. Antoniadis, “Strained silicon MOSFET technology,” in *IEDM Tech. Dig.*, Dec. 2002, pp. 23–26.

[6] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, “Uniaxial-process-induced strained-Si: Extending the CMOS roadmap,” *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, May 2006.

[7] C. Y. Kang, J.-W. Yang, J. Oh, R. Choi, Y. J. Suh, H. Floresca, J. Kim, M. Kim, B. H. Lee, H.-H. Tseng, and R. Jammy, “Effects of film stress modulation using TiN metal gate on stress engineering and its impact on device characteristics in metal gate/high-k dielectric SOI FinFETs,” *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 487–490, May 2008.

[8] F. Conzatti, N. Serra, D. Esseni, M. De Michielis, A. Paussa, P. Palestri, L. Selmi, S. M. Thomas, T. E. Whall, D. Leadley, E. H. C. Parker, L. Witters, M. J. Hytch, E. Snoeck, T. J. Wang, W. C. Lee, G. Doornbos, G. Vellianitis, M. J. H. van Dal, and R. J. P. Lander, “Investigation of strain engineering in FinFETs comprising experimental analysis and numerical simulations,” *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1583–1593, Jun. 2011.

[9] G. L. Bir and G. E. Pikus, *Symmetry and Strain-Induced Effects in Semiconductors*. Jerusalem, Israel: Israel Program Sci. Translations, 1974.

[10] M. J. H. van Dal, N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. J. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavyy, R. Rooyackers, M. Kaiser, R. G. R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, and R. J. P. Lander, “Highly manufacturable FinFETs with sub-10nm fin width and high aspect ratio fabricated with immersion lithography,” in *VLSI Symp. Tech. Dig.*, Jun. 2007, pp. 110–111.

[11] *Comsol MultiPhysics*, COMSOL, Inc., Palo Alto, CA, USA, 2010.

[12] D. K. Venkatachalam, J. E. Bradby, M. N. Saleh, S. Ruffell, and R. G. Elliman, “Nanomechanical properties of sputter-deposited HfO_2 and $Hf_xSi_{x-1}O_2$ thin films,” *J. Appl. Phys.*, vol. 110, no. 4, pp. 043527-1–043527-5, Aug. 2011. [Online]. Available: http://link.aip.org/link/?JAP/110/043527/1

[13] Q.-J. Liu, Z.-T. Liu, L.-P. Feng, H. Tian, and W. Zeng, “First-principles investigations on structural, elastic, electronic, and optical properties of tetragonal $HfSiO_4$,” *Braz. J. Phys.*, vol. 42, no. 1/2, pp. 20–27, Apr. 2012. [Online]. Available: http://dx.doi.org/10.1007/s13538-012-0067-0

[14] H. Li, S. Zhou, and S. Zhang, “The relationship between the thermal expansions and structures of ABO_4 oxides,” *J. Solid State Chem.*, vol. 180, no. 2, pp. 589–595, Feb. 2007. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0022459606006232

[15] C.-S. Oh and W. Sharpe, Jr., “Techniques for measuring thermal expansion and creep of polysilicon,” *Sens. Actuators A, Phys.*, vol. 112, no. 1, pp. 66–73, Apr. 2004. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0924424703007143

[16] W. N. Sharpe, Jr., B. Yuan, R. Vaidyanathan, and R. L. Edwards, “Measurements of Young’s modulus, Poisson’s ratio, and tensile strength of polysilicon,” in *Proc. MEMS*, Jan. 1997, pp. 424–429.

[17] A. J. Perry, “A contribution to the study of Poisson’s ratios and elastic constants of TiN, ZrN and HfN,” *Thin Solid Films*, vol. 193/194, pt. 1, pp. 463–471, 1990.

[18] B. D. Fulcher, X. Y. Cui, B. Delley, and C. Stampfl, “Hardness analysis of cubic metal mononitrides from first principles,” *Phys. Rev. B*, vol. 85, no. 18, pp. 184106-1–184106-9, May 2012. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.85.184106

[19] H.-C. Tsai and W. Fang, “Determining the Poisson’s ratio of thin film materials using resonant method,” *Sens. Actuators A, Phys.*, vol. 103, no. 3, pp. 377–383, Feb. 2003.

[20] A. K. Sinha, H. J. Levinstein, and T. E. Smith, “Thermal stresses and cracking resistance of dielectric films (SiN, Si_3N_4, and SiO_2) on Si substrates,” *J. Appl. Phys.*, vol. 49, no. 4, pp. 2423–2426, Apr. 1978. [Online]. Available: http://link.aip.org/link/?JAP/49/2423/1

[21] L. A. Davis, “Fracture toughnesses of metallic glasses,” *Metallurg. Trans. A*, vol. 10, no. 2, pp. 235–240, Feb. 1979. [Online]. Available: http://dx.doi.org/10.1007/BF02817633

[22] A. Howatson, P. Lund, and J. Todd, *Engineering Tables and Data*. London, U.K.: Chapman & Hall, 1991.

[23] T. van Hemert, B. Kaleli Kemaneci, R. J. E. Hueting, D. Esseni, M. J. H. van Dal, and J. Schmitz, “Extracting the conduction band offset in strained FinFETs from subthreshold-current measurements,” in *Proc. ESSDERC*, Sep. 2011, pp. 275–278.

[24] M. V. Fischetti and S. E. Laux, “Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys,” *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2252, Aug. 1996.

[25] E. Ungersboeck, S. Dhar, G. Karlowatz, V. Sverdlov, H. Kosina, and S. Selberherr, “The effect of general strain on the band structure and electron mobility of silicon,” *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2183–2190, Sep. 2007.

[26] N. Serra and D. Esseni, “Mobility enhancement in strained n-FinFETs: Basic insight and stress engineering,” *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 482–490, Feb. 2010.

[27] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS Transistors: Semi-Classical Modeling and Applications*. Cambridge, U.K.: Cambridge Univ. Press, 2011.

[28] Y. Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 245–247, May 2000.
[29] J. Frei, C. Johns, A. Vazquez, W. Xiong, C. Cleavelin, T. Schulz, N. Chaudhary, G. Gebara, J. Zaman, M. Gostkowski, K. Matthews, and J.-P. Colinge, "Body effect in tri- and pi-gate SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 12, pp. 813–815, Dec. 2004.
[30] J.-L. P. J. van der Steen, R. J. E. Hueting, and J. Schmitz, "Extracting energy band offsets on long-channel thin silicon-on-insulator MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1999–2007, Sep. 2009.
[31] J. Welser, J. L. Hoyt, S. Takagi, and J. F. Gibbons, "Strain dependence of the performance enhancement in strained-Si n-MOSFETs," in *IEDM Tech. Dig.*, Dec. 1994, pp. 373–376.
[32] D. Flandre, V. Kilchytska, and T. Rudenko, "g_m/i_d method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 930–932, Sep. 2010.
[33] H. Brut and R. Velghe, "Contribution to the characterization of the hump effect in MOSFET submicronic technologies," in *Proc. ICMTS*, Mar. 1999, pp. 188–193.
[34] *Sentaurus Device User Guide*, Synopsys, Inc., Mountain View, CA, USA, 2007.
[35] M. G. Ancona and H. F. Tiersten, "Macroscopic physics of the silicon inversion layer," *Phys. Rev. B*, vol. 35, no. 15, pp. 7959–7965, May 1987.
[36] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B*, vol. 39, no. 13, pp. 9536–9540, May 1989.

T. van Hemert (S'10) is currently working toward the Ph.D. degree at the University of Twente, Enschede, The Netherlands.

His research interests are strain in narrow FinFETs, piezoelectric resonators, and the combination of these two.

B. Kaleli received the B.Sc. and M.Sc. degrees in physics from the Middle East Technical University, in 2007 and 2009. She is currently working toward the Ph.D. degree at the University of Twente, Enschede, The Netherlands.

R. J. E. Hueting (S'94–M'98–SM'06) received the M.Sc. (*cum laude*) and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands.

He is with the University of Twente, Enschede, The Netherlands.

D. Esseni (S'98–M'00–SM'06–F'13) received the Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 1999.

Since 2005, he has been an Associate Professor with the University of Udine, Udine, Italy.

M. J. H. van Dal received the Ph.D. degree from Eindhoven University of Technology, Eindhoven, The Netherlands.

He is with the Advanced Device Technology Division, TSMC Europe, Leuven, Belgium.

J. Schmitz (M'02–SM'05) received the M.Sc. degree in physics (*cum laude*) and the Ph.D. degree from the University of Amsterdam, Amsterdam, The Netherlands, in 1990 and 1994, respectively.

He is currently a Full Professor with the University of Twente, Enschede, The Netherlands.