A Beamformer with Constant-Gm Vector Modulators and its Spatial Intermodulation Distortion

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Abstract

Spatial interference rejection in analog adaptive beamforming receivers can improve the distortion performance of the circuits following the beamforming network, but is susceptible to the non-linearity of the beamforming network itself. This paper presents an analysis of intermodulation product cancellation in analog active phased array receivers and verifies the distortion improvement in a 4-element adaptive beamforming receiver for low power applications in the 1.0 to 2.5 GHz frequency band. In this architecture, a constant-Gm vector modulator is proposed which produces an accurate equidistance square constellation, leading to a sliced frontend design that is duplicated for each antenna element. By moving the transconductances to RF, a four-fold reduction in power is achieved, while simultaneously providing input impedance matching. The 65-nm implementation consumes between 6.5 and 9 mW per antenna element, and shows a +1 to +20 dBm in-band, out-of-beam IIP3 due to intermodulation distortion reduction.

Index Terms

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analog beamforming, phased array, vector modulator, phase shifter, mixer, compression point, intercept point, switched-capacitor, interference nulling, spatial filtering, receiver

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I. Introduction

In beamforming phased-array receivers, the aim is to combine signals from multiple antennas such that sensitivity is improved and interferers are rejected in the spatial domain [1][2][3][4]. As is sketched schematically in Fig. 1, an interference cancelling beamforming receiver aims to maximize the received amplitude of the desired signals, while simultaneously minimizing the amplitude of one or multiple interferers. This is achieved by amplitude and phase weighting of the received signals from multiple antennas, usually spaced half the carrier wavelength apart, and summing into a common output signal [5].

Increasing the number of antennas improves the sensitivity at the expense of increased power consumption due to the multiple receiver frontends. A power efficient frontend is thus required, and the signals from the multiple frontends should be combined into a beamformed signal as early in the receiver chain as possible. On the other hand, interferers are suppressed by spatial filtering after the summing node, placing stringent linearity requirements on the receiver frontends. A tradeoff between low power consumption and distortion performance is therefore fundamental in the frontend design.

Good linearity can be achieved by adopting a passive switched-capacitor architecture for the antenna elements and summing node [6][7][8]. This comes at the cost of increased noise figure and clock power consumption. Recently, a gain-boosted mixer-first receiver frontend was proposed with impedance translated spatial notch at the antenna input and digital beamforming, greatly boosting out-of-band interferer rejection [9]. An analog beamformer with active pre-amplification

and passive mixer / phase shifter and summing node was presented earlier [10], and demonstrated a reduced power consumption at the expense of in-band, in-beam linearity performance.

In phased array receivers, the power consumption of an antenna element should be kept as low as possible, since the elements are duplicated several times to form the full array. This conflicts with the demand for good linearity of the receiver frontend to withstand interferers before spatial filtering occurs, which in general raises the power consumption. A combination of a low power beamforming architecture with adaptive interference nulling could potentially give the best trade-off. In this case the nulling beamforming algorithm has to operate on the intermodulation products created by the receiver frontend instead of the fundamental signals themselves. The phases of these intermodulation products across antenna elements are expected to behave differently from convential beamforming, asking for an updated analysis approach.

In this paper, we therefore provide a theoretical basis for the propagation and beamforming of intermodulation products in active phased array receivers and demonstrate the achievable linearity enhancements in measurements. This paper specifically targets beamforming for interference rejection in the low-GHz bands, for instance in the 2.4 GHz band, that is becoming very crowded. More information of interference mitigation by integrated MIMO system can for instance be found in [11]. To this end, this paper first expands on the analysis and design of the low-power beamforming architecture published earlier [10], by analyzing the constant-Gm vector modulation topology in section II and the low-power implementation of the beamforming receiver in section III. Next, Section IV focuses in detail on the intermodulation distortion performance in active phased arrays and proposes a theoretical model. Single-element and array measurement results are reported in section V to verify the linearity analysis, followed by the conclusions.

II. Vector Modulator Architectures

A. Cartesian Vector Modulator

The vector modulator is a combined phase shifter/amplitude modulator that in general depends on adding multiple copies of the input signal with different phase shifts and amplitude gains

[1][2][12][13]. In the phasor domain, each copy is represented by a vector whose length indicates the signal amplitude gain, and whose orientation indicates the signal phase shift. We can see that the combination of different vectors can lead to a final vector with arbitrary amplitude gain and phase shift, i.e. summing signal copies with different amplitude gains and phase shifts result in a summed signal which has arbitrary amplitude gain and phase shift. Vector modulator architectures differ in the way in which different phase shifts are generated and how amplitude gains are applied.

In a Cartesian vector modulator, a set of four basis signals having 0, 90, 180 and 270 degree phases are first generated. A convenient way of generating these phases in many radio architectures is to use the In-phase (I) and Quadrature (Q) outputs of a mixer, as well as their negative counterparts in a balanced structure, as is indicated in Fig. 2.

As summing is easy in the current domain and many I/Q mixers produce output voltages, variable transconductors are used to both convert to the current domain, scale the I and Q signals and sum into a common node. In order to reach all four quadrants of the phase shifter constellation (and hence cover a full 360 degree phase shift), it is necessary to have opposite phase I and Q signals available. In baseband zero-IF architectures, differential signaling is implemented to reject common-mode noise and disturbances, providing the required balanced signals. Also note that in order to preserve this rejection and to facilitate demodulation, it is required to generate a phase shifted four-phase output which is again differential and I/Q. Therefore, the hardware in a baseband Cartesian vector modulator is replicated four times.

Note that the *phase shifter* constellation is different from the *modulation* constellation of the signal itself. Each point in the phase shifter constellation represents an amplitude and phase adjustment that the vector modulator is capable of, represented as a phasor. Whereas the modulation changes its constellation point each symbol, the phase shifter constellation point is constant and only changes when the array is pointed to a different position. The modulation constellation of the signal is thus preserved while passing through the vector modulator, apart from a scaling and rotation of the entire signal constellation corresponding to the applied amplitude and phase

adjustment.

B. Constant-Gm Vector Modulator

From the principle of the Cartesian vector modulator in Fig. 2 we can observe that each constellation point requires different lengths of vectors, and that the sum of their lengths is also variable. In implementing this architecture care must therefore be taken that the variable amount of transconductance does not introduce phase and gain errors in the constellation. Moreover, good isolation between the output of and input of the variable transconductance is required.

Instead, in this paper we propose a vector modulator architecture that always uses the same total amount of tranconductance to produce a constellation point. The constant-Gm circuit architecture is shown in Fig. 3, and consists of a mixer as I/Q generator, a fixed bank of N binary scaled transconductances whose currents are summed into the output, and a set of reconfiguration switches at the transconductor inputs. These switches allow each transconductor to pick one of the four mixer phases, which effectively rotates its phase by 0, 90, 180 or 270 degrees.

The resulting constellation (shown in Fig. 4 for $N = 1$, $N = 2$ and $N = 3$) is square with equidistance points, but rotated 45 degrees with respect to the Cartesian vector modulator. It can therefore produce the same phase shifts and amplitudes, with similar quantization errors. The advantage of the constant-Gm vector modulator is that for any constellation point, the same number of transconductances are enabled. This translates into equal loading of all circuit nodes (including the RF input node), and therefore a higher precision in the constellation. Moreover, the total amount of transconductance for producing the same maximum output current is reduced by $\sqrt{2}$. In a Cartesian vector modulator, the transconductors are split by half on the real and imaginary axes, and a summation leads to a maximum of $1/\sqrt{(2)}$ times the total transconductance. In contrast, the transconductances in the constant-Gm vector modulator can sum up in-phase to the full total transconductance.

The constellation can be expanded by increasing N, i.e. by adding smaller binary scaled transconductances. The achievable phase resolution is limited by several factors. The I/Q phase error of

the LO clock generation can deform the constellation to a trapezoid shape, in a similar way to I/Q phase errors in image reject receivers. Furthermore, the mismatch between the transconductances generates randomly distributed phase and gain errors which can limit the resolution.

The mapping of desired phase shift and amplitude scaling is achieved by picking the nearest possible constellation point, therefore more transconductance quantization steps results in more vector modulator accuracy [4]. The maximum amplitude of the vector modulator is determined by the largest circle that can be drawn inside the boundaries of the constellation. Constellation points outside of this circle (in the corners) are therefore not usable.

The resolution of the quantized phase steps can be estimated by the realization that the shortest distance between two constellation points is approximately mapped to an arc that is a fraction of a circle with maximum radius that fits into the square constellation:

$$\text{phase points} \approx 2\pi \cdot 0.9 \cdot L \tag{1}$$

where the factor of 0.9 is a fitting factor to compensate for the curvature of the arc and L is the number of points along one axis in the square constellation. The number of phase points has to be rounded to the closest multiple of 4, to obtain a symmetric constellation. For example, in a 16x16 square constellation, the number of quantized phase points will be 44. An estimate for the depth of a null with respect to the main beam QL is given in dB by [4]:

$$QL \approx 6 \cdot \log_2(K) - 4 \tag{2}$$

where K is the number of phase steps in the phase shifter. This results in a rejection of 29 dB for 44 phase steps.

The constant-Gm vector modulator as depicted in Fig. 3 has the drawback that four duplicate sets of transconductors are required for the four mixer phases. We can however share the transconductors between the mixer phases in the case of a passive current mixer with non-overlapping clock phases (less than 25% duty cycle in this case). Since the current in such a mixer is steered towards one output at a time, the transconductors can be shared and thus moved to the RF domain.

This baseband to RF transformation is conceptually depicted in Fig. 5. Operation as a constant-Gm vector modulator is enabled by subdividing both the mixer and transconductor into multiple identical slices. The reconfiguration switches are in the baseband domain and essentially perform a 0, 90, 180 or 270 degrees phase shift for each slice. In general, for a constant-Gm architecture with N binary scaled groups, the number of identical slices M needed for the vector modulator is equal to:

$$M = 2^N - 1 \tag{3}$$

For a constant-Gm architecture with N binary scaled transconductors, a 2^Nx2^N constellation is created.

Changing the order from mixer-switches-*transconductors* (Fig. 3) to *transconductor*-mixer-switches thus enables a four-times reduction in the number of transconductors, with an associated 4X reduction in power consumption.

III. Low-Power Circuit Implementation

A. Low-Power Beamforming Frontend Topology

In order to implement the constant-Gm vector modulator, three elements are required: a transconductor, an I/Q mixer and reconfiguration switches. The low-power implementation consists of a 4-phase 25% duty cycle passive RC mixer for generating differential I/Q, as shown in Fig. 6. This mixer consumes no static power, and has a low conversion loss and low noise figure for the case where the RC product of the resistance driving the mixer (R_{OUT}) and load capacitance (C_{BB}) is larger than the switch-on time [14]. The theoretical minimum conversion loss and noise figure for 25% duty cycle is 0.9 dB, with additional noise from the switch resistances [14]. The switching mixer folds back harmonic images around 3 times and 5 times the LO frequency with a rejection of 10dB and 14dB respectively, as well as higher harmonics, so an additional RF bandpass filter will be required [15].

Adding reconfiguration switches after each mixer to steer the current of each slice to one of the four outputs completes the components for the vector modulator. Their on-resistance can be

made low by sizing the transistors large, as their capacitance can be absorbed into the baseband capacitors. The baseband bandwidth can be made reconfigurable by implementing the baseband capacitors as a variable capacitor bank, without affecting the vector modulator constellation, at no additional power consumption.

The vector modulator transconductance at RF acts as an LNA and provides input matching at the RF input port. In this design, a shunt resistor feedback inverter amplifier operating in moderate inversion is chosen because of its high power efficiency. The inverter reuses current in the NMOS and the PMOS which both contribute to the total transconductance. The shunt feedback resistor provides a low noise, low power impedance match due to the Miller effect caused by the voltage gain between input and output of the amplifier [16][17]. The output impedance looking into the inverter structure is calculated as:

$$R_{OUT} = R_{ds,N}//R_{ds,P}//\frac{R_s + R_f}{1 + (Gm_N + Gm_P)R_s} \tag{4}$$

where $R_{ds,N}$ and $R_{ds,P}$ are the output conductances of the inverter NMOS and PMOS, Gm_N and Gm_P are the NMOS and PMOS transconductances, R_s is the source resistance driving the RF port, and R_f is the shunt feedback resistance.

By AC-coupling the receiver at RF and biasing the sources and drains of the mixer switches at ground potential, the inverters of the clock tree can directly drive the gates of the mixer switches with large overdrive. The added benefit of RF AC coupling is the blocking of IM2 products generated by the LNA inverter, which boosts narrowband IIP2 performance, as well as filtering of the inverter 1/f noise. The AC-coupling capacitor is implemented with a Metal-Insulator-Metal capacitor for minimum parasitic capacitance to ground (1% of the capacitance value). The combined parasitic capacitance to ground of the LNA, AC-coupling capacitor and mixer switches forms a pole with the output impedance of the LNA and therefore limits the RF bandwidth of the system.

Because a minimum gate-length inverter is used as the LNA, its intrinsic gain is limited to 7.5, and noise contribution due to the output impedance of the LNA and the mixer switches raise the noise figure of a single element to about 6dB in simulation. Alternatively, a larger than

minimum gate-length can result in better gain, linearity and noise figure at the expense of lower RF bandwidth.

This receiver slice is expanded into the full beamforming receiver with vector modulation by copying the unit slice multiple times and connecting the baseband capacitance nodes together, which is shown schematically in Fig. 7. The currents of the antenna elements are summed into the summing node and filtered by the common baseband capacitances.

In the implemented N=4 design with a 16x16 constellation, a total of 15 slices per element are needed, with each slice providing 1/15th of the input match. This structure is again multiplied for the amount of antenna elements that is needed. In contrast to the Cartesian vector modulator, there are no variable transconductances, but only a rerouting of mixer current. Therefore, the constant-Gm topology provides a constant impedance match, and also a constant mixer baseband bandwidth over all vector modulator codes.

B. Mixer Transformation Properties

One important aspect of the passive mixer is its lack of isolation from output to input. Rather than an undesirable property, this fact is utilized in this design to improve the receiver's robustness to large interferers in the frequency and spatial domain [7].

The important observation to note is that the voltage swing on the mixer RF node is a translation of the baseband voltage swings [18]. A lowering of the baseband voltage swing results therefore in a lowering of the RF voltage swing.

In the frequency domain, this property expresses itself in the low-pass filtering by the baseband capacitors. The -3 dB baseband bandwidth of the passive mixer is determined by the output impedance of the inverter structure including feedback resistance, together with the baseband capacitors (assuming that switch resistance is negligible compared to the inverter output resistance):

$$BW = \frac{1}{2\pi \cdot 4 \cdot R_{out} C_{BB}} \tag{5}$$

Intuitively, the factor of 4 can be understood as relating to duty-cycle: each capacitor is only charged 1/4 of the period. In the stop band of this low pass filter, the voltage swing on the baseband capacitor

as well as the mixer RF node is reduced. Effectively, the low pass filter at baseband is translated into a band-pass filter at RF centered around the clock frequency [7][19][20]. The reduced out-of-band voltage swing at the inverter output increases its out-of-band compression point, as well as 3rd-order intercept points due to output conductance non-linearity.

This concept can be extended to the beamforming pattern of the array, in the spatial domain. For signals coming from the directions for which the beamforming algorithm maximizes the signal amplitude, the currents from the array elements are in phase and sum up coherently into a larger current, which results in a large voltage swing on the baseband capacitors. For cancelled signals, the element currents destructively sum into a small current and hence a lowered baseband voltage swing. Since this reduced voltage swing is transformed to the RF node, the out-of-beam compression point and weak non-linearity of the inverters are also improved.

C. Clock Generation

An accurate four-phase 25% duty cycle clock is required to drive the mixer switches in the vector modulator. Phase errors between clock phases are transferred to the phases of the rotated vector in the modulator, resulting in a gain and phase error after summation. As a result, the square constellation may become trapezoid, a property that is known from image-reject receiver architectures.

The clock generation is performed on-chip in a clock divider architecture, shown in Fig. 8, with a differential external clock as a reference. The first part of the clock generation performs a divide-by-two with a looped flipflop, in order to divide down the reference clock and produce enough clock edges to select for the four clock phases. Next, a shift register generates the four phases, but with a 50% duty cycle. Therefore, AND gates combine pairs of shift register outputs together to produce 25% duty cycle clock signals.

The balance of the differential reference clock is of importance, as the edges of half the output phases originate from the positive reference, while the edges of the other half originate from the negative reference. In other words, a phase imbalance in the reference clock is transferred to an

I/Q imbalance in the output phases. Therefore, the reference is first amplified with Current-Mode-Logic buffers whose common-mode-rejection reduces common-mode components in the clock, and therefore the imbalance. These buffers also serve the purpose of boosting the reference clock amplitude to a square waveform. In simulation, the RMS phase imbalance is found to be 0.7 degrees.

IV. Intermodulation Products in Active Beamforming Arrays

A. Frontend Linearity Model

Fig. 9 illustrates the signal flows in an active beamforming frontend with passive mixer. Note that only one mixer switch and one baseband capacitor is shown for clarity.

The LNA transconductor converts the RF voltage to current i_{LNA}, which is mixed down by the mixer switch with a 25% duty cycle clock waveform. The downconverted modulated current i_{BB} has conversion gain of $1/4\text{sinc}(1/4) \approx 0.9$, which models the conversion of RF current into higher mixer harmonics [21].

If only one frontend is present, the baseband current i_{BB} gets converted into voltage by the equivalent baseband impedance R_{BB}. This impedance is equivalent to four times the LNA output impedance, as it is connected by the switch to the baseband node for one-quarter of the time. The gain (in-beam and in-band) of the frontend is therefore equivalent to:

$$G_{BB} = Gm_{LNA} \cdot R_{OUT} \cdot \text{sinc}(1/4) \tag{6}$$

which is the intrinsic voltage gain of the LNA inverter reduced by the mixer conversion loss of 0.9dB.

A pole is present at the baseband node due to the equivalent baseband impedance R_{BB} and capacitor C_{BB}, with frequency [22]:

$$f_{BB} = \frac{1}{2\pi \cdot 4 \cdot R_{OUT} C_{BB}} \tag{7}$$

From the impedance transformation properties of the passive mixer, the filtered baseband voltage gets upconverted to the LNA RF output node. This can be seen as a second mixer action, since

the passive mixer is bi-directional. The conversion gain of this upconversion is equivalent to $\text{sinc}(1/4) \approx 0.9$. As a result, the low pass filtering on the baseband node is translated into a bandpass filtering on the mixer RF input [8].

The intermodulation products due to weak non-linearity in this design are mainly generated by the LNA, since the linearity of the passive mixer very high and the gain of the LNA is rather low. These components arise due to the non-linearity in the inverter transconductance and drain-voltage-swing induced distortion. Since the voltage on the LNA output is upconverted from the filtered baseband output voltage, the distortion current of the NMOS and PMOS output conductance is filtered as well. Therefore, an increase of IIP3 is expected out-of-band, but up to a certain point where the transconductance non-linearity is dominating.

When the baseband currents are out-of-phase, complete or partial cancelling of the currents occur and the baseband voltage swing is reduced. This is the main principle behind spatial filtering from the beamforming array. Also, it can be concluded that the LNA output voltage swing is reduced as well, leading to an increase of IIP3 . However, the intermodulation currents due to the LNA transconductance can also be reduced due to the beamforming action, as they can cancel in the summation process. This depends on the relative phases of the intermodulation currents between antenna elements, as discussed in the next subsection.

B. Intermodulation Array Factor

The gain due to beamforming, the array factor AF, can be expressed as [23]:

$$AF_{FUN}(u) = \sum_{n=0}^{N-1} e^{j2\pi \cdot n \frac{d}{\lambda}(u-u_0)}. \tag{8}$$

where $u \equiv \sin(\theta)$ expresses the angle-of-arrival in u-space, d is the distance between antenna elements, λ is the wavelength, u_0 is the direction in which the main beam is steered and N is the number of antennas in the array. The array factor describes the spatial filtering that is performed by the array. For short-hand notation we introduce the constant:

$$\Phi \equiv 2\pi \frac{d}{\lambda} \tag{9}$$

With the main beam steered to the signal-of-interest, interferers are spatially filtered by the array factor. By small perturbations of the element weights in both amplitude and phase, nulls can be steered to interferer directions, thereby maximizing interferer rejection [4].

Non-linearity in the frontends before the summing node will generate intermodulation tones, which are affected by the beamforming as well. Fig. 10 illustrates the propagation of intermodulation tones in multiple antenna elements. The phase difference between fundamental tones of different antenna elements is preserved after the non-linearity. As such, the intermodulation tones have defined phase differences depending on the particular intermodulation product, and are shaped by a different antenna factor than the fundamental tones.

In this analysis we consider the distortion caused by two interferers with sinusoidal sources, with frequency ω_1 and ω_2 respectively, which are being received on angle u_1 and u_2 respectively. The n-th antenna will receive the following sum of the two phase shifted interferers:

$$RX_n(t) = \cos(\omega_1 t + n \cdot u_1 \cdot \Phi) + \cos(\omega_2 t + n \cdot u_2 \cdot \Phi) \tag{10}$$

The array is pointed towards the desired signal at angle u_0, so that its phase shift across the elements is equal in phase and the signal is coherently summed.

In contrast, after third order distortion in the LNA, third-order intermodulation (IM3) terms emerge on the nth channel:

$$\begin{aligned}(RX_N)^3(t) =& C_{12} \cdot \cos((2 \cdot \omega_1 - \omega_2)t + n \cdot (2 \cdot u_1 - u_2)\Phi) + \\ & C_{21} \cdot \cos((2 \cdot \omega_2 - \omega_1)t + n \cdot (2 \cdot u_2 - u_1)\Phi) + ...\end{aligned} \tag{11}$$

where C_{12} and C_{21} are constants. In particular, an IM3 term emerges with frequency $2 \cdot \omega_1 - \omega_2$ and a second term with $2 \cdot \omega_2 - \omega_1$. The phase of the IM3 terms is equal to $n \cdot (2 \cdot u_1 - u_2)\Phi$ and $n \cdot (2 \cdot u_2 - u_1)\Phi$ respectively. When comparing to (10), it is seen that these phase differences correspond to the case where a fundamental signal is originating from $2 \cdot u_2 - u_1$ and $2 \cdot u_1 - u_2$ respectively.

In general, we can conclude that for an intermodulation tone located at frequency:

$$\omega_{IM} = A_1 \cdot \omega_1 + A_2 \cdot \omega_2 \tag{12}$$

the corresponding effective angle in u-space of the intermodulation tone follows the same linear combination with coefficients A_1 and A_2:

$$u_{IM} = A_1 \cdot u_1 + A_2 \cdot u_2. \tag{13}$$

By substition into (8), the array factor for the intermodulation tone is equal to:

$$AF_{IM} = \sum_{n=0}^{N-1} e^{jn\Phi(A_1 u_1 + A_2 u_2 - u_0)}. \tag{14}$$

Examining (14) it is seen that the the intermodulation array factor AF_{IM} can be obtained from the fundamental array factor AF_{FUN} in (8)by substitution of $u = u_{IM} = A_1 \cdot u_1 + A_2 \cdot u_2$. In principle, existing nulling algorithms that steer nulls in the fundamental array factor could also be used to steer nulls in the intermodulation array factor to improve linearity, as illustrated in Fig. 11. This figure plots an array factor in solid line with a null located close to $u = 0.2$. This null can be steered to the location of an interferer by adjusting the beamforming weights. Two of these adjusted patterns with shifted null position are also displayed in the figure in dashed lines. For intermodulation nulling it is however required to steer the null to the effective angle in u-space, u_{IM} which is a combination of the angle of the interferers and the intermodulation coefficients as outlined in(13). These algorithms are left for exploration in future work.

V. Measurements

The 4-element beamforming receiver was implemented in STMicroelectronics's standard 65-nm LP CMOS technology (die photograph in Fig. 12), with an active area of 0.20 mm^2 including the baseband capacitors, RF AC coupling capacitors and clock generation. The baseband switches and associated routing, which are additional requirements for a Constant-Gm vector-modulator, occupy less than 0.3% of the total active area. The baseband capacitance area is not affected by the slicing of the receiver elements and the RF AC-decoupling capacitor area increases only by about 20%. This renders only a small change in the length of the required clock distribution wires and hence no significant additional power penalty.

A. Single Element Measurements

The performance of a single element is evaluated by disabling all the reconfiguration switches in three out of four antenna elements. This effectively disconnects all but one antenna element from the output. The differential baseband outputs are sensed with two Lecroy AP033 high input impedance active differential probes. The frequency band of operation is from 1.0 to 2.5 GHz, with center frequency set by the LO frequency. The baseband bandwidth can be changed from 30 to 300 MHz by the tunable baseband capacitances, allowing for operation in different radio standards.

The complete receiver frontend consumes between 26 to 36 mW from a 1 V supply, as the clock frequency is increased from 1.0 to 2.5 GHz. The increase in power consumption is due to the dynamic power consumed in the clock divider and clock tree. This amounts to 6.5 to 9 mW of power consumption per element, with clock generation included.

In the passband, the gain of a single element is measured to be 12 dB, with a DSB noise figure of 6 dB. With all four elements enabled, the baseband voltages of the elements are averaged, leading to the same baseband voltage swing as in the single element case in the main beam, where complete coherent summation occurs. The increased sensitivity is due to the reduced noise by the averaging (summing) operation, leading to a 6 dB improvement for 4 elements.

The measured vector modulator constellation is given in Fig. 13 and compared to an ideal 16x16 square equidistance constellation. The constellation was measured with a VNA using a single-tone stimulus with an input power of -20 dBm. Note that this is not the modulation constellation of the signal, but the phase shifter constellation representing the possible phase shifts and amplitude adjustments that the vector modulator is capable of. The realized phasor points are close to the ideal, with an RMS phase error of 0.8 degrees and a RMS gain error of 0.17 dB. This translates to a 1.4% EVM. The constellation of ten dies was measured and the mismatch between their constellations was determined to be 0.07 dB RMS in gain and 0.7 degrees in phase.The high accuracy in the constellation is reached due to a small imbalance in the I/Q clocks and good

matching between the vector modulator slices, without the need for calibration.

The input-referred third-order intercept point (IIP3) and 1 dB compression point (CP) are plotted for a clock frequency of 1.5 GHz in Fig. 15, together with the gain and S11. It is observed that the IIP3 increases from 1 dBm in-band to 5 dBm out-of-band, while the CP increases from -9 dBm in-band to -3 dBm out-of-band. The increased linearity performance is due to the impedance transformation properties of the passive mixer in the vector modulator, which translates the lowpass baseband filter into an equivalent bandpass RF filter. This improves the robustness of this architecture to interferers present before the beamforming summing node. It can also be seen that the S11 is degraded out-of-band, due to the resistive-feedback matching network at the LNA input. Looking a Fig. 15, we see that a dip in CP1dB and IIP3 occurs at a frequency below the switching frequency of 1.5GHz, which is likely related to the shift in S11 as often seen in N-path filters, due to parasitic input capacitance as discussed in [18]. It is notable that the maximum gain does not coincide exactly with these dips, which is a subject for further investigations.

Fig. 16 plots the gain, NF and IIP3 over LO frequency up to 2.5 GHz. The pole at the LNA output node is responsible for the gain roll-off at higher frequencies, limiting the maximum operating frequency of the receiver.

As interferers are present in the frontend upto the summing node, the small signal NF should not degrade when interferers are present. Fig. 17 plots the single-element NF versus blocker power at 1.5 GHz RF with 80 MHz blocker offset. The NF is unaffected upto -20 dBm of blocker power, after which a 3 dB degradation is present at -10 dBm of blocker power.

B. Intermodulation Array Factor

In these measurements the IIP3 of the beamforming receiver is measured and compared to the theoretical intermodulation array factor equations as discussed in the previous section. Three somewhat arbitrary cases will be discussed that exhibit interesting behavior and show the merit of the intermodulation array factor for predicting the linearity performance of the beamforming receiver.

To this end, the intermodulation distortion performance of the beamforming phased array was evaluated with the measurement setup in Fig. 18. An RF signal is split into four and phase shifted with high-precision discrete vector modulators (Telemakus TEV2700-45) to emulate an interferer wavefront coming from direction u_1. At the same time, a second RF signal is split into four and fed directly into the receiver, thereby emulating a second interferer coming from broadside ($u_2 = 0$). In addition, the receiver applies the required phase shift to point the main beam to the desired signal direction u_0 (in this experiment no amplitude control is utilized to steer the nulls). In this setup, we can therefore control the angle between the two interferers, as well as the angle between the main beam and the interferers.

Care was taken to match transmission lines and power splitter/combiners in this setup, in order to minimize the effect of phase and gain errors on the measurement results. The external vector modulators were individually calibrated. We estimate that the resulting phase and gain errors were less than 1.0 degrees and 0.1 dB respectively, which if modelled as random errors in a 4-element phased array would result in a peak error sidelobe level of better than 28 dB below the main beam [24]. As the nulls in the measured IIP3 are less than 20 dB deep and are at the same location as the nulls in the simulated intermodulation beamforming array factor, we therefore believe that this measurement setup has adequately low phase and gain errors.

With a spectrum analyzer, the fundamental and IM3 products after summing were measured, and an IIP3 was calculated. We will now show that the IIP3 depends on the angles between the main beam and the two interferers. To illustrate this point, Fig. 19 plots the IIP3 calculated from the IM3 frequency tone ($A_1 = 2$ and $A_2 = -1$), for three scenarios. The calculated intermodulation array factor according to (14) is displayed in grey. In the first scenario shown in Fig. 19a, the two interferers are located at the same angle. In this case, $u_1 = u_2$, and the intermodulation array factor is calculated as:

$$AF_{IM}(u_1 - u_0)|_{u_1=u_2} = \sum_{n=0}^{N-1} e^{jn\Phi(2*u_1-u_2-u_0)} = \sum_{n=0}^{N-1} e^{jn\Phi(u_1-u_0)} = AF_{FUN}(u = u_1 - u_0) \quad (15)$$

In this case when the two interferer tones are at the same angle, the third order intermodulation AF

follows the fundamental tone AF. It is observed that the IIP3 is increased when the array factor is decreased by as much as 18 dB. When the interferers are at the same direction as the main beam, the IIP3 is minimum as no cancellation is possible without reducing the desired signal as well.

In the second scenario in Fig. 19b, the interferers are spaced apart by 45 degrees (0.5 in u-space) and their direction is swept with respect to the main beam. In this case $u_2 = u_1 + 0.5$ and we can derive:

$$AF_{IM}(u_1 - u_0)|_{u_2=u_1+0.5} = \sum_{n=0}^{N-1} e^{jn\Phi(2*u_1-u_2-u_0)} = \sum_{n=0}^{N-1} e^{jn\Phi(u_1-u_0-(u_1-u_2))} \\ = AF_{FUN}(u = u_1 - u_0 - 0.5) \tag{16}$$

This means that the intermodulation AF is shifted with respect to the fundamental AF (by 0.5 in u-space). Interestingly, even when one interferer is at the same angle as the main beam ($u_1 - u_0 = 0$), cancelling of its intermodulation product is achieved by the second interferer at angle $u_2 = u_0 + 0.5$.

In the third scenario, Fig. 19c displays the scenario when one interferer is kept with the same direction as the main beam, while the second interferer is swept, so that $u_2 = u_0$:

$$AF_{IM}(u_1 - u_0)|_{u_2=u_0} = \sum_{n=0}^{N-1} e^{jn\Phi(2*u_1-u_2-u_0)} = \sum_{n=0}^{N-1} e^{jn\Phi(2u_1-2u_0)} = AF_{FUN}(u = 2(u_1 - u_0)) \tag{17}$$

In this case, the intermodulation array factor in u-space is compressed by a factor of two as compared to the fundamental array factor. With the first interferer at angle $u_1 = 1.0$, the fundamental AF would suggest a high IIP3, but the third order intermodulation AF reveals that the intermodulation products are not cancelled and the measurement reveals a low IIP3 instead.

Since the receiver is capable of both amplitude and phase steering, an adaptive nulling algorithm could be used to steer the nulls in the intermodulation AF to the angle of the interferers, depending on the actual interferer scenario. The details of this implementation are left as future work.

C. Comparison with State-of-the-Art Beamforming Receivers

The measured results are compared to state-of-the-art beamforming receivers in Table I. This design consumes between 6.5 and 9.0 mW of power per element, while achieving a NF of 6 dB,

which is a significantly lower power consumption than the state-of-the-art. This is achieved by utilizing the following design techniques. Firstly, the constant-Gm vector modulator architecture efficiently utilizes a fixed number of transconductances to produce each point on the constellation. This architecture furthermore allows the transconductances to be moved from baseband to RF which achieves a four-fold reduction of the total required transconductance. Note that the LO phase generation is included in the power consumption of all designs by dividing its power dissipation by the number of elements.

In earlier published designs, a multitude of linearity performance figures has been reported, due to the combination of frequency and spatial filtering in beamforming receivers. Similar to the familiar in-band and out-of-band distortion figures which define whether we are inside or outside the frequency filtered band of interest, we can define in-beam as the condition where maximal coherent summing occurs and out-of-beam where some spatial filtering occurs.

As some designs do not provide gain [6] [7] [8], using input-referred IP3 under in-beam conditions can be misleading as linearity will be degraded by subsequent gain stages. In this case, comparing output-referred IP3 is preferred. On the other hand, out-of-beam conditions justify that spatial filtering has occurred and that the interferers are suppressed sufficiently such that additional gain stages do not degrade linearity further, enabling the use of input-referred IP3. This design achieves high in-band IP3 due to the spatial suppression of intermodulation products, while the out-of-band IIP3 is limited by the input transconductor and is lower than passive-first designs with N-path filters applied to the RF input [6] [7] [8] or across the input transconductor [9].

There is a trade-off between RF frequency and power consumption in this architecture. The RF frequency range is mainly limited by two effects, namely the pole at the LNA output node and parasitic capacitance in the LO frequency divider. In the current design, the LNA output capacitance dominates the bandwidth limitation, which is largely determined by the intrinsic speed of the technology but can be improved by increasing the supply voltage. Even though the clock divider is implemented using power efficient dynamic logic, it becomes a relevant power contribution at

high frequency, as power consumption scales linearly with frequency. Reducing mixer switch size helps to reduce the capacitive loading to the LO-frequency divider, but comes at the cost of less out-of-band N-path filtering and hence degrades out-of-band and out-of-beam linearity.

From the comparison, we can conclude that this design achieves a balance between NF, gain and intermodulation distortion performance, while maintaining low power consumption.

VI. Conclusion

In this paper, a low-power four-element beamforming receiver with constant-Gm vector modulator was presented. The vector modulator combines rotated binary scaled signals into the phase shifted and amplitude scaled output, implementing a 16x16 square constellation. The constant number of enabled transconductances avoids errors due to code-dependent loading of the circuit nodes. By moving the vector modulator transconductors into the RF domain before the passive 25% duty cycle I/Q mixer, a four-fold reduction in the amount of transconductance is achieved. The shunt resistor feedback inverter-based transconductors double as LNA and provide low-power impedance matching at the input ports.

The 65-nm implementation consumes between 6.5 and 9 mW per antenna element in a 1.0 to 2.5 GHz RF frequency band, including clock generator, and achieves a single-element 6 dB NF. The measured RMS phase and gain errors with respect to an ideal square equidistance constellation are 0.8 degrees and 0.17 dB respectively. A theoretical model for the cancellation of frontend intermodulation products in active phased arrays was given, showing that these products follow a different array factor due to their modified effective angle-of-arrival. Measurements observed an improvement of up to 19 dB in IIP3 for out-of-beam interferers.

Acknowledgements

This research was conducted as part of the Sensor Technology Applied in Reconfigurable systems for sustainable Security (STARS) project funded by the Dutch Government. We thank STMicroelectronics for silicon donation and CMP for assistance. Many thanks to Hugo Westerveld

for assistance during measurements. Also, thanks go to Gerard Wienk and Henk de Vries for CAD support and lab assistance.

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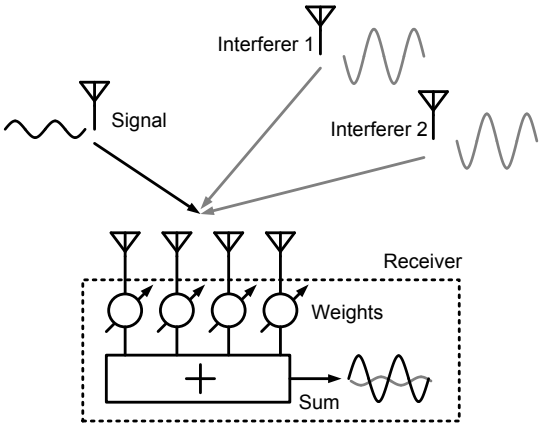

Fig. 1: Principle of a beamforming receiver for sensitivity improvement and interferer suppression.

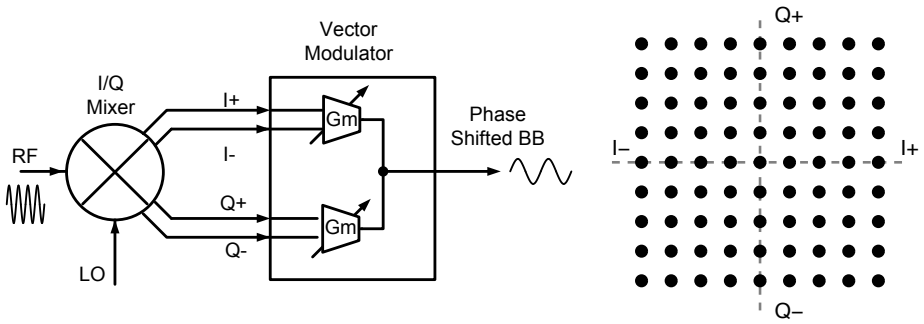

Fig. 2: Cartesian baseband vector modulator block diagram and phase shift constellation.

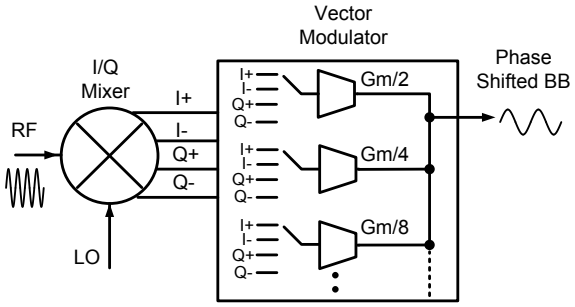

Fig. 3: Constant-Gm baseband vector modulator block diagram.

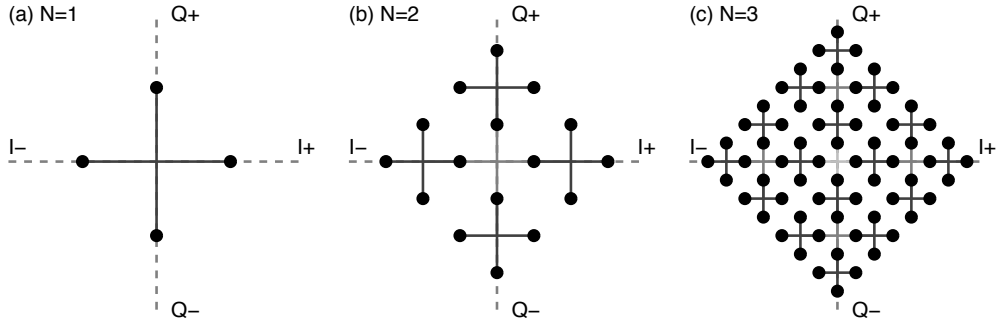

Fig. 4: Constant-Gm phase shift constellation for (a) N=1, (b) N=2 and (c) N=3.

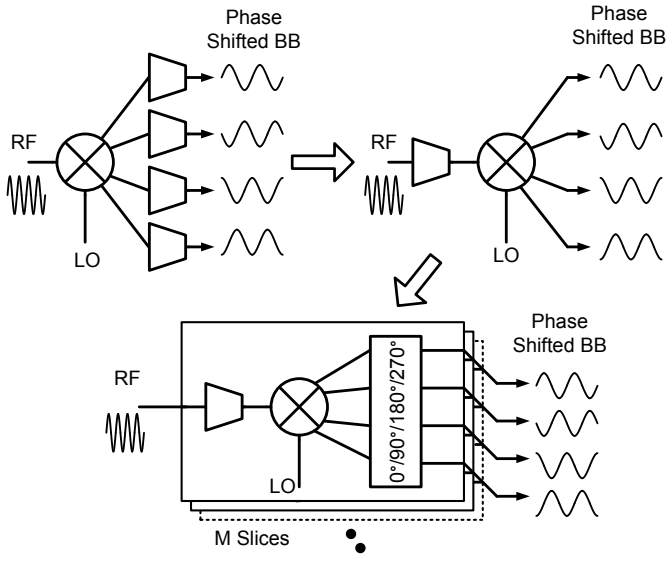

Fig. 5: Transformation of the transconductance from baseband to RF for a passive mixer with non-overlapping clock phases, and subsequent slicing into a constant-Gm vector modulator.

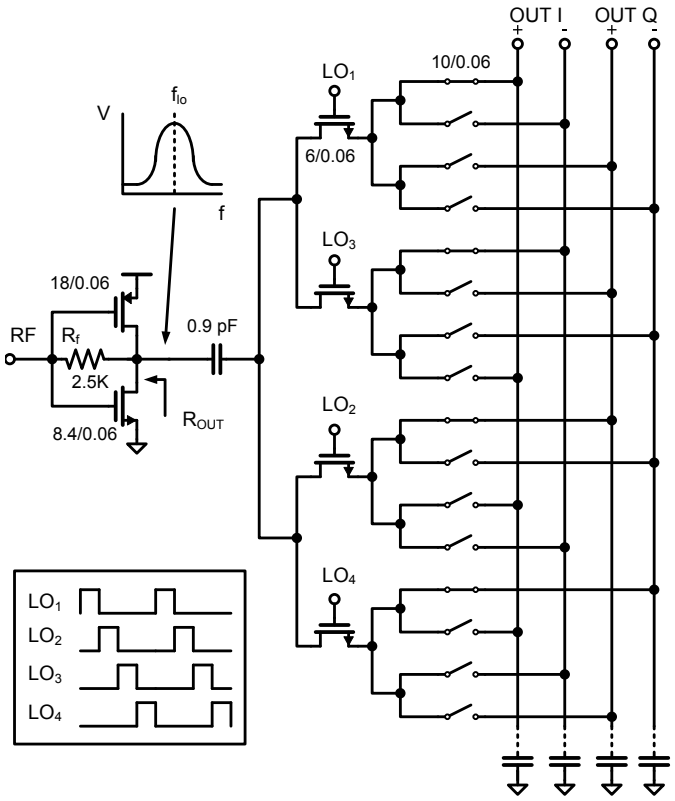

Fig. 6: Unit slice of the receiver frontend.

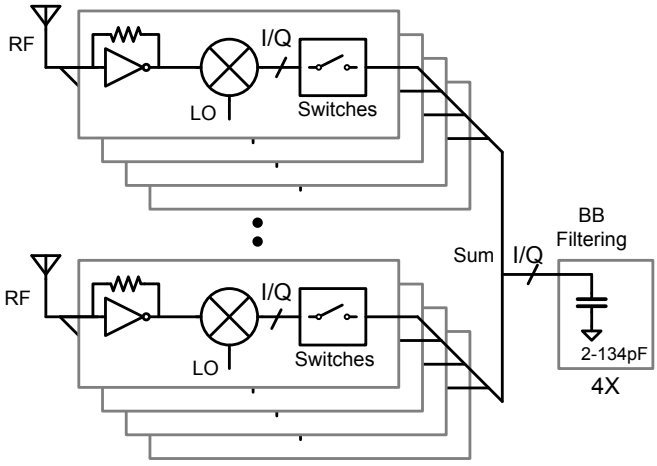

Fig. 7: Receiver frontend with constant-Gm vector modulation.

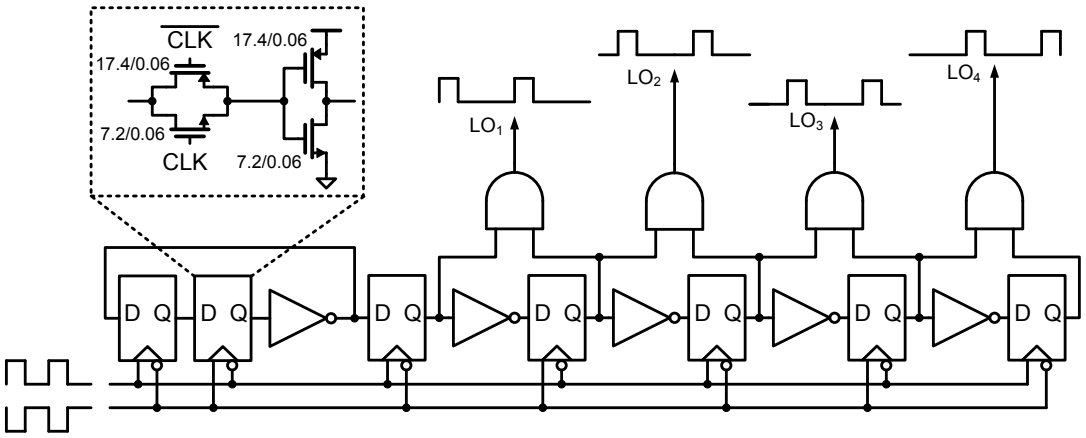

Fig. 8: Clock generation block diagram.

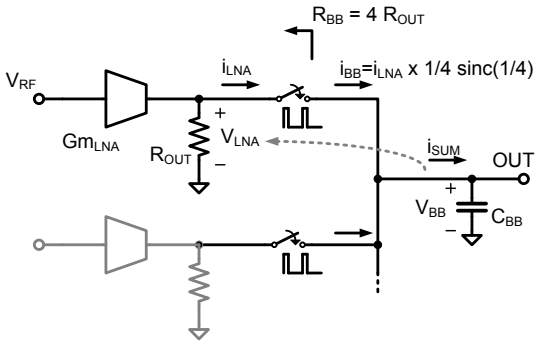

Fig. 9: Signal transformation in an active beamformer with passive mixer.

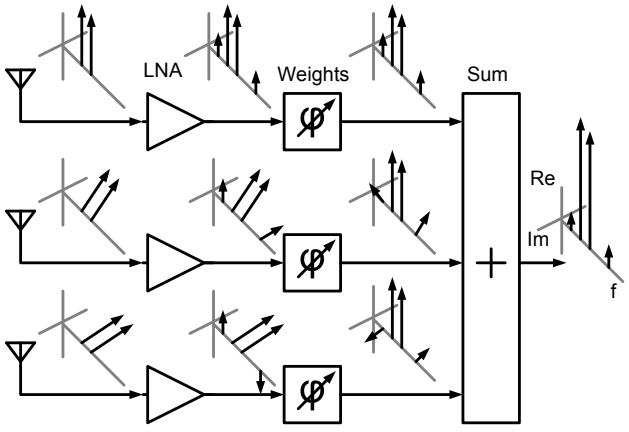

Fig. 10: Example of second-order intermodulation (IM2) products in an active phased array.

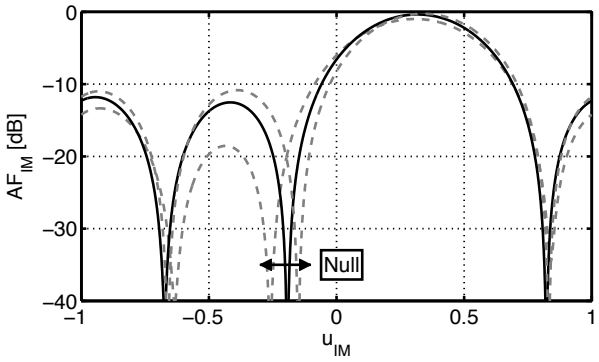

Fig. 11: Null steering in the intermodulation array factor AF_{IM}. Two alternative array factors with the null located in a different location are indicated with dashed lines.

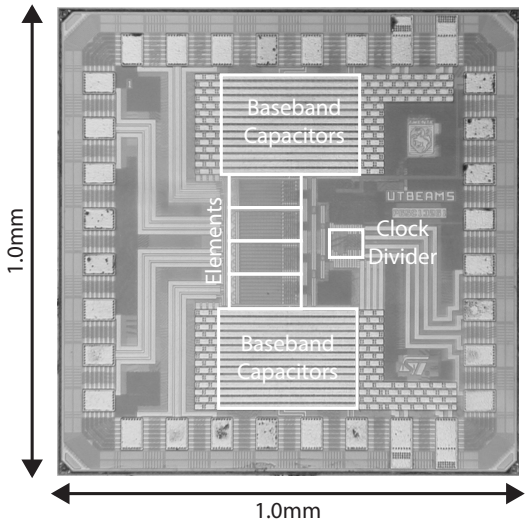

Fig. 12: Chip photograph of the four-element beamforming receiver, die measuring 1.0 by 1.0 mm.

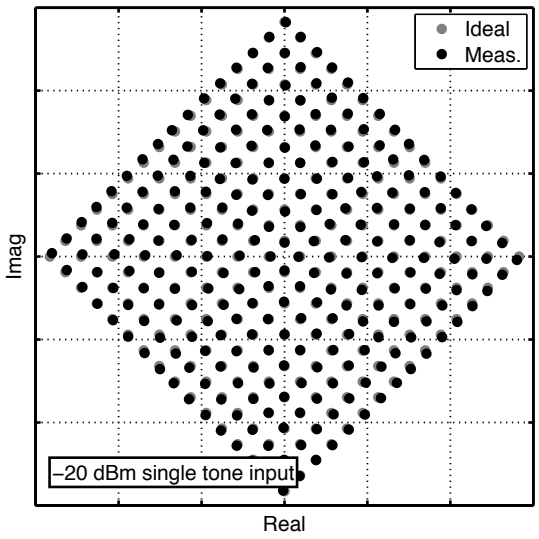

Fig. 13: Measured vector modulator constellation, single tone excitation with -20 dBm input power.

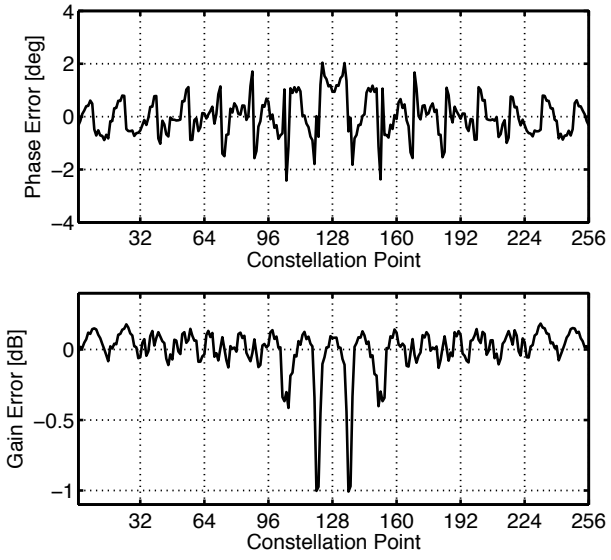

Fig. 14: Measured phase and gain errors of constellation.

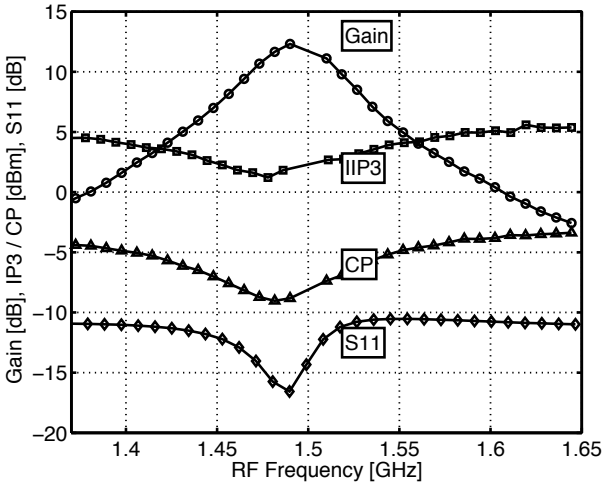

Fig. 15: Measured gain, linearity and S11 at 1.5 GHz LO frequency for a single element.

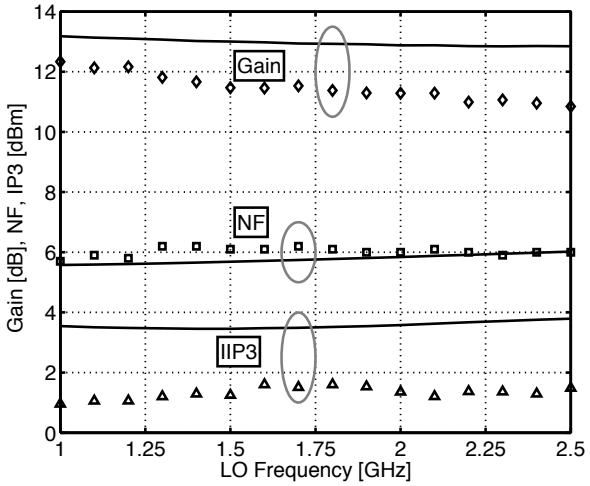

Fig. 16: Gain, NF and IIP3 swept over LO frequency for a single element(simulation in lines, measurements in markers)

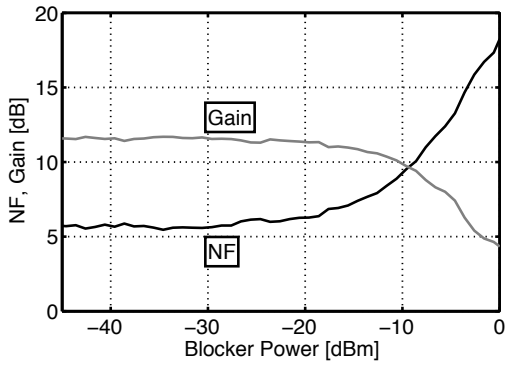

Fig. 17: Measured single-element noise figure versus blocker power.

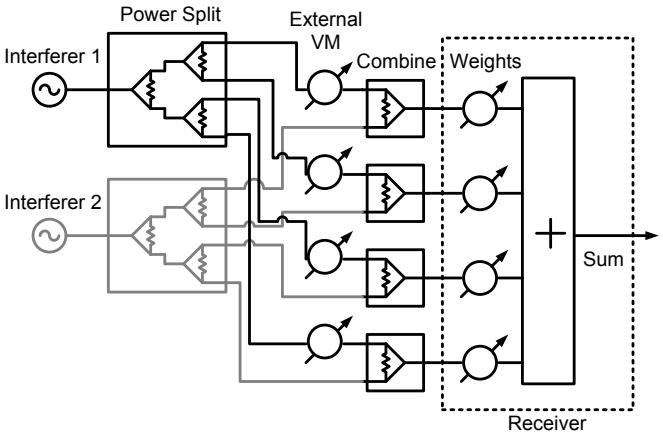

Fig. 18: Intermodulation measurement setup.

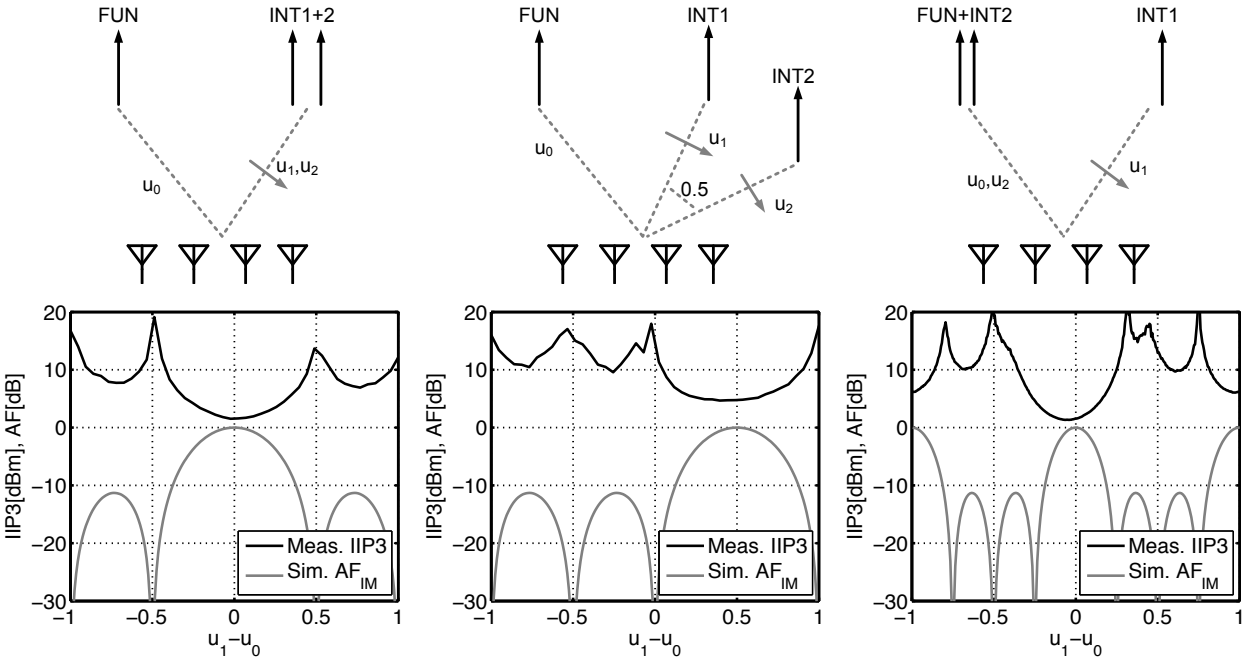

Fig. 19: Calculated third-order intermodulation array factors (AF_{IM}) and measured IIP3 for (a) $u_1 = u_2$, (b) $u_2 = u_1 + 0.5$ and (c) $u_2 = u_0$

	[3]	[6]	[7]	[8]	[9]	This Work	
Technology	90nm	65nm	65nm	28nm	65nm	65nm	
Active Area	1.4	0.18	0.97	0.65	1.69	0.20	mm2
Supply Voltage	1.2	1.0-1.2	1.2	1.0	1.2	1.0	V
RF Frequency	4.0	1.5-5.0	0.6-3.6	0.6-4.5	0.1-1.7	1.0-2.5	GHz
Power/Element	41[1]	16-42[1]	17-49[1]	8.5-30[1]	37@500MHz[1]	6.5-9[1]	mW
# Phase Shifter Steps	32	32	8	8	64	44	
Gain	15	-6	-1	-1	41	12	dB
1-Element Noise Figure	13	18	4	4	2.2-4.6	6	dB
4-Element SNR improvement	6	6	4	4	6	6	dB
CP (in-band,in-beam)	N/A	2	-5	-5.5	N/A	-9	dBm
OIP3 (in-band,in-beam)	17	7	5	5	0	13	dBm
IIP3 (in-band,out-of-beam)	N/A	N/A	+2..+9	+5.5..+11	-7	+1..+20	dBm
IIP3 (out-of-band,in-beam)	+2	N/A	+11	+20	+11	+5	dBm

[1] Includes LO clock divider power divided by the number of elements.

TABLE I: Comparison with state-of-the-art beamforming receivers.