A Coupled Sawtooth Oscillator Combining Low Jitter With High Control Linearity

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Abstract—A new type of relaxation oscillator is presented that combines excellent control linearity with low timing jitter. By using an alternative for the Schmitt trigger, the jitter caused by threshold level noise can be significantly reduced compared to a conventional relaxation oscillator, under equal conditions of control linearity. Circuits realized in a 0.8-μm CMOS process show a typical measured distortion in the control characteristic of $HD_2 = -67$ dB and $HD_3 = -90$ dB ($\Delta f = 500$ KHz), without using any feedback linearization techniques. The measured phase noise is -102 dBc/Hz at 10-kHz offset at $f_{osc} = 1.5$ MHz (65-ppm rms jitter) for a total supply current of 360 μA.

I. INTRODUCTION

VOLTAGE-CONTROLLED oscillators (VCOs) are widely used in applications such as phase-locked loops (PLLs), frequency (de)modulators, and timing recovery circuits. A low jitter is important in these applications in order to achieve a high dynamic range. Apart from low jitter, VCOs used in frequency (de)modulation circuits also require good control linearity, to minimize distortion of the (de)modulated signal [1]. Furthermore, control linearity is desirable for an optimal loop transfer function of the PLL [2]. Finally, a VCO with high control linearity can be applied as multibit quantizer/integrator in a delta–sigma analog-to-digital (AD) converter [3].

The relaxation oscillator's strength is that it combines a naturally wide tuning range with a fundamentally linear frequency-control characteristic. However, in conventional relaxation oscillators, the achievement of high control linearity comes at the expense of an increase in jitter. This article presents a new, alternative relaxation oscillator concept that circumvents this tradeoff.

Fig. 1 shows a circuit schematic of a conventional relaxation oscillator. Whenever the capacitor voltage reaches one of either threshold level V_H or V_L, the bistable memory toggles and reverses the direction of the capacitor current. The delay t_d, introduced by the level detection circuitry, is the major cause of the oscillator's control nonlinearity, as it forms a part of the period of oscillation that is not inversely proportional to the control current [1], [4]. Conventionally, high control linearity is achieved
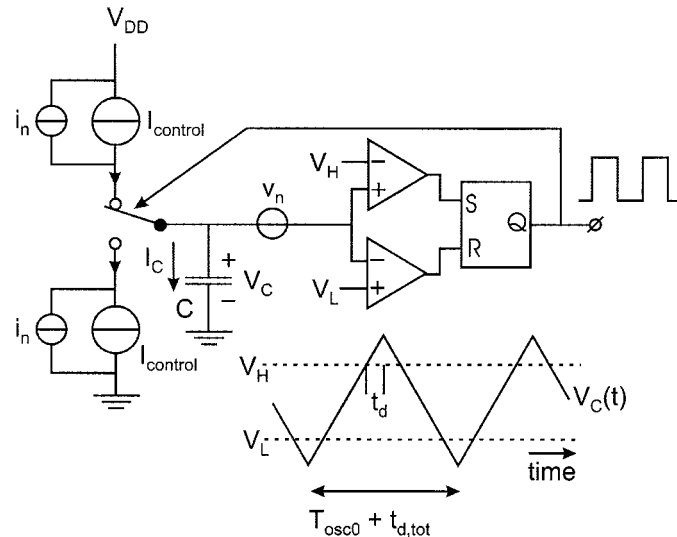
Fig. 1. Conventional relaxation oscillator and its waveforms.

by making the detection circuit fast, resulting in a small delay t_d compared to the overall period of oscillation T_{osc}. However, a faster detection results in an increased jitter, as will be clarified in Section II. Thus, in the design of the relaxation oscillator, a tradeoff exists between control linearity (fast level detection circuit preferred) and jitter (slow level detection circuit preferred). The design approach followed usually is to aim for low jitter at the expense of poor control linearity. Compensation techniques are then applied to improve control linearity [1], [4], [7], [10].

In Section III, a new, alternative level detection concept is introduced that allows low jitter to be achieved *without* deterioration of the relaxation oscillator's intrinsically high control linearity. Instead of aiming to *instantly* reverse the capacitor current upon a threshold level crossing, a differential pair is used to *gradually* turn on the capacitor's charge current. Section V shows that this effectively implements a low-pass filtering of the threshold level noise by the oscillator's timing capacitor, thus decreasing the contribution of threshold level noise to jitter. As will be explained in Section IV, this approach does not deteriorate the control linearity. Section VI deals with the practical implementation of the so-called coupled sawtooth oscillator and Section VII presents the experimental results.

II. CONVENTIONAL RELAXATION OSCILLATOR

A. Control Linearity

Ideally, the frequency of oscillation is linearly dependent on the control current in the relaxation oscillator. In practice, the
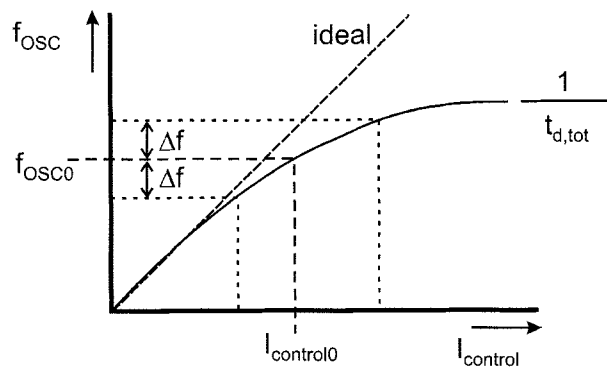
Fig. 2. Nonlinear control characteristic of the relaxation oscillator.

level detection circuitry exhibits a certain delay t_d, due to its limited bandwidth. In first order, the delay t_d is independent of the control current $I_{control}$, such that we can write

$$f_{osc} = \frac{1}{T_{osc0} + t_{d,tot}} = \frac{1}{\frac{2 \cdot C \cdot (V_H - V_L)}{I_{control}} + 4 \cdot t_d}. \quad (1)$$

T_{osc0}, $t_{d,tot}$, and t_d are defined in Fig. 1. Fig. 2 shows a plot of the nonlinear control characteristic that asymptotically approaches its maximum value of $1/t_{d,tot}$ [4].

The control nonlinearity results in distortion in a frequency (de)modulation application, e.g., when the oscillator is used for FM demodulation, it gives rise to second-order distortion [1]:

$$HD_2 = \frac{t_{d,tot} \cdot \Delta f}{2} \quad (2)$$

in which Δf is the frequency sweep (see Fig. 2) and $t_{d,tot}$ is the total delay occurring in one period of oscillation (see Fig. 1). Notice that the distortion in independent of the oscillation frequency.

According to (2), the total delay $t_{d,tot}$ must be made small in order to minimize HD_2. Unfortunately, this increases the jitter of this type of oscillator, as will be shown next.

B. Jitter

The primary contributors to the relaxation oscillator's jitter are the noise current i_n flowing into the capacitor and the noise voltage v_n present in series with the threshold level (see Fig. 1). The latter is generally the dominant cause of jitter, due to its much larger contributing bandwidth [5]–[7]. Therefore, the calculations will focus solely on the jitter, caused by threshold level noise.

In the circuit of Fig. 1, the threshold level noise v_n is given by the input-referred noise of the comparators and the voltage noise, intrinsically present on the comparator levels V_H and V_L. The variance of the time error, associated with one level crossing, can be calculated as [5]

$$\sigma_{\Delta t}^2 \propto \frac{\sigma_{v_n}^2}{(slope_{Vc})^2} \quad (3)$$

where $\sigma_{v_n}^2$ is the variance of the threshold level noise v_n and $slope_{Vc}$ is the slope of the capacitor voltage. When the noise voltage v_n is white, the successive timing errors Δt are uncor-

related and the variances $\sigma_{v_n}^2$ can be summed into the one-period timing error. In [5], Abidi derives

$$(\sigma_{\Delta T_{osc}})_{v_n} = \alpha \cdot \sqrt{6} \cdot \frac{\sigma_{v_n}}{slope_{Vc}} \quad (4)$$

where α is a constant, valued between 0.5 and 1, depending on the spectral properties of the threshold level noise. The slope of the capacitor voltage is given by $slope_{Vc} = 2(V_H - V_L)/T_{osc}$ (see Fig. 1), resulting in the following expression for the jitter due to threshold level noise v_n:

$$\left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}} \right)_{v_n} = \alpha \cdot \sqrt{1.5} \cdot \frac{\sigma_{v_n}}{(V_H - V_L)}. \quad (5)$$

In the case that the threshold noise voltage v_n is white, its variance is given by the product

$$\sigma_{v_n}^2 = S_{v_n} \cdot B_n \quad (6)$$

where S_{v_n} is the power spectral density of the white threshold noise and B_n is its noise bandwidth.

Now suppose the comparator's noise bandwidth B_n is set by a dominating low-pass single-pole RC combination, with associated time constant τ_{comp}. Then B_n is given by

$$B_n = \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{1}{4RC} = \frac{1}{4\tau_{comp}}. \quad (7)$$

Assuming that the comparator's delay t_d (see Fig. 1) can be approximated by its time constant τ_{comp}: $t_d \approx \tau_{comp}$, we can rewrite (7) as

$$B_n = \frac{1}{4\tau_{comp}} = \frac{1}{4t_d} \underset{(Fig.1)}{=} \frac{1}{t_{d,tot}}. \quad (8)$$

Combining (5), (6), and (8) gives the final expression for the jitter due to threshold level noise:

$$\left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}} \right)_{v_n} = \alpha \cdot \sqrt{1.5} \cdot \frac{\sqrt{S_{v_n} \cdot \frac{1}{t_{d,tot}}}}{(V_H - V_L)}. \quad (9)$$

Thus, in the conventional relaxation oscillator, the rms jitter is inversely proportional to the square root of the delay $t_{d,tot}$, whereas the distortion is proportional to $t_{d,tot}$ [see (2)]. This reveals the tradeoff between control linearity and jitter in the conventional relaxation oscillator.

III. PRINCIPLE OF THE COUPLED SAWTOOTH OSCILLATOR

Low jitter *and* high control linearity cannot be achieved simultaneously in a conventional relaxation oscillator, as shown previously. In this section, an alternative implementation of the level crossing detection is proposed, allowing for the achievement of *both* low jitter *and* good control linearity.

In the coupled sawtooth oscillator, one period of oscillation is determined by the sum of the durations of solely rising slopes of capacitor voltage waveforms. The falling edges do not contribute to the definition of the period of oscillation. The only condition to be satisfied is that a capacitor must be discharged in time to enable its participation in the next period of oscillation. The minimum number of capacitors needed in such a timing scheme is two, resulting in the waveforms of Fig. 3.
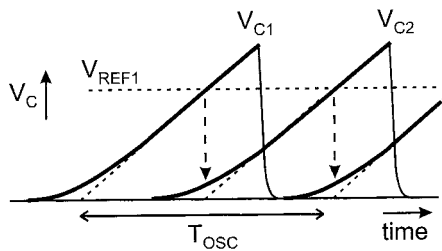
Fig. 3. Capacitor voltage waveforms appearing in the coupled sawtooth oscillator.
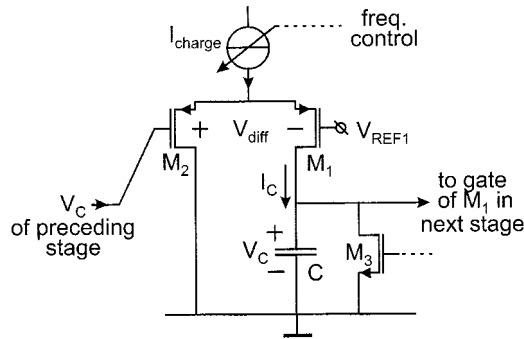

Fig. 4. Basic implementation of one stage in the coupled sawtooth oscillator.

Fig. 5. Capacitor's current and voltage waveforms in one stage of the coupled sawtooth oscillator during startup of a ramp.

IV. CONTROL LINEARITY OF THE COUPLED SAWTOOTH OSCILLATOR

Fig. 5 explains the preservation of control linearity in the coupled sawtooth oscillator. The solid curve in the upper graph of Fig. 5 shows the relationship between the drain current of M_1 (or, equivalently, the capacitor current I_C) and the differential voltage V_{diff} (see Fig. 4). The dashed curve in the upper graph of Fig. 5 depicts the situation in which the differential pair $M_{1,2}$ acts as an instantaneous switch (similar to the functionality of the level detection circuit in an idealized conventional relaxation oscillator). The lower graph in Fig. 5 shows the resulting V_C curves that are calculated by integrating the I_C curves. This integration is mathematically correct; although the horizontal axis of the upper graph is a voltage, it is equivalent to time. This can be concluded from Fig. 3; the capacitor voltage waveform (that drives the differential pair) is a linear function of time the moment it crosses V_{REF1}.

The linearity in the oscillator's control characteristic $f_{\text{osc}}(I_{\text{charge}})$ is guaranteed when the solid V_C curve overlaps the dashed V_C curve in their joint linear parts (point S in the lower graph of Fig. 5), irrespectively of the value of I_{charge}. This condition is guaranteed if areas *I* and *II* in Fig. 5 are equal for each value of I_{charge}. This is indeed the case because the differential pair's transfer function between the input voltage V_{diff} and the drain current of M_2 is point symmetrical in the point $V_{\text{diff}} = 0$ V, irrespective of the value of the tail current I_{charge}.

The control linearity of the coupled sawtooth oscillator is ultimately limited only by the following.

- K-mismatch in the differential pair, giving rise to a current-dependent offset voltage. This current-dependent offset voltage can be thought of as added to the threshold voltage level V_{REF1}.
- Threshold-voltage mismatch in the current mirror that supplies the tail current I_{charge} to the differential pair (see Fig. 4), giving rise to a current-dependent mirror ratio.
- Charge injection. When a stage's capacitor discharges, the source voltage of the differential pair in the following stage is lowered abruptly. This may cause charge injection onto the gate-bias rail of the tail current sources, affecting the charge current in some other stage. If the amount of

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The charging of a capacitor starts whenever the previous capacitor voltage ramp reaches the vicinity of the threshold level V_{REF1} (which is the equivalent of the threshold levels V_H and V_L in Fig. 1). The crucial difference between the coupled sawtooth oscillator and the conventional relaxation oscillator is that the decision to start a new capacitor voltage ramp is not taken *quickly*, but rather as *slowly* as possible. By allowing each capacitor voltage to *traverse* the threshold level V_{REF1}, a trajectory is created around the threshold level that is used to *gradually* start up a new ramp.

In [13], a relaxation oscillator is described whose period of oscillation is also determined solely by rising slopes of capacitor voltages. However, it uses a "classical" level detection circuit and thus has a design tradeoff between control linearity and jitter similar to the conventional relaxation oscillator.

In the coupled sawtooth oscillator, a differential pair implements the mechanism by which a new ramp is started gradually. Fig. 4 shows the basic implementation of one of the multiple stages in the coupled sawtooth oscillator. The differential pair $M_{1,2}$ converts the voltage difference V_{diff} between the capacitor voltage of the preceding stage and the threshold-level V_{REF1} into the charge current for the capacitor. The gate of transistor M_1 is connected to a reference voltage V_{REF1}. The gate of transistor M_2 is the control gate and it is connected to the capacitor in the preceding stage of the oscillator. Transistor M_3 discharges the capacitor; its gate control is discussed in Section VI. The frequency of oscillation is controlled by the current I_{charge}.

The next section focuses on the control linearity. It will be shown that the gradual startup of a capacitor voltage ramp does not harm the control linearity of the oscillator. Later sections derive the jitter expressions and explain its reduction, compared to the conventional relaxation oscillator.
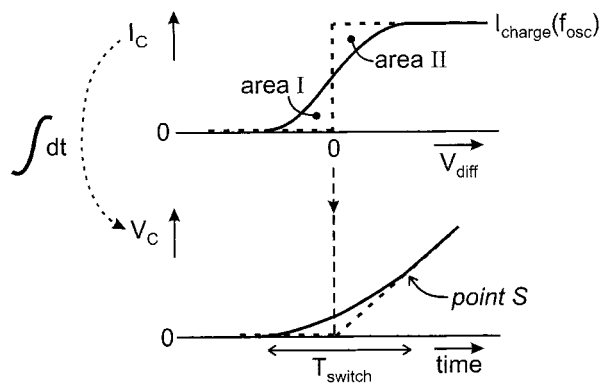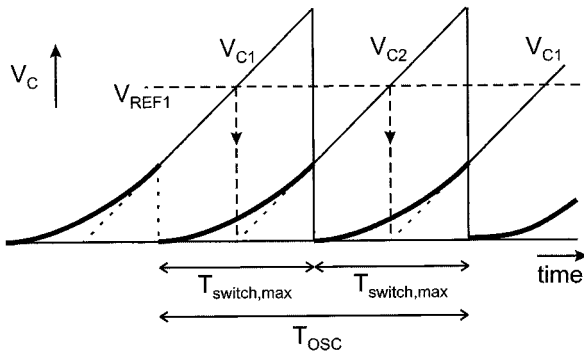
Fig. 6. Allowable maximum switching time $T_{\text{switch,max}}$ of the differential pairs.

injected charge is dependent on I_{charge} (for example, because parasitic capacitances change), it introduces control nonlinearity.

A quantitative analysis of the effect of transistor mismatches on control linearity is given in [19].

As explained by means of Fig. 5, the point-symmetrical transfer function of the differential pair assures that the oscillator's control linearity is maintained, provided that the input differential voltage of the differential pair is a linear function of time during the switching interval T_{switch}. To assure this, the "curved" start-up intervals of successive capacitor voltage ramps are not allowed to overlap in time. Thus, the maximum allowable T_{switch} in an n-stage coupled sawtooth oscillator is given by

$$T_{\text{switch}_{\max}} = \frac{T_{\text{osc}}}{n}. \tag{10}$$

Fig. 6 illustrates the maximum allowable T_{switch} for a two-stage coupled sawtooth oscillator. Note that V_{C1} is a linear function of time during the start-up intervals of V_{C2} and vice versa.

V. JITTER OF THE COUPLED SAWTOOTH OSCILLATOR

In Fig. 7, the conventional relaxation oscillator [Fig. 7(a)] and the coupled sawtooth oscillator [Fig. 7(b)] are compared, with respect to the timing error that arises due to threshold level noise v_{n}. The figure shows the capacitor voltage waveforms V_{C1} and V_{C2} appearing in two successive stages, during startup of V_{C2}. Fig. 7(a) shows the time error Δt_{trig} that results in case a trigger circuit is used to start a new capacitor voltage ramp. By definition, the time error is proportional (via the slope of the ramp) to the error made in the capacitor voltage. In turn, the capacitor voltage error is given by a sample of the threshold level noise. Thus, we can write for the situation depicted in Fig. 7(a) [5]

$$\sigma^2_{\Delta t_{\text{trig}}} \equiv \frac{\sigma^2_{\Delta V_{\text{C}}}}{(\text{slope}_{\text{Vc}})^2} = \frac{\sigma^2_{v_{\text{n}}}}{(\text{slope}_{\text{Vc}})^2}. \tag{11}$$

Fig. 7(b) shows the situation in the coupled sawtooth oscillator. During the time interval T_{switch} that the differential pair switches on the capacitor's charge current, the noise v_{n} is transferred into a current that is *integrated* (or filtered) by the capacitor. Again, via the slope of the capacitor voltage ramp, the resulting voltage error ΔV_{C2} gives rise to a time error Δt_{saw}.
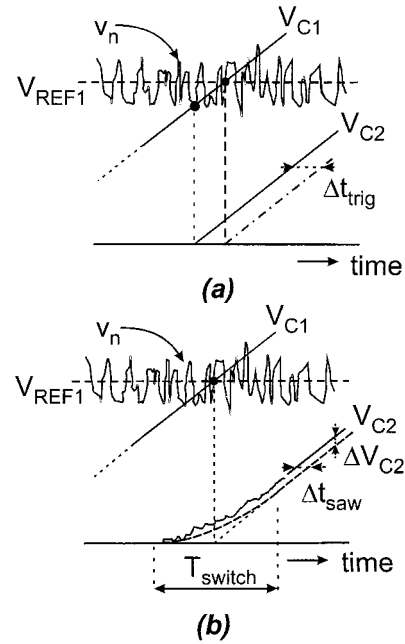

Fig. 7. Comparison of timing errors due to threshold level noise. (a) Conventional relaxation oscillator. (b) Coupled sawtooth oscillator.

However, as will be shown next, unlike in the conventional relaxation oscillator, the variance of the capacitor voltage error is smaller than that of the threshold level noise. As a result, the time error in the coupled sawtooth oscillator [Fig. 7(b)] is significantly smaller than that of the relaxation oscillator [Fig. 7(a)], explaining the improvement in jitter performance of the coupled sawtooth oscillator.

Similar to the relaxation oscillator, the variance of the timing error Δt_{saw} can be expressed as

$$\sigma^2_{\Delta t_{\text{saw}}} = \frac{\sigma^2_{\Delta V_{\text{C}}}}{(\text{slope}_{\text{Vc}})^2}. \tag{12}$$

An expression for the variance $\sigma^2 \Delta_{\text{Vc}}$ is derived from the expression of the capacitor voltage error ΔV_{C} [see Fig. 7(b)] that appears when the differential pair has fully switched:

$$\Delta V_{\text{C}} = \frac{1}{C} \cdot \int_{T_{\text{switch}}} g_m(\tau) \cdot v_{\text{n}}(\tau) d\tau \tag{13}$$

in which g_m is the differential pair's transconductance between input differential voltage and M_1's drain current (see Fig. 4) and v_{n} is the threshold level noise. To simplify the calculations, the assumption is made that the transconductance g_m is constant during switching of the differential pair and equals its maximum value g_{m0}. It can be shown easily that g_{m0} is related to the differential pair's switching time T_{switch} via the approximation

$$T_{\text{switch}} \approx \frac{C}{g_{m0}}. \tag{14}$$

Substituting (14) into (13) gives the following expression for the capacitor voltage error ΔV_{C} that results when the differential pair has fully switched on the capacitor's charge current:

$$\Delta V_{\text{C}} = \frac{1}{T_{\text{switch}}} \cdot \int_{T_{\text{switch}}} v_{\text{n}}(\tau) d\tau. \tag{15}$$
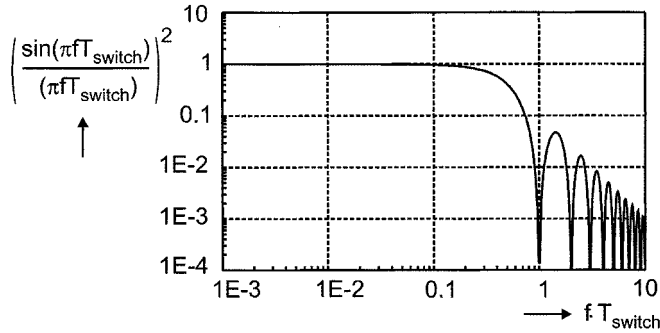
Fig. 8.   Squared sinc function in (17) as a function of $f \cdot T_{\text{switch}}$.

This error ΔV_{C} can be thought of as a sample of a continuous time random variable, given by

$$\Delta V_{\text{C}}(t) = \frac{1}{T_{\text{switch}}} \int_{t-T_{\text{switch}}}^{t} v_{\text{n}}(\tau)d\tau. \tag{16}$$

This continuous-time expression allows us to calculate the power spectral density $S_{\Delta V_{\text{C}}}(f)$ associated with ΔV_{C} by Fourier transforming the continuous-time expression $\Delta V_{\text{C}}(t)$, giving [22]

$$S_{\Delta V_{\text{C}}}(f) = S_{v_{\text{n}}} \cdot \left(\frac{\sin\left(\pi f T_{\text{switch}}\right)}{\pi f T_{\text{switch}}} \right)^2 \tag{17}$$

where $S_{v_{\text{n}}}$ is the power spectral density of the white-noise voltage v_{n}. Fig. 8 shows a log–log plot of the squared sinc function in (17). One can conclude from this plot that only the low-frequency portion of the threshold level noise v_{n} contributes significantly to the power spectral density $S_{\Delta V_{\text{C}}}(f)$. The larger the differential pair's switching interval T_{switch}, the more effective is this low-pass filtering.

The variance $\sigma_{\Delta V_C}^2$ of the capacitor voltage error ΔV_{C} is given by the integration of the power spectral density $S_{\Delta V_{\text{C}}}(f)$ over all frequencies, which gives

$$\sigma_{\Delta V_C}^2 = \frac{1}{2} \cdot S_{v_{\text{n}}} \cdot \frac{1}{T_{\text{switch}}}. \tag{18}$$

Comparing (18) with (6) [with B_{n} given by $1/t_{\text{d,tot}}$ (8)], the improvement is apparent: in the coupled sawtooth oscillator, the effective bandwidth by which threshold level noise contributes to the variance of the capacitor voltage error is given by $1/(2 \cdot T_{\text{switch}})$. This bandwidth is much smaller than the noise bandwidth $1/t_{\text{d,tot}}$ of the level detection circuitry in the conventional relaxation oscillator [see (8)]. Thus, by gradually starting up a capacitor voltage ramp using a differential pair, the oscillator exploits its own capacitor to effectively reduce the bandwidth by which the threshold level noise contributes to the capacitor voltage error and thus to jitter.

Now suppose that a coupled sawtooth oscillator exists of n equal stages, such that the sum of n positive capacitor voltage ramps forms one single period of oscillation. Then the following expression for the one-cycle jitter can be easily derived:

$$\left(\frac{\sigma_{\Delta T_{\text{osc}}}}{T_{\text{osc}}} \right)_{\text{saw},v_{\text{n}}} = \frac{\sqrt{\frac{S_{v_{\text{n}}}}{2} \cdot \frac{1}{n} \cdot \frac{1}{T_{\text{switch}}}}}{V_{\text{REF1}}}. \tag{19}$$

Notice that maximizing the differential pair's switching interval T_{switch} reduces the jitter. The maximum T_{switch} that can be chosen in an n-stage coupled sawtooth oscillator (whilst still preserving control linearity) is given by expression (10). Substituting (10) into (19) gives the final expression for the minimum achievable jitter due to threshold level noise of the coupled sawtooth oscillator:

$$\left(\frac{\sigma_{\Delta T_{\text{osc}}}}{T_{\text{osc}}} \right)_{\text{saw},v_{\text{n}}} = \frac{\sqrt{S_{v_{\text{n}}} \cdot \frac{f_{\text{osc}}}{2}}}{V_{\text{REF1}}}. \tag{20}$$

An important conclusion can be drawn from (20): the jitter due to threshold level noise is independent of the number of stages n. The reason for this is that with an increasing number of stages, the slope of the ramps increases, which compensates for the increasing number of threshold level crossings and the decreasing value of T_{switch}. Expression (20) shows that the jitter due to threshold level noise is proportional to a noise-to-signal ratio of the threshold level V_{REF1}.

The jitter ratio due to threshold level noise between the coupled sawtooth and relaxation oscillators can be found by dividing (20) with (9) (under the assumption that both oscillators have equal values of T_{osc}, $V_{\text{Cmax}}(V_H - V_L = V_{\text{REF1}})$, and furthermore assuming that $\alpha\sqrt{1.5} \approx 1$):

$$\left(\frac{\sigma_{\Delta T_{\text{osc,saw}}}}{\sigma_{\Delta T_{\text{osc,relax}}}} \right)_{v_{\text{n}}} = \sqrt{\frac{t_{\text{d,tot}}}{2 \cdot T_{\text{osc}}}}. \tag{21}$$

In this expression, $t_{\text{d,tot}}$ is the total delay, added to one period of oscillation by the level detection circuit in the conventional relaxation oscillator (see Fig. 1). This jitter ratio is independent of the number of stages used in the coupled sawtooth oscillator to generate one period of oscillation. As a good control linearity implies a total delay $t_{\text{d,tot}}$ that is much smaller than T_{osc}, it is clear from (21) that the jitter of the coupled sawtooth oscillator is much smaller that that of the conventional relaxation oscillator, when compared at equal control linearity.

The emphasis in this paper has been on the jitter due to threshold level noise, since it is the dominant cause of jitter in the conventional relaxation oscillator. To be complete, however, the jitter due to noise on the charge current I_{charge} (see Fig. 4) can be derived as [19]

$$\left(\frac{\sigma_{\Delta T_{\text{osc}}}}{T_{\text{osc}}} \right)_{\text{saw},i_{\text{n}}} = \frac{\sqrt{S_{i_{\text{n}}} \cdot \frac{f_{\text{osc}}}{2}}}{I_{\text{charge}}} \tag{22}$$

in which $S_{i_{\text{n}}}$ is the power spectral density of the current noise, associated with I_{charge}.

VI. IMPLEMENTATION

Fig. 9 shows the implementation of the coupled sawtooth oscillator, consisting of a ring of four identical stages. One period of oscillation is determined by the sum of the four rising ramps. Fig. 9(a) shows the current biasing scheme of all stages. Fig. 9(b) shows a single stage (stage number "i"). The numbering of the signals in italics applies to stage number one.

The differential pair $M_{1,2}$ in Fig. 9(b) controls the gradual startup of the capacitor voltage ramp. The comparator in
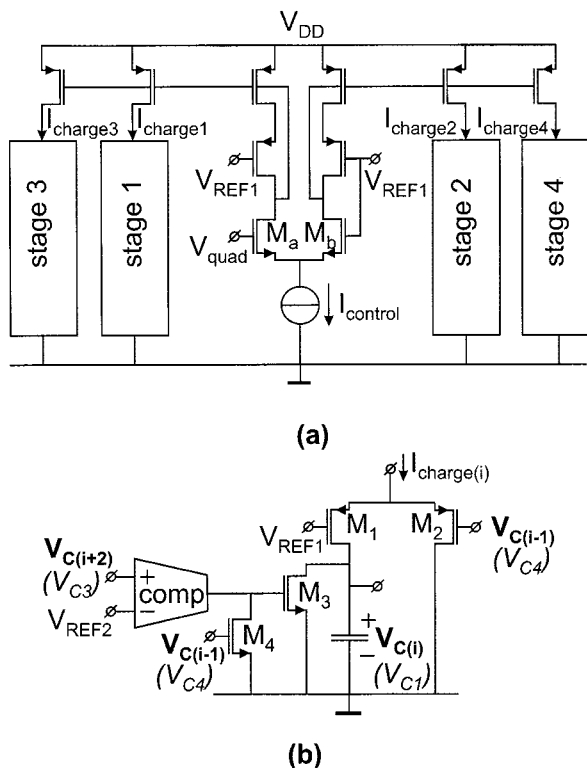
(a)

(b)

Fig. 9. (a) The four-stage coupled sawtooth oscillator and (b) the circuit schematic of a single stage number "i". The signals in italics apply to stage number 1. The interconnect between stages in (a) follows from the signal numbering in (b).

Fig. 9(b) (a simple one-stage operational transconductance amplifier) initiates the discharging of the capacitor through transistor M_3. Transistor M_4 deactivates the discharge switch M_3. It assures that the capacitor is "released" in time for the generation of the next rising ramp (see Fig. 10). Transistors $M_{3,4}$ and the comparator are only involved with the discharge intervals of the capacitor and thus do not add jitter. The resulting waveform timing is depicted in Fig. 10.

The oscillator generates two square-wave output signals that are ideally in quadrature to each other. The edges of the first output signal are defined by the rising slopes in stages 1 and 3 and the edges of the other output signal are defined by the those in stages 2 and 4. By splitting the oscillator's control current I_{control} in two halves by means of the differential pair $M_{a,b}$ [see Fig. 9(a)], the phase difference between the two quadrature signals can be altered by means of the voltage V_{quad}. Two edges can be adjusted to exactly 90°; the position of the other edges have a fixed phase relation determined by stage matching. Although the periodicity of each of the individual outputs is not subject to fixed pattern jitter, the quadrature relationship ultimately will be, because the edges of the quadrature signals are derived from different stages. Another advantage of splitting I_{control} is that the gate rails of the two 1 : 1 pMOS current mirrors are separated. Any charge injection onto the gate bias rail of the pMOS current mirror during a capacitor's discharge cannot affect the current I_{charge} in the "active" stage.

The frequency of oscillation is given by

$$f_{\text{osc}} = \frac{I_{\text{control}}}{2 \cdot V_{\text{REF1}} \cdot C_{\text{tot}}} \quad (23)$$
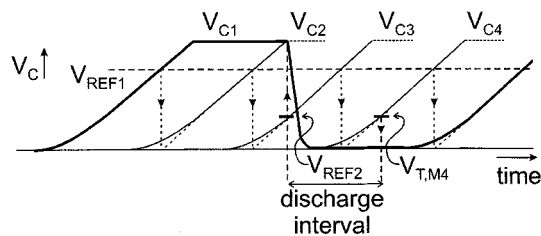

Fig. 10. Capacitor voltage waveforms appearing in the circuit of Fig. 11. V_{T,M_4} refers to the threshold voltage of M_4 in Fig. 11(b).
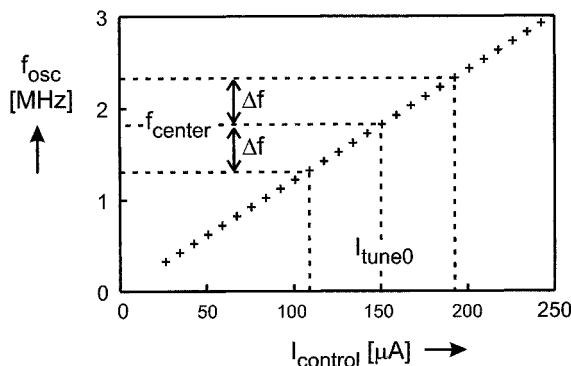

Fig. 11. Measured $f_{\text{osc}}(I_{\text{control}})$ of one IC.

in which C_{tot} represents the sum of the capacitors in the four stages.

As the frequency of oscillation is relatively low in our application, we can use a comparator to drive the gate of M_3 [see Fig. 9(b)], giving maximum experimental controllability over the discharge level V_{REF2}. If the aim is a maximum operating frequency, it is probably better to use a six-stage coupled sawtooth oscillator; it can be shown that using six stages allows one to remove the comparator and drive the gate of M_3 directly with $V_{\text{C}(i+2)}$. The only parasitic node then remaining in a stage is the source connection of the differential pair $M_{1,2}$.

VII. EXPERIMENTAL RESULTS

The coupled sawtooth oscillator has been realized in a standard 0.8-μm double-metal single-poly CMOS process. The circuit is designed for application in a HiFi FM-sound (de)modulation PLL in a VCR with a sound-carrier frequency of 1.8 MHz. Fig. 11 shows the measured $f_{\text{osc}}(I_{\text{control}})$. By polynomial fitting the data in Fig. 11 around $f_{\text{osc0}} = 1.8$ MHz, the distortion in the $I_{\text{control}}(f_{\text{osc}})$ relationship is calculated with $\Delta f = 500$ kHz (!), giving $HD_2 = -67$ dB and $HD_3 = -90$ dB. This is more than sufficient for the application, where Δf is only 50 kHz. Fig. 12 shows similarly measured distortion figures of ten realizations of the oscillator. The cause of the distortion and the variations in it can be explained by V_{T} mismatches in the pMOS current mirror of Fig. 11(a) [19].

Fig. 13 shows the measured phase noise ($f_{\text{osc}} = 1.5$ MHz, $I_{\text{control}} = 120$ μA, $I_{DD} = 360$ μA, $L(10$ kHz$) = -102$ dBc/Hz). In this phase-noise measurement, the external applied noise impedance at the threshold level V_{REF1} is 24 kΩ and the external noise impedance applied at the sources of $M_{a,b}$ in Fig. 9(a) is 1.35 kΩ. The -30 dB/dec portion of the phase-noise spectrum is caused by the $1/f$ noise of the
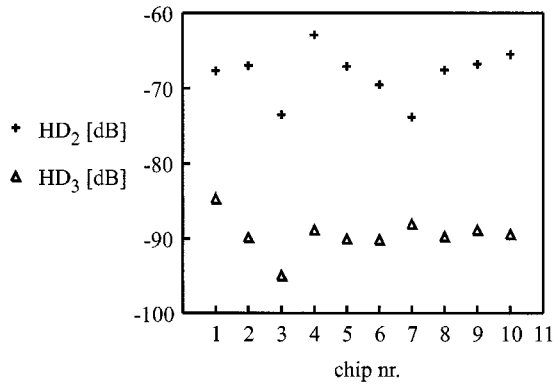
Fig. 12.   Measured distortion of the control characteristic of ten ICs. $f_{osc0} = 1.8$ MHz and $\Delta f = 500$ kHz.
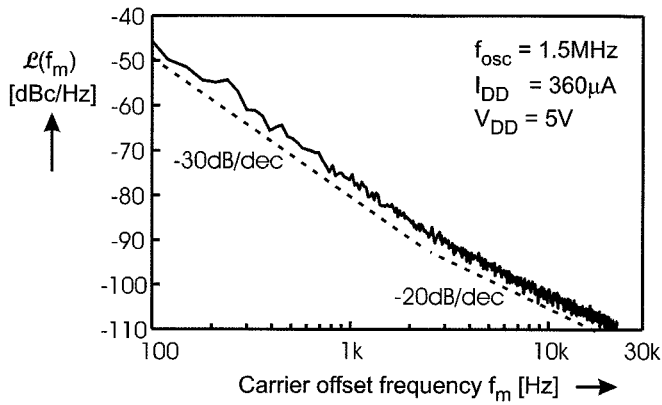

Fig. 13.   Measured phase noise. $f_{osc} = 1.5$ MHz.

TABLE I
CIRCUIT CHARACTERISTICS

V_{DD}	5V
V_{REF1}	2V
V_{REF2}	1.2V
C_{TOT}	20pF
HD$_2$ I$_{CONTROL}$(f_{OSC}) (Δf=500kHz f_{OSC}=1.8MHz)	-67dB (typ)
HD$_3$ I$_{CONTROL}$(f_{OSC}) (Δf=500kHz f_{OSC}=1.8MHz)	-90dB (typ)
L(10kHz) @ f_{OSC}=1.5MHz	-102dBc/Hz
I$_{DD}$ @ f_{OSC}=1.5MHz	360µA

pMOS current mirror transistors. It can be reduced by applying the switched-bias technique to these transistors [20] or by periodically interchanging the transistors in the mirror [19]. Using a formula derived in [19] and [21]

$$L(f_m) = \left(\frac{f_{osc}}{f_m^2} \cdot \left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}} \right)^2 \right) \Rightarrow \frac{\sigma_{\Delta T_{osc}}}{T_{osc}} = \sqrt{\frac{L(f_m) \cdot f_m^2}{f_{osc}}} \tag{24}$$

where $L(f_m)$ is the common measure for phase noise, f_m is the carrier offset frequency, and $(\sigma_{\Delta T_{osc}}/T_{osc})$ is the ppm rms jitter. The portion of the phase-noise spectrum that has a -20 dB/dec slope (see Fig. 13) can be translated into a 65-ppm rms cycle jitter. Compared to calculations, the jitter due to threshold level noise is only 16 ppm [calculated using (19) with $S_{v_n} = 4kT \cdot 24$ kΩ and $T_{switch} = (1/14) \cdot T_{osc}$, which in turn is based on (14) and the particular transconductance of the differential pair]. However, the theoretical jitter due to noise on the charge current was found to be 60 ppm, using (22) where S_{i_n} is set by the noise of the mirror transistors [the top-row transistors in Fig. 9(a)] giving a total predicted jitter of $\sqrt{60^2 + 16^2} = 62$ ppm, which agrees well with the measured value. Nevertheless, it shows that there is room for optimization; by sacrificing some swing across the capacitors, the voltage headroom of the transistors in the current mirror can be significantly increased, thus reducing their contribution to jitter.

It is interesting to calculate the amount of threshold level noise that would be required to give a similar 60-ppm contri-

bution to jitter. It can be calculated with (19) by again using $T_{switch} = (1/14) \cdot T_{osc}$, giving an equivalent resistor value of 400 kΩ. If this *same* amount of threshold noise is present in a relaxation oscillator that has the *same* control nonlinearity as specified in Table I and the *same* capacitor voltage swing, its rms jitter due to threshold level noise would be a factor 15 larger than that of the coupled sawtooth oscillator [calculated by using (2) and (9)]. This has been verified by simulation [23]. Table I summarizes the circuit characteristics including measurement results.

A commonly used figure-of-merit (FOM) for comparing the phase-noise performance of different oscillators is given by

$$\text{FOM} = 10 \cdot \log \left(\frac{f_{osc}^2}{f_m^2 \cdot L(f_m)} \cdot \frac{1}{P_{diss}} \right)$$
$$\underset{\text{eq.(24)}}{=} 10 \cdot \log \left(\frac{T_{osc}}{\sigma_{T_{osc}}^2} \cdot \frac{1}{P_{diss}} \right) \tag{25}$$

in which P_{diss} is the dissipated power in the core of the oscillator. In [1], an FM demodulator is presented that uses a well-designed low-noise relaxation oscillator that utilizes a compensation circuit to increase control linearity. Table II gives a performance comparison of that design with our particular realization of the coupled sawtooth oscillator.

Note that the design in [1] has a phase-noise FOM that is about 3 dB better than ours. The reason is that in our particular realization, the jitter is dominated by the noise on the charge current I_{charge}. By substituting the expression for jitter due to noise on I_{charge} (22) in (25) (with $S_{i_n} = 4kT \cdot 2g_{m_{mirror}}$, in which $g_{m_{mirror}}$ is the transconductance of the mirror transistors), one can derive its contribution to the FOM:

$$\text{FOM} = 10 \cdot log \left(\frac{1}{8kT} \frac{V_{GT_{mirror}}}{V_{DD}} \right). \tag{26}$$

Thus, in order to further improve the phase-noise performance of our realization, the effective gate–source voltage of the mirror transistors should be increased. This will come at the expense of the swing across the capacitors, but since the jitter due to threshold level noise is much lower, the overall jitter will improve. In general, one can conclude that for optimal jitter per-

TABLE II
PERFORMANCE COMPARISON

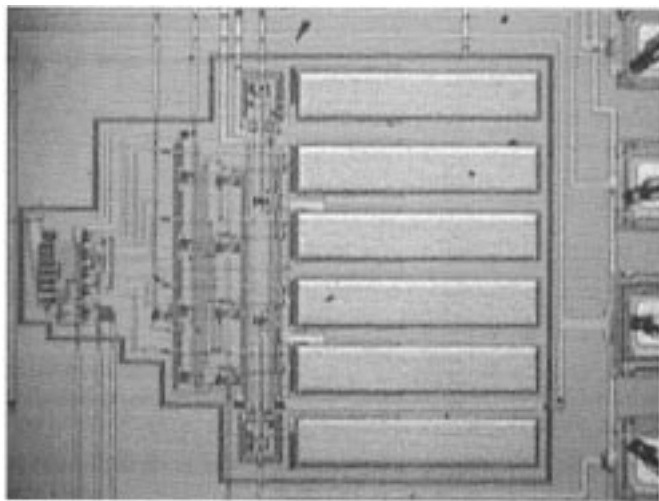|	Sempel [1]	Our design
f_{osc}	6.8MHz	1.5MHz
V_{DD}	5V	5V
I_{charge}	4mA	60μA
L(10kHz)	-110dBc/Hz	-102dBc/Hz
HD$_2$(50kHz) (see eq. 2)	-75dB (after compensation)	-87dB (no compensation)
FOM$_{phase\ noise}$ (see eq. 25)	153.6	150.7

Fig. 14. Chip photograph of the oscillator (1195 μm $\times$ 980 μm).

formance of the coupled sawtooth oscillator, both the jitter due to threshold level noise and noise on the charge current should be taken into account in the minimization of the overall jitter.

Fig. 14 shows a chip photograph. Clearly, one can recognize the oscillator's capacitors. There are six capacitors. The outer two capacitors are not used in the oscillator; they are part of two output buffer circuits that are able to drive 50-Ω loads.

VIII. CONCLUSION

A new current-controlled oscillator principle is presented that combines extremely high control linearity with low timing jitter. Compared with the theoretical jitter of a relaxation oscillator designed with equal oscillation frequency, control linearity, and capacitor voltage swing, the rms jitter due to threshold level noise improves with a factor 15. Better matching between stages would increase the control linearity further and make the advantage over the relaxation oscillator even larger.

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