New Low-Stress PECVD Poly-SiGe Layers for MEMS

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***Abstract*—Thick poly-SiGe layers, deposited by plasma-enhanced chemical vapor deposition (PECVD), are very promising structural layers for use in microaccelerometers, microgyroscopes or for thin-film encapsulation, especially for applications where the thermal budget is limited. In this work it is shown for the first time that these layers are an attractive alternative to low-pressure CVD (LPCVD) poly-Si or poly-SiGe because of their high growth rate (100–200 nm/min) and low deposition temperature (520 °C–590 °C). The combination of both of these features is impossible to achieve with either LPCVD SiGe (2–30 nm/min growth rate) or LPCVD poly-Si (annealing temperature higher than 900 °C to achieve structural layer having low tensile stress). Additional advantages are that no nucleation layer is needed (deposition directly on SiO_2 is possible) and that the as-deposited layers are polycrystalline. No stress or dopant activation anneal of the structural layer is needed since *in situ* phosphorus doping gives an as-deposited tensile stress down to 20 MPa, and a resistivity of 10 $m\Omega$-cm to 30 $m\Omega$-cm. With *in situ* boron doping, resistivities down to 0.6 $m\Omega$-cm are possible. The use of these films as an encapsulation layer above an accelerometer is shown. [958]**

***Index Terms*—Accelerometer, encapsulation, low-stress thick layer, MEMS, plasma-enhanced chemical vapor deposition (PECVD), poly-SiGe.**

I. Introduction

MICROELECTROMECHANICAL systems (MEMS) are used in a wide variety of systems such as accelerometers, gyroscopes, infrared detectors, turbines, etc. A low tensile stress and stress gradient of the structural layer used for the fabrication of these systems is essential since stress and stress gradient can severely affect the device performance. For example, a compressive stress can lead to a bad thermal insulation of bolometers and a stress gradient can produce high displacements in accelerometers [1]–[3]. Also, the thermal budget of the deposition technique is of concern. A high thermal budget increases the processing costs, and limits the number of materials and material combinations that can be located on the substrate prior to processing. Polycrystalline silicon (poly-Si) has been widely used for MEMS applications but its main disadvantage is that it requires a processing temperature higher than 900 °C to achieve the desired physical properties (especially stress) [4].

Polycrystalline silicon germanium (poly-SiGe) [1], [5]–[7] seems to be an attractive alternative to poly-Si as it has similar properties. The presence of germanium reduces the melting point of the silicon germanium alloy and hence the desired physical properties are expected to be realized at lower temperature, allowing the growth on low-cost substrates such as glass and, also, allowing post processing MEMS on top of CMOS [6]. Depending on the germanium concentration and the deposition pressure the transition temperature from amorphous to polycrystalline can be reduced to 450 °C, or even lower, compared to 580 °C for LPCVD poly-Si [8], [9].

Until now, most of the deposition_techniques of poly-SiGe presented in the literature have low deposition rates (2–30 nm/min). The deposition rate can be increased substantially by the use of plasma-enhanced deposition [7]. The high deposition rate might however degrade the physical properties of the deposited layer. It is for example expected that the amorphous to crystalline transition will occur at a higher temperature for a high deposition rate process compared to a low deposition rate process. For a high growth rate process, the time at the deposition temperature is shorter than for a low growth rate process. The thermal budget is therefore decreased and in consequence the film does not crystallize so easily. Also, high growth rate processes often give rise to material frozen into a nonequilibrium state. A growth rate increase of 5 to 10 times is advantageous as it results in a more economic deposition process (less gasses consumed, less heat wasted, faster turn-around time). This is especially important for thick film deposition.

In this article, PECVD poly-SiGe is proposed as a material that can be processed with a high deposition rate (up to 200 nm/min) and excellent MEMS properties at a low deposition temperature. Process results are shown for deposition temperatures between 400 °C and 590 °C, for germanium concentrations from 35% to 61%, and with *in situ* boron or phosphorus doping. The use of poly-SiGe in MEMS applications is demonstrated by using a thick poly-SiGe layer as encapsulation membrane above an accelerometer.

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II. Experimental

The PECVD poly-SiGe layers were deposited in an Oxford Plasma Technology (OPT) Plasma Lab 100 cold wall system. Calibration of the wafer temperature was done in vacuum and at a hydrogen pressure of about 266 Pa (2 torr) with a thermocouple wafer, having seven thermocouples. The silicon gas source for the depositions is pure silane, whereas 10% germane (GeH_4) in hydrogen (H_2) has been used as the germanium (Ge) gas source. For *in situ* doping of the layers 1% diborane (B_2H_6) in H_2 has been used as the boron (B) gas source (p-type SiGe), and 1% phosphine (PH_3) in silane (SiH_4) has been used as the phosphorus (P) gas source (n-type SiGe). Films have been deposited on six-inch silicon wafers having 110 nm or 2.5 μm of PECVD SiO_2 deposited at about 480°C. Wafers with a thick SiO_2 layer were used for determining the stress gradient in the poly-SiGe film. While most of the depositions were done without a nucleation layer, a few tests were performed using a nucleation layer on top of SiO_2. The nucleation layer is PECVD amorphous silicon, which has been deposited for one minute, using a mixture of 1000 sccm hydrogen and 50 sccm silane at 60 W and 133 Pa (1 torr).

The deposition of B-doped SiGe has been done at wafer temperatures of 400 °C, 430 °C, and 590 °C. P-doped SiGe has been deposited at 520 °C, 550 °C, and 590 °C. The deposition pressure has been fixed at 266 Pa (2 torr) and the power at 30 W (except for Section III-A1 where the power was varied). The silane flow rate has been fixed at 30 sccm, whereas germane flows of 100 sccm and 166 sccm have been used. The diborane flow rate was 40 sccm and the phosphine flow rate was 40 sccm, 60 sccm and 80 sccm, respectively.

The Si and Ge concentration have been determined by Rutherford Back Scattering (RBS) and the B and P concentrations by Secondary Ion Mass Spectroscopy (SIMS). Composition and crystallinity of the deposited layers have been determined by using X-ray diffraction (XRD) $\theta - 2\theta$ scans and/or transmission electron microscopy (TEM). The layer thickness has been measured using a mask etch of silicon germanium and measuring the step height using a surface profiler. Stress has been determined by measuring the bow of the wafer before and after depositing the layers using an Eichorn and Hausmann MX 203 stressmeter (it has 2×33 sensors leading to 16 local stress values, which are averaged out to determine the average stress). Sheet resistance has been measured on different locations on the wafer using a four-point probe. Atomic force microscope (AFM) was used to determine the surface roughness. The cantilever deflection has been measured using a UBM laser profilometer.

Patterning PECVD poly-SiGe was done by wet etching ($HNO_3 + \text{buffer HF} + H_2O$) or by plasma etching ($SF_6 + O_2/C_4F_8$). To determine the stress gradient, the underlying sacrificial SiO_2 was removed by vapor HF at 35 °C for 20 min or by wet HF (26 wt.%) for 25 min at room temperature.

III. Results and Discussion

A. *In Situ B-Doped* $Si_{0.31}Ge_{0.69}$ *Deposited at 400* °C

For all the depositions reported in this section, the deposition temperature was 400 °C and a nucleation layer was used.

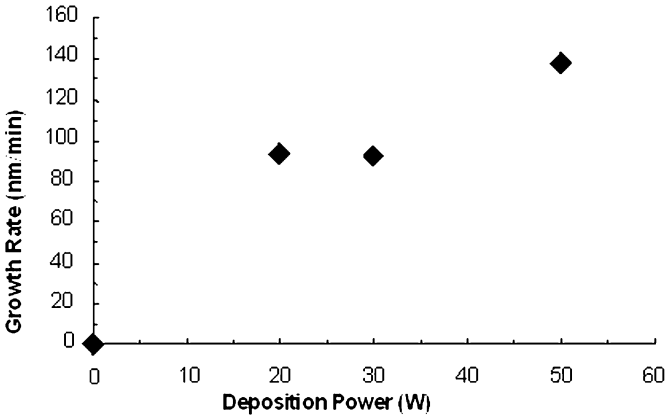


Fig. 1. Dependence of growth rate of *in situ* doped B-$Si_{0.31}Ge_{0.69}$ deposited at 400 °C on deposition plasma power.

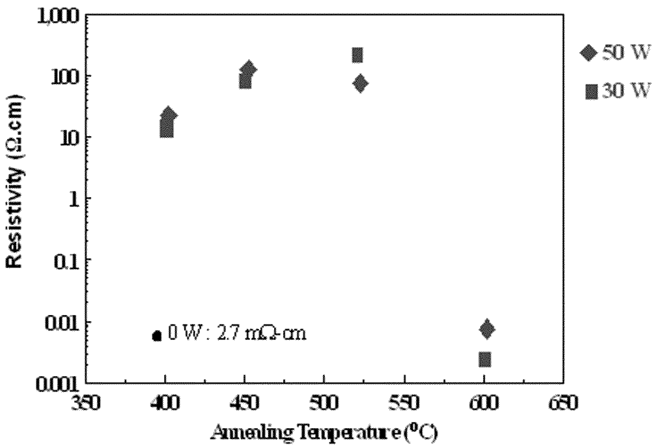


Fig. 2. Effect of annealing temperature and plasma power on resistivity of *in situ* doped B-$Si_{0.31}Ge_{0.69}$ deposited at 400 °C.

The B-doped SiGe films have 69% Ge and a B concentration of 3.75×10^{20} B/cm^3. At this low deposition temperature, an *in situ* deposition of polycrystalline (poly) layers by PECVD is difficult. Crystalline layers are only formed when no power is used (CVD) [10]. One of the reasons is probably the lower deposition rate for CVD compared to PECVD.

1) Influence of Deposition Plasma Power on Growth Rate: The impact of deposition power on the growth rate of *in situ* B-doped poly-$Si_{0.31}Ge_{0.69}$ deposited at 400 °C is displayed in Fig. 1. Increasing the deposition power from 0 W (CVD process) to 50 W changes the growth rate considerably, from 3.7 nm/min to 138 nm/min. However, for a power higher than 20 W (90 nm/min), the increase in the deposition rate is not so significant. Therefore, for all further depositions the deposition plasma power will be fixed to 30 W in order to obtain a high deposition rate at a relatively low plasma power. The higher the plasma power, the harder the bombardment of the film. This bombardment can lead to high stress, defects, *and* amorphous regions, which is not desired.

2) Influence of Power and Annealing Temperature on Crystallinity/Resistance: As grown layers without plasma (0 W) have a low resistivity (2.7 mΩ-cm) (Fig. 2), while deposited layers obtained by PECVD deposition have a higher resistivity (13.7 Ω-cm and 24.2 Ω-cm for 30 and 50 W, respectively). Low

TABLE I
SUMMARY OF THE CHARACTERISTICS OF AS-DEPOSITED, *In Situ* B- AND P-DOPED SiGe LAYERS FOR DIFFERENT FLOW RATES AND DEPOSITION TEMPERATURES (>400 °C)

In situ dopant	P											B	
GeH_4 flow rate [sccm]	166				100	166							
Deposition temp. [°C]	590					550			520			430	590
Doping gas flow [sccm]	80	60	40	40	40	80	40	40	60	40	40	40	
SiGe thickness [μm]	2	~2	~2	10	~2	~8.8	8.5	1.9	~2	9	~2	1.5	2
Stress [MPa]	+79	+100	+70	+110	-140	-45	+20	+38**	-93	+50	+19	-120	+100
Resistivity ρ [mΩ-cm]	25	25	20	17	very high	very high	30	17	very high	18	16	very high	0.64
Ge concentr. (%)	37	44	46		35			43			44	61	56
P or B [10^{20} %]	9	7	6.5	~6.5	6.8	~9	~6.5	~6.5	~7	~6.5	~6.5	~6.5	~6.5
Deposition rate* [nm/min]	200						170	180		180		100	130

* phosphine is in silane while diborane in hydrogen, thus there is more silane for the P-doped layers leading to a higher growth rate.

** underlying SiO_2 layer is annealed twice at 590°C. The stress values of SiGe layers deposited on thick SiO_2 are not corrected for the stress change in SiO_2. However, these stress values represent the maximum stress values for the SiGe layers (see Section III-B4)

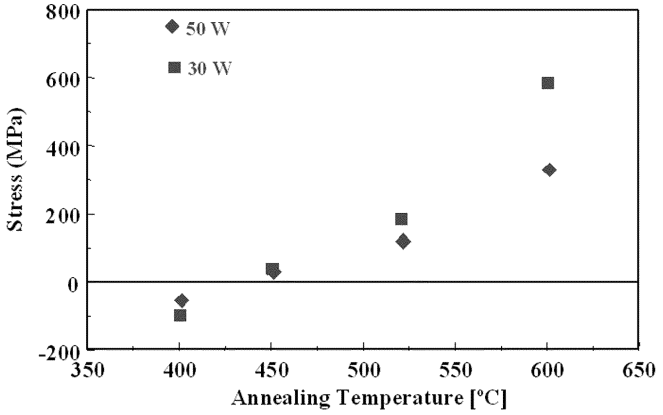


Fig. 3. Dependence of the stress of *in situ* B-doped $Si_{0.31}Ge_{0.69}$ (deposited at 400 °C) on annealing temperature (30 min in N_2 atmosphere) for two plasma power settings, 30 and 50 W, respectively.

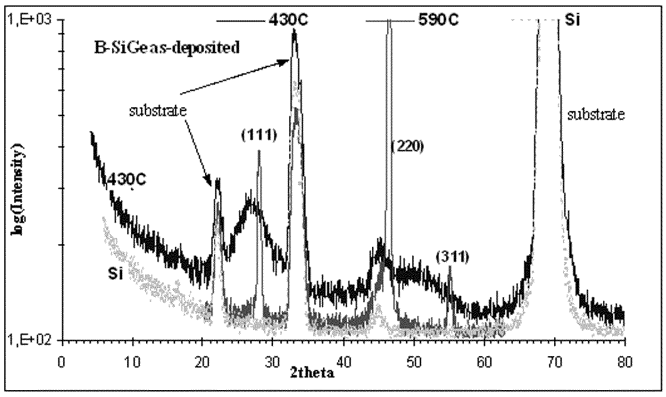
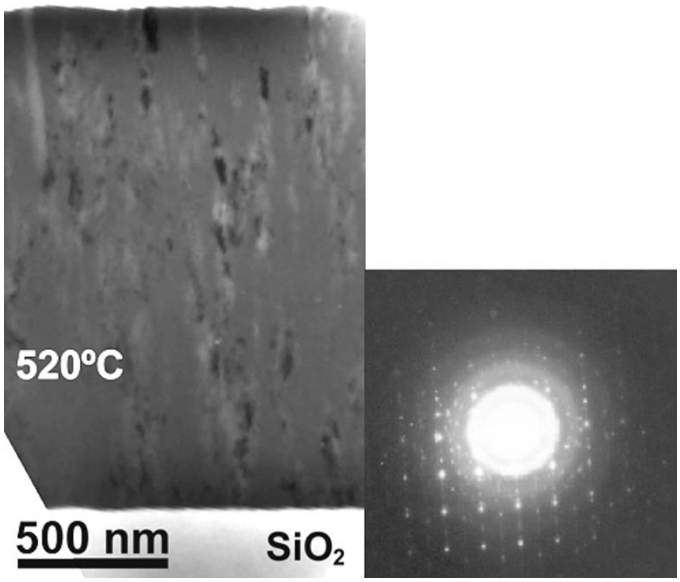


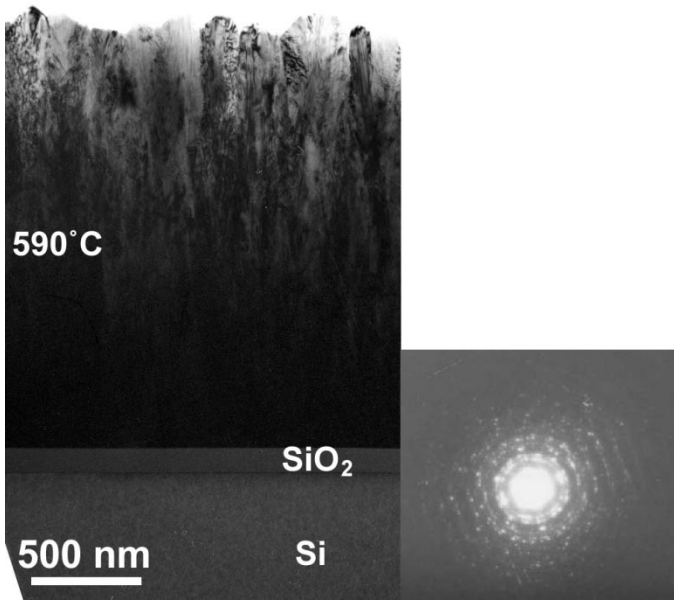
Fig. 4. XRD pattern of B-doped SiGe deposited at 430 °C(amorphous) and 590 °C (polycrystalline).

resistivity for PECVD layers can be reached after subsequent annealing at higher temperature (e.g., at 600 °C: 2.3 mΩ-cm and 8 mΩ-cm for 30 and 50 W, respectively). All anneals were done for 30 min (both at 520 °C and 600 °C) in N_2 atmosphere. Crystallization takes place between 550 °C and 600 °C as it is expected from the resistivity measurements (see later). Resistivity for 0 W is low as this layer is *in situ* crystalline. In fact, the resistivity of this film is similar to the PECVD films annealed at 600 °C which became crystalline after annealing (shown later in Section III-A3).

A direct correlation between the resistivity of *in situ* doped silicon germanium layers and their crystallinity can be expected. A high resistivity is in general observed for amorphous layers, while (partial) crystalline layers have a low resistivity [1], [10] (see Table I together with Fig. 4). Using the plasma power at this low temperature has the disadvantage that the as-deposited layers are amorphous and have a high resistivity.



(a)



(b)

Fig. 5. Cross-section TEM of 2 μm P-doped SiGe layers deposited at (a) 520 °C (predominant amorphous) and (b) 590 °C (polycrystalline) (40 sccm 1% PH_3 in silane).

3) Influence of Annealing Temperature and Plasma Power on Stress: The dependence of stress on annealing temperature and plasma power is demonstrated in Fig. 3. The as-deposited *in situ* B-doped $Si_{0.31}Ge_{0.69}$ layers have a low stress (compressive -100 MPa and -50 MPa for 30 W and 50 W, respectively). However, a tensile stress is preferred as free standing compressive films can buckle. These as-deposited SiGe layers are amorphous and in order to obtain crystallinity an annealing step is necessary. When these layers are annealed at low temperature (450 °C and 520 °C), the stress changes to tensile and remains low. High stress is obtained if the layers are annealed at high temperatures:

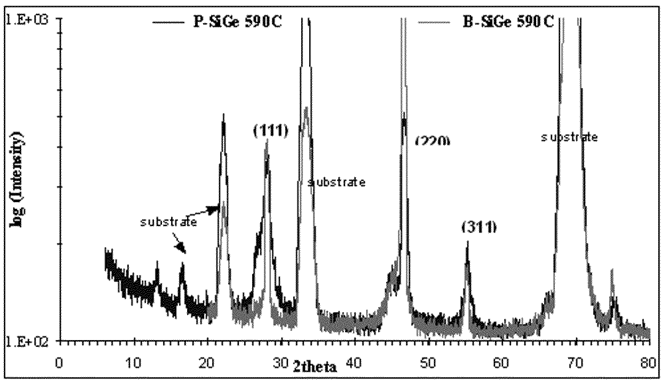


Fig. 6. XRD pattern of as-deposited *in situ* B- and P-doped poly-SiGe at 590 °C.

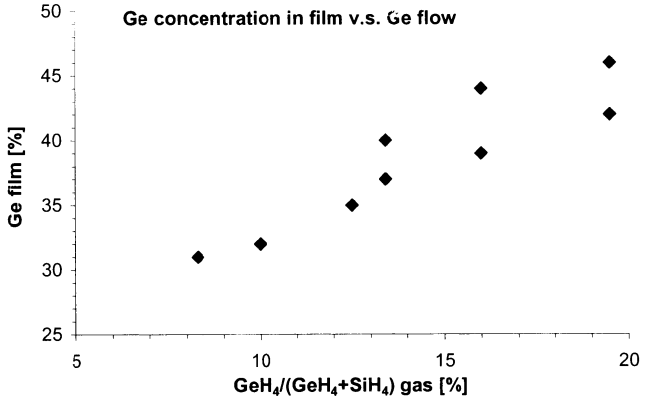


Fig. 7. Variation of Ge concentration in the film by varying the flow of GeH_4 and of the P-doping gas (1% PH_3 in silane).

at 600 °C anneal temperature stress values of $+587$ MPa and $+337$ MPa are measured for 30 and 50 W, respectively. At this temperature however cracks and/or pinholes were formed as seen with the naked eye. This can probably be explained by the crystallization of the films with associated Hydrogen release.

We can conclude that PECVD layers deposited at 400 °C and annealed at low temperature (450 °C to 520 °C) have a low stress but a high resistivity (see Figs. 2 and 3). Low resistivity but high stress and cracks and/or pinholes are obtained for PECVD layers annealed at high temperature (600 °C). These observations can be explained by the fact that the as-deposited amorphous films crystallized during the 600 °C annealing step. If one wants to obtain *in situ* polycrystalline layers with low tensile stress and low resistivity, a higher deposition temperature is necessary.

B. In Situ B- and P-Doped Poly-SiGe Deposited at $T > 400$ °C

For all the PECVD depositions, the quality of the film (resistivity and stress) is not influenced by the presence of the amorphous Si nucleation layer. A nucleation layer can be used for the PECVD deposition, but this is not necessary. This is actually an advantage over other CVD deposition techniques for SiGe where a nucleation layer is needed to eliminate long incubation times for the growth of SiGe on SiO_2 [11]. For all depositions reported in this section no nucleation layer was used. In later

TABLE II
VARIATION OF GE CONCENTRATION IN THE FILM BY VARYING THE FLOW OF GeH_4 (10% GeH_4 IN H_2) AND OF THE P-DOPING GAS (1% PH_3 IN SILANE)

Deposition temp. [°C]	590				550		520	
GeH_4 flow rate [sccm]	166			100	166			
'P' doping gas flow [sccm]	80	60	40	40	80	40	60	40
Stress [MPa]	+79	+100	+70	-140	-45	+38	-93	+19
Resistivity ρ [mΩ-cm]	25	25	20	very high	very high	17	very high	16
Ge concentr. (%)	37	44	46	35		43		44
P concentr. [10^{20} %]	9	7	6.5	6.8	~9	~6.5	~7	~6.5
$\left(\frac{GeH_4}{SiH_4 + GeH_4}\right)_{gas}$ [%]	13.4	16	19.5	12.5				
Total SiH_4 [sccm]	110	90	70	70				
Total GeH_4 [sccm]	17	17	17	10				

work it was found that omitting the a-Si nucleation layer sometimes affects adhesion [Mehta *et al.*, to be published], but this problem was never encountered in this work.

1) Influence of Deposition Temperature: The impact of the deposition temperature on the crystallinity and on the properties of as-deposited PECVD *in situ* doped SiGe is demonstrated in Figs. 4 and 5 and Table I. At 430 °C the B-doped layers are predominantly amorphous, while at 590 °C they are polycrystalline (see Fig. 4). The (111), (220), and (311) are the most important crystalline peaks. Similarly, for P-doped layers, it can be seen from the TEM cross section that at 520 °C the layers are predominant amorphous, while at 590 °C they are fully polycrystalline (see Fig. 5) with columnar grains. The electron diffraction patterns contain rings characteristic of the SiGe crystallographic structure. On the other hand, the SiGe layer deposited at 520 °C is mostly amorphous with some embedded crystals. Similarly, the Ge concentration determines whether an as-deposited layer is, at least partially polycrystalline or not (see Section III-B2). Predominantly amorphous layers are characterized by a high resistivity and a compressive stress (see Table I).

2) Influence of Dopant Type and Ge-Concentration: As-deposited polycrystalline layers deposited at 590 °C are obtained for both types of dopant, boron (40 sccm diborane) or phosphorus (80 sccm phosphine) as shown in Fig. 6. The Ge concentration in the film can be varied by varying the flow of germane (GeH_4) and the flow of the P-doping gas (1% PH_3 in SiH_4), as can be seen in Table II and Fig. 7. The SiH_4 flow is fixed to 30 sccm. As expected, the higher the percentage of $GeH_4/(SiH_4 + GeH_4)$ in the gas mixture, the more Ge in the film.

Germane flow variation

P-doped SiGe layers (40 sccm 1% PH_3 in SiH_4) deposited at 590 °C are amorphous with a compressive stress (-140 MPa) for a 100 sccm GeH_4 flow rate leading to 35% Ge, while these layers are crystalline with a tensile stress ($+70$ MPa) for a 166 sccm GeH_4 flow rate leading to 46% Ge (as can be seen in Table I and Fig. 8).

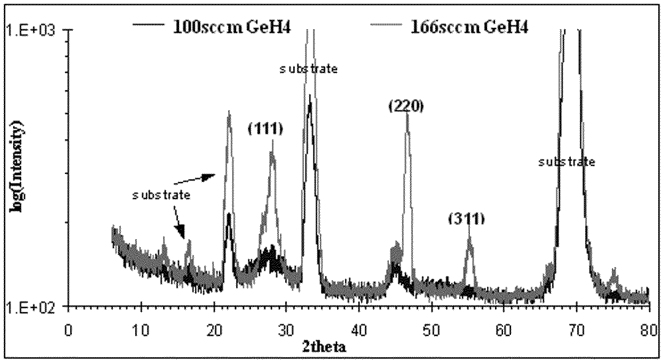


Fig. 8. XRD pattern of as-deposited *in situ* P-doped SiGe deposited at 590 °C. Amorphous layer for 100 sccm GeH_4, while polycrystalline for 166 sccm.

Phosphine flow variation

The concentration of the phosphorus dopant has been varied by changing the phosphine flow (80 sccm, 60 sccm and 40 sccm 1% PH_3 in SiH_4) and by keeping the germane and silane flows constant. Phosphorus concentrations have been determined by SIMS and, for a germane flow of 100 sccm and phosphine flow of 40 sccm, 60 sccm and 80 sccm have been found to be 6.8×10^{20}, 9×10^{20}, 1×10^{21} $\mathrm{Phosphorus/cm^3}$, respectively. For the germane flow of 166 sccm, the SIMS values are shown in Table II.

Changing the P-doping gas flow, and consequently the Ge concentration (see above), has a strong effect on the crystallinity of layers deposited at 520 °C or 550 °C (as can be seen in Figs. 9 and 10), but has no effect on layers deposited at 590 °C [see Table II].

3) Thick P-Doped Layers: When growing a thick film the deposition temperature needed to get a crystalline layer is lowered due to the increased thermal budget. The thicker a layer is, the longer it is exposed to the deposition temperature.

While 2 μm thick P-doped SiGe layers were found to be predominantly amorphous at 520°C [see Fig. 5(a)], 10 μm thick P-doped SiGe layers have been grown (predominantly) polycrystalline at the same deposition temperature (see

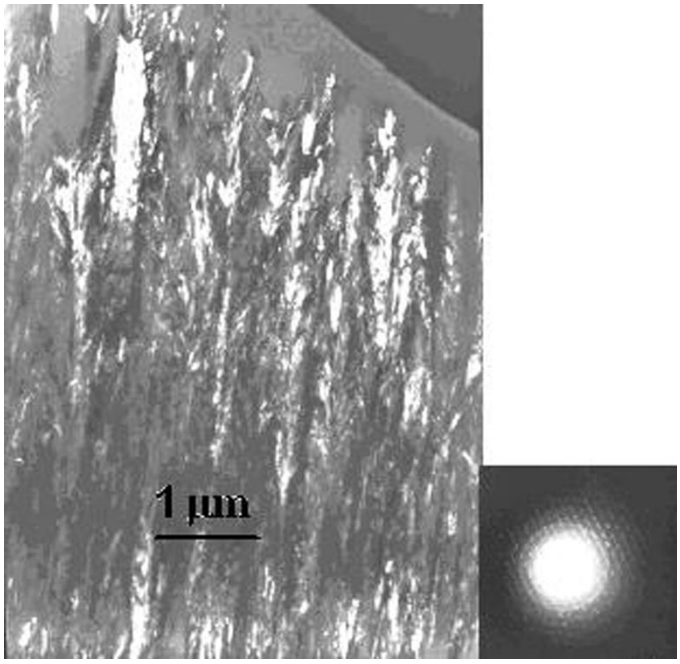


Fig. 9. Cross-section TEM of 9 μm P-doped SiGe layers deposited at 520 °C predominant polycrystalline (40 sccm 1% PH_3 in silane).

Fig. 9). These thick P-doped layers have a low tensile stress ($<+100$ MPa) and low resistivity (18 mΩ-cm).

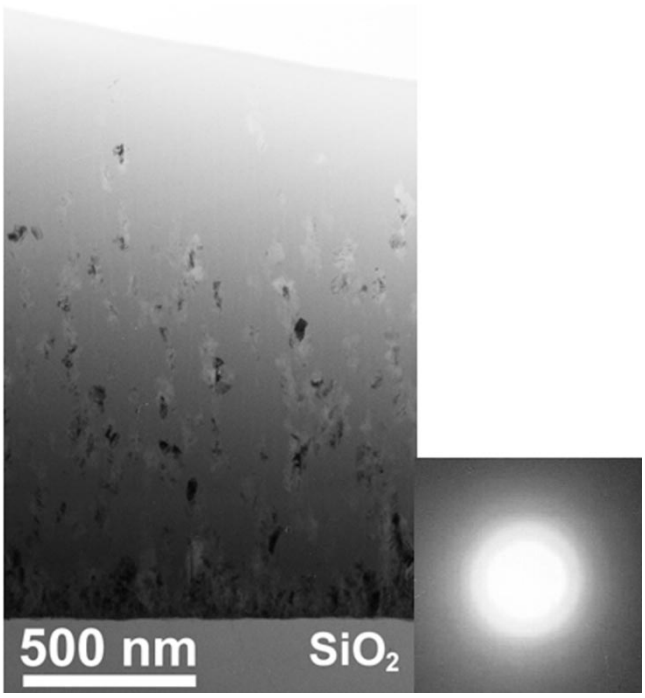
4) Effect of SiO_2 Substrate: The SiGe layers are always deposited on a SiO_2 layer grown at 480 °C. For some of the depositions this SiO_2 layer was annealed at 710 °C or 800 °C prior to SiGe layer deposition to investigate the influence of the substrate on the SiGe layer. The Si-oxide itself seemed to densify somewhat as seen from the stress measurements before ($\sim$25 MPa) and after annealing (37 MPa after 50 min at 710 °C and 53 MPa after 50 min at 800 °C), but this did not have any influence on the SiGe properties. From thickness measurements, no differences between the samples are observed, indicating that the growth rate of the SiGe layer is not influenced by the annealing treatment of the SiO_2. Also, from TEM analysis no significant differences in the morphology of the layer are observed at the level of the SiO_2/SiGe interface, and also no significant variations in the roughness of the SiO_2 layer/SiGe layer interface are observed. This allows us to conclude that annealing of the SiO_2 layer does not influence the SiGe layer characteristics.

C. Characterization

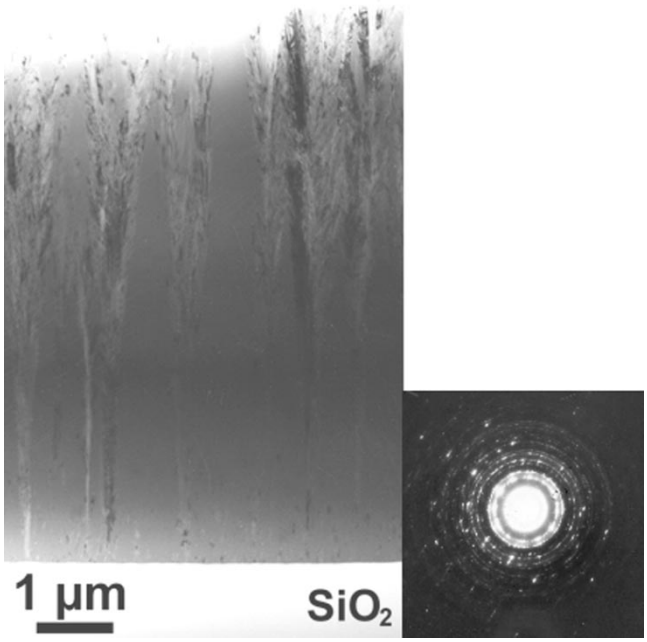
1) Surface Roughness: The surface roughness of the layers depends mainly on the temperature, pressure and thickness. A rather smooth surface is observed, in general, for an amorphous film, while a rough surface is observed for a crystalline film (see Figs. 11 and 12). Also, a thinner film is smoother than a thicker one (see Fig. 13). Note that for both Figs. 12 and 13, the scale is not the same in order to see the surface roughness.

2) Stress Gradient: Patterning of poly-SiGe layers can be done with a standard deep dry reactive ion etching tool using SF_6 and C_4F_8 gasses with an etch rate of 1 μm/min (see Fig. 14) [14]. To release the poly-SiGe microstructures, vapor or wet HF sacrificial etching of the underlying SiO_2 (2.5 μm thick) layer was used (Fig. 15). Unfortunately, SiO_2 residues form during vapor HF etching making most of the structures stick to the bottom of the wafer (Fig. 16). These residues are expected to be similar to the residues found after Si_3N_4 etching by vapor HF [12] as PECVD SiO_2 has built-in N [13]. To eliminate this residue, another type of SiO_2 which does not contain N has to be used (e.g., thermal oxide, TEOS…).

From a cantilever-beam array, the strain gradient is found to be rather high for 1.9 μm thick layers (2.5×10^{-4} μm^{-1}), but



(a)



(b)

Fig. 10. Cross-section TEM of 8.5 μm P-doped SiGe layer deposited at 550 °C (a) mostly amorphous for 80 sccm 1% PH_3 in silane, (b) mostly polycrystalline for 40 sccm 1% PH_3 in silane.

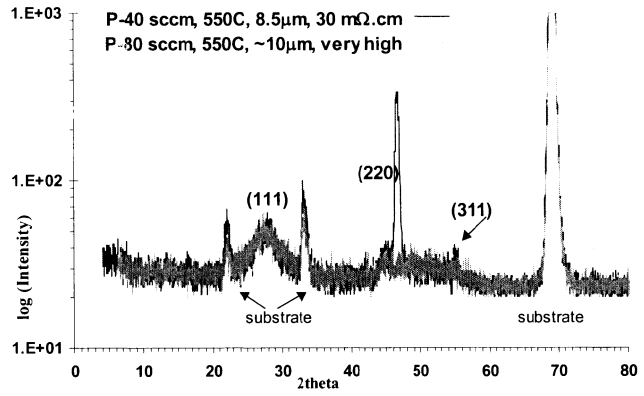


Fig. 11. XRD pattern of P-doped SiGe layer deposited at 550 °C with 40 sccm 1% PH_3 in silane (crystalline peaks) and 80 sccm 1% PH_3 in silane (amorphous).

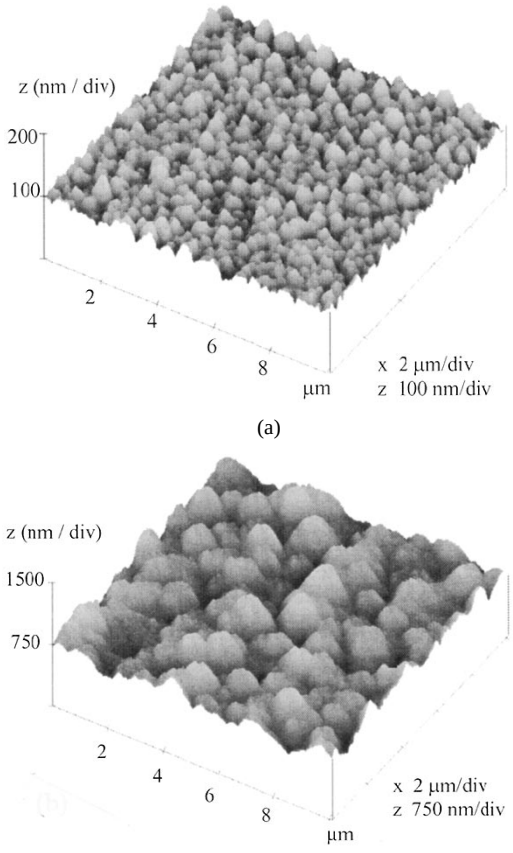


Fig. 12. Topographic AFM images of 8.5 μm P-doped SiGe layer deposited at 550 °C (a) mostly amorphous, RMS = 9.2 nm (80 sccm 1% PH_3 in silane), (b) polycrystalline, RMS = 117 nm (40 sccm 1% PH_3 in silane).

acceptable for 8.5 μm thick layers ($2.5 \times 10^{-5}\ \mu m^{-1}$) as shown in Fig. 17 (both P-doped layers deposited at 550 °C). This strain gradient with the upper part of the layer being more tensile than the lower part may be related to the growth morphology of the poly-SiGe grains [see Fig. 10(b)] [15]. It is expected that by optimising the deposition and annealing conditions further, this strain gradient can be minimized even more.

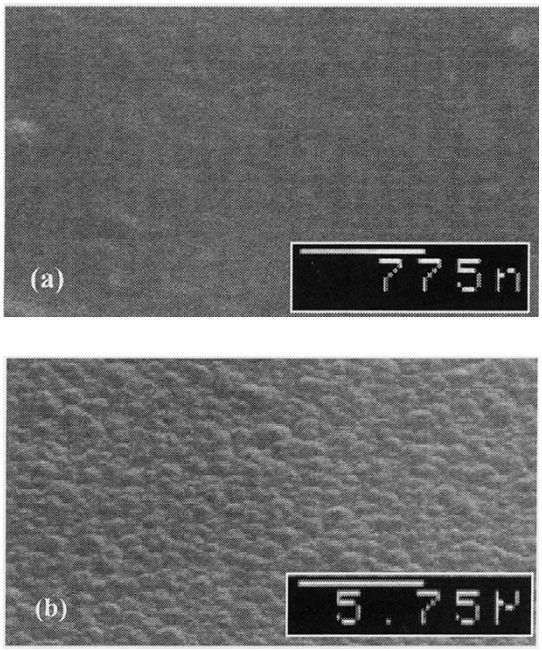


Fig. 13. SEM image of P-doped poly-SiGe layers deposited at 590 °C: (a) 2 μm and (b) 10.6 μm.

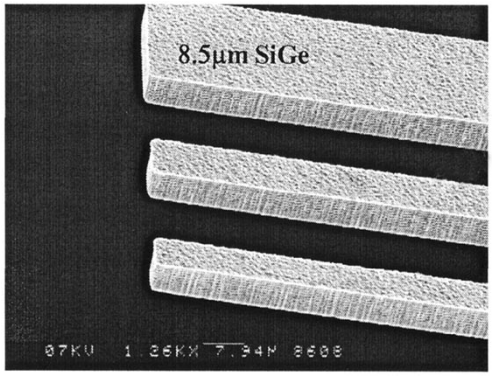


Fig. 14. Dry plasma etch of 8.5 μm thick poly-SiGe layer deposited at 550 °C.

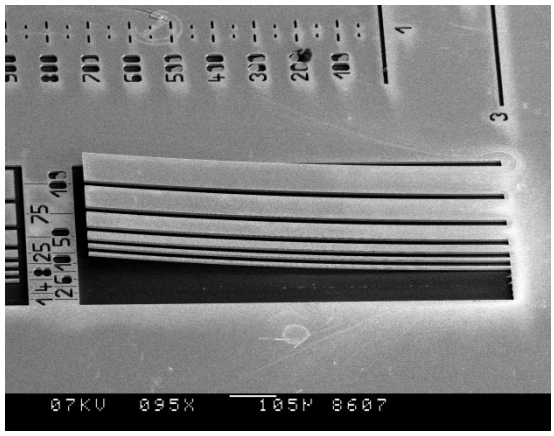


Fig. 15. Surface micromachined 8.5 μm thick and 1 mm long poly-SiGe cantilever deposited at 550 °C.

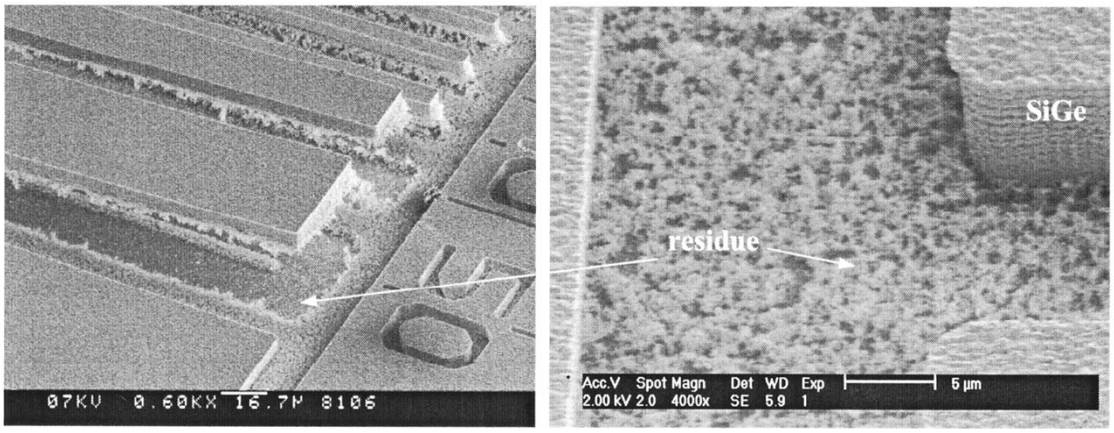


Fig. 16. Residues that occur after vapor HF of PECVD SiO_2. The residues are located on both the substrate and on the released cantilevers.

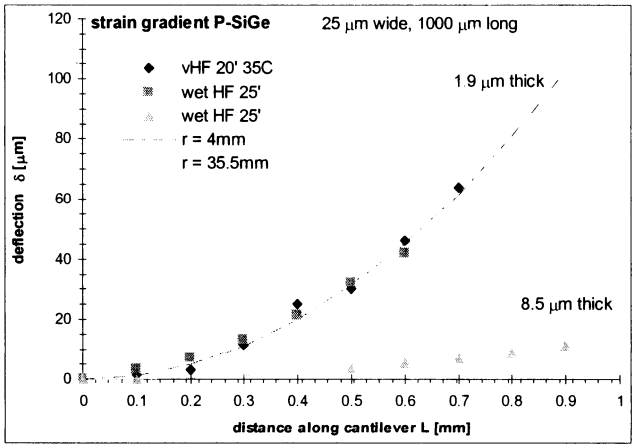
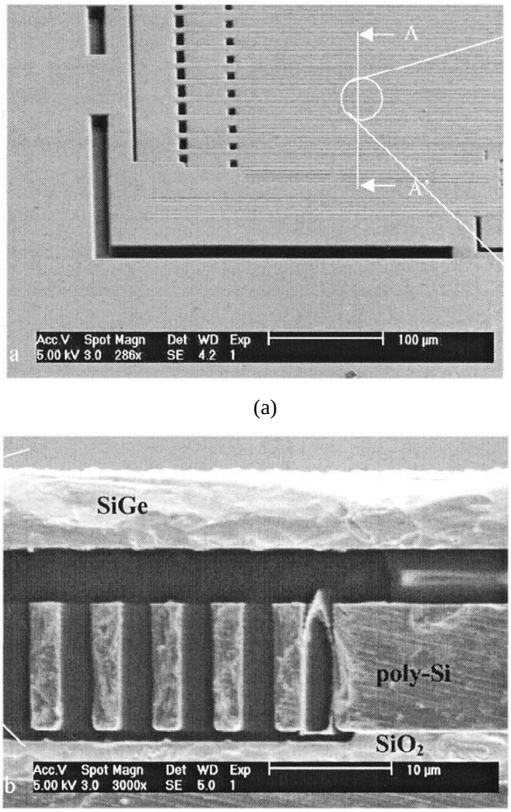


Fig. 17. The deflection of 1.9 μm and 8.5 μm thick poly-SiGe cantilevers deposited at 550 °C due to the stress gradient.



(a)

(b)

Fig. 18. (a) Before (top view) and (b) after (cross section) deposition of 8 μm PECVD poly-SiGe as encapsulating layer above a Bosch accelerometer and HF etching of sacrificial SiO_2.

D. MEMS Application

The high deposition rate and low deposition temperature of these PECVD poly-SiGe layers make them ideal membrane layers for thin film encapsulation of MEMS structures [16], [17].

For example, an 8 μm thick PECVD poly-SiGe layer is forming a protective membrane above an accelerometer (see Fig. 18). This is from a test run for encapsulating an accelerometer with a membrane. The sacrificial layer in this case was removed by HF etching after cleaving the sample with the membrane. For the final run etching will happen through holes in the membrane, which are sealed afterwards. This work is still ongoing.

A deposition rate of 200 nm/min ensures an economical process and the 550 °C or 590 °C deposition temperature guaranties that no structural changes occur in the underlying poly-Si functional layer.

IV. Conclusion

The use of PECVD SiGe offers a substantially higher deposition rate compared to thermal SiGe deposition processes. Moreover, plasma enhanced deposition gives the possibility of direct deposition on SiO_2, without the use of a nucleation layer. This nucleation layer, amorphous Si, might be a non- or poorly conducting layer, leading to a high resistance.

The B-doped SiGe films grown at 400 °C display low stress values when annealed at low temperature (450 °C and 520 °C), but resistivity is high. Low resistivity but high stress is obtained after annealing at high temperature (600 °C). These results indicate that deposition at a temperature higher than 400 °C is needed to get membrane layers with both low stress and resistivity values.

Low tensile stress and low resistivity polycrystalline layers can be obtained for both types of dopant (boron or phosphorus) if the temperature and the germane flow rate are high enough

($T \geq 520$ °C and germane flow rate $>12.5\%$ of silane + germane gas mixture). Moreover thick PECVD P-doped SiGe layers can be deposited predominantly polycrystalline at a temperature as low as 520 °C, with a growth rate of 0.2 $\mu\mathrm{m}/\mathrm{min}$ and with low tensile stress $(+50\ \mathrm{MPa})$ and low resistivity (18 $\mathrm{m}\Omega$-cm). Fully crystalline layers are obtained at 590 °C. These thick layers can be used as encapsulation layers for wafer level packaging in case the thermal budget is limited.

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Luc Geenen, photograph and biography not available at the time of publication.

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Bert Otter, photograph and biography not available at the time of publication.